Explicit Gate Delay Model for Timing Evaluation *

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ABSTRACT

Delay evaluation is always a crucial concern in the VLSI design and it becomes increasingly more critical in the nowadays deep-submicron technology. To obtain an accurate delay value, the gate modeling is a key issue. As the VLSI feature size scaling down and meanwhile operating frequency increasing, the modeling work becomes more difficult than ever for high-performance digital ICs. Nevertheless, most conventional techniques of gate modeling are based on the switch-resistor model (i.e., a voltage source concatenating a driving resistance), which can only capture the gate characteristic in its switching region. Hence, these modeling techniques have to decouple the gate with its interconnects and compute a piecewise linear function for the driving source in the iterative computation of effective capacitance [1, 3, 4]. Since the driving source of the model is dependent on gate load, when the design modification affects the load, the gate has to be modeled again almost from the beginning for a new timing analysis. The efficiency will be deteriorated in synthesis loops due to this. In this paper, we present an explicit gate delay model, which is not sensitive to gate load and can be pre-computed before timing analysis and synthesis. Thus, the repetition of modeling work is totally unnecessary even when the gate load keeps on changing in the performance optimization procedure. The efficiency is certainly improved in the synthesis/optimization loops. The advantage is attributed to using a second-order circuit as the model base. This two-pole approach also certifies the model to yield an accurate result to match the non-linear output of gate.

*This work was partially supported by the National Science Foundation under grant CCR-0244236.

ISPD'03, April 6–9, 2003, Monterey, California, USA.

Categories and Subject Descriptors

B.7.2 [**Integrated Circuits**]: Design Aids — *Simulation*; J.6 [**Computer Applications**]: Computer-Aided Engineering — *Computer-aided design(CAD)*

General Terms

Design, Experimentation

Keywords

gate delay model, explicit, pre-characterize

1. INTRODUCTION

As the feature size of VLSI decreasing to deep-submicron region, the delay caused by interconnects becomes the dominant portion in signal delay. Meanwhile, the delay contributed by the gate keeps reducing. The techniques on how to evaluate interconnect delay efficiently and accurately are developed rapidly, such as AWE [13, 15], PVL [7]. In contrast, since the gate is composed of non-linear components, it is difficult to be modeled effectively and precisely. Traditionally, a gate is modeled as a step voltage source in series with a linear resistance, or by empirical formulas in which the gate output parameters are functions of input transition time and load capacitance. However, with the IC technologies advancing, when the driver impedance does not dominate the metal resistance of interconnect any more, these models begin to suffer inaccuracy problem. Therefore, some techniques are proposed to improve the above gate model by turning the step voltage source into a time-varying piecewise one and choosing the value of the series resistor more elaborately. Such approaches to how to assign the parameters of voltage source function and the series resistance are presented in [1, 3, 4, 5].

In practice, given a gate, its input signal, sinks and interconnects that the gate drives, usually our object for the timing analysis is to obtain the voltage waveform of gate fan-out point at each sink. By comparing the input signal with fan-out point waveform, we can get the values of delay and signal slew over the whole circuit, as illustrated in Figure 1. However, based on most of the proposed gate models, the fan-out point waveform can not be deduced directly from the gate input signal since the gate model is not *a priori*. In the

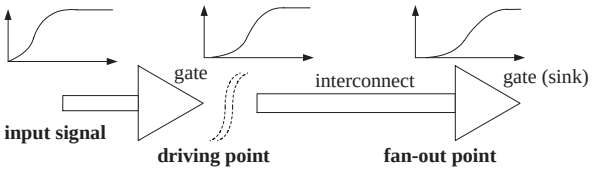

Figure 1: A gate drives its interconnects and receivers (sinks).

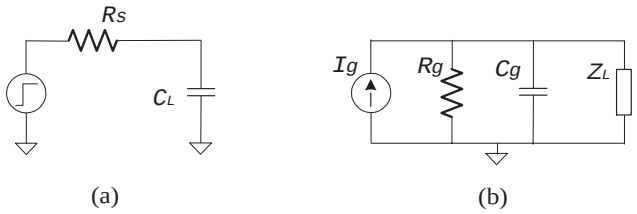

Figure 2: (a) switch-resistor model (b) effective current model

procedure of gate modeling, the information of gate load is required. Moreover, the load is needed to reduce to an "effective capacitance". The derivation of the voltage source for a model circuit is combined with an iterative computation of effective capacitance. Thus, the calculation of effective capacitance is an important procedure in the gate modeling process. However, most of techniques on the computation of effective capacitance [14, 16] are not explicit and they need several iterations to converge. Although some computation methods of effective capacitance [8, 9] are iterationless, the accuracy is sacrificed. Moreover, even if it does not take too much time for computing the effective capacitance once, when it is applied in the tight synthesis-analysis loops, the evaluation procedure may need to be repeated hundreds of times under any design modification affecting the gate load, and consequently, the runtime may not be affordable under this situation. Therefore, in this paper, we propose an explicit gate delay model with the following three characteristics:

1) the work of gate modeling is independent of its load;
2) compatible with techniques of the interconnect timing analysis;
3) concise circuit structure.

The first point of characteristic of this model makes it possible to pre-compute the gate model before the start of any timing analysis and synthesis, and then it is not needed to do the gate modeling again. The derivation of this gate model does not rely on the gate loading induced by interconnect and sinks. Hence, the time-consuming calculation of the effective capacitance is totally unnecessary in the new model. This significantly speeds up the procedures of timing analysis, particularly in optimization loops. Moreover, based on the second characteristic, the gate model can be incorporated into the process of interconnect delay evaluation seamlessly. Since it is not necessary to decouple the gate with its interconnect analysis, we can do the timing analysis all the way from the gate input to the fan-out point and get the stage delay directly. In addition, the third characteristic certifies that this unified analysis keeps almost the same complexity as the original one since there are only several linear components being added into the timing analysis of interconnect.

The rest of the paper is organized as follows. In section 2, we review some previous work on the gate modeling. In section 3, a new explicit gate modeling technique is presented and the comparison with previous models is given. We show the experimental results of this new model in Section 4. Finally, the conclusion on this modeling technique is drawn in section 5.

2. PREVIOUS WORK ON GATE MODEL

At the early developing stage of VLSI technology, the gate output impedance dominates the metal resistance of interconnect, and thus, for capturing the characteristic in the switching region, the gate can be modeled as a step voltage source in series with a linear resistance R_s, as shown in Figure 2(a). This model is denominated as the switch-resistor model. The value of the resistor R_s is empirically approximated by fitting the gate output characteristic of different loads. This model has gained prevalent acceptance since it is simple in structure and can be easily incorporated in the interconnect timing analysis. Another approach to the gate modeling is to express the shift and transition time of gate output waveform at driving point as functions in term of the transition time of gate input signal and load capacitance. Among this kind of models, the well-known k-factor functions is a typical one, which is widely used in industry to empirically pre-characterize the gate.

However, with the IC technology scaling down, the resistive and inductive shielding of interconnect keeps on increasing and the gate load can not be considered as purely capacitive impedance. Thus, approximating the gate load by the total capacitance "seen" from the gate output becomes more and more inaccurate. Many techniques on how to reduce the interconnect to a simple low order circuit are proposed. Although the second-order input admittance models(pi-model [12]) are often regarded as accurate enough for representing characteristics of the whole RC interconnect, the high order admittance models are sometimes needed for the interconnect timing analysis, particularly for those interconnects whose inductance is not negligible. An eight-order driving point admittance model is used in the effective capacitance computation algorithm for the RLC interconnect [1]. Due to lack of a circuit model of the above approach, a third-order realizable circuit is presented in [10] to improve the efficiency. However, owing to the complexity of high order circuit model, even the pi-model circuit, as far as the running time, is prohibitively expensive to be used in design optimization loops. Hence, for simplification and compatibility with previous gate delay models, it is usually preferred to reduce the interconnect into a single "effective" capacitance which, somehow, still captures the resistive shielding effect. With this effective capacitance, the driving point waveform can be easily characterized by k-factor functions or the voltage waveform can be derived by the switch-resistor gate model. However, the driving point waveform obtained from this two gate models may not always meet the accuracy requirement. To further improve the accuracy of gate model, the step voltage source in the

switch-resistor model is replaced by a piecewise linear voltage source. Then, incorporated into the process of effective capacitance calculation, a time-varying voltage function is iteratively derived. Moreover, the value of the series resistor R_s is obtained either in an iteration of a least-squares fitting to the SPICE result [3] or by computing each corresponding resistance with a sequence of increasing gate load capacitance until the resistance converges [1].

Recently, a gate delay model constructed on an effective current source is proposed in [11]. The current source I_g is in parallel to a resistance R_g and capacitance C_g, as illustrated in Figure 2(b). In this model, Norton's theorem is applied instead of Thevenin's theorem to the gate circuit and the voltage source in the switch-resistor model is replaced by a current source. That is the model's advantage to capture the characteristic of the voltage-controlled-current device by using the effective current directly. In this model, I_g and R_g are determined by the gate driving strength, C_g represents the equivalent parasitic capacitance of gate output. Another implicit parameter of this model is the gate intrinsic delay T_0. These four parameters can be derived from four equations, which are obtained by setting up the relationship between parameters of the model circuit and gate characteristics drawn from k-factor functions. Thus, one of the key points to determine the accuracy of this gate model is the fidelity of the empirical k-factor functions. In addition, I_g is a constant current source in this model and this is equivalent to a step voltage source, however, this is not the assumption of k-factor model. Although this can be solved by setting I_g to be time varying and limiting the maximum product of I_g and R_g to be V_{DD}(power supply voltage), it will surely make the model much complicated. Furthermore, to improve the integrity of output waveform of this model, particularly for the exponential tail area, the gate output area has to be divided into two parts by the empirically-derived threshold voltage. However, since the product of I_g and R_g is not always equal to V_{DD}, the tail area may not be totally fitted by this model. Another problem of this model is that, besides the four equations mentioned above, there exists another equation in term of the model parameters and $t_d(0)$, which is a constant in the k-factor functions. However, this extra equation can not always be satisfied by the model parameters derived from the first four equations. The reason is that this gate model does not fully match the model of k-factor functions, whereas all the parameters of this model is derived from equations based on k-factor functions.

Summarizing from the above models, we notice that the foundations of these models are all built on a first-order RC circuit and the inherent one-pole characteristic of this circuit makes it unable to fully fit with the non-linear output of a gate, particularly in the nowadays deep submicron technology. Thus, to compensate it, the driving source of model circuit has to be set to a time varying one, such as linear piecewise. This instead complicates the "simple" model on the other aspect. Moreover, in most of these modeling techniques, it is needed to incorporate the iterative computation of effective capacitance into the gate modeling process to derive the driving source function. This approach not only is time-consuming but also makes these models related to gate loads, and consequently, any design modification may cause the modeling work to be repeated from beginning. Hence, it is very expensive for these gate modeling techniques to be applied in design synthesis/optimization loops.

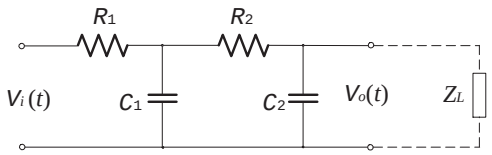

Figure 3: The new gate delay model is based on a second-order circuit.

3. EXPLICIT GATE DELAY MODEL

Instead of employing the first-order circuit of the switch-resistor model, we construct the new gate model on a second-order circuit, which is shown in Figure 3. In theory, a two-pole approximation is applied to fit to the characteristic of gate output instead of one-pole as before.

The transfer function of this second-order RC circuit is as follows

$$H(s) = \frac{\frac{1}{R_1R_2C_1C_2}}{s^2 + \left(\frac{1}{R_1C_1} + \frac{1}{R_2C_1} + \frac{1}{R_2C_2}\right)s + \frac{1}{R_1R_2C_1C_2}} \quad (1)$$

Suppose that p_1, p_2 are the two poles of the second-order RC circuit, and k_1, k_2 are the two corresponding residues. Then, the transfer function can be expressed by poles and residues.

$$H(s) = \frac{k_1}{s + p_1} + \frac{k_2}{s + p_2} \quad (2)$$

Thus, the relationship between the two poles and the four parameters of the RC circuit can be obtained from the comparison of equation (1) and (2) as the following two equations

$$\begin{aligned} p_1 + p_2 &= \frac{1}{R_1C_1} + \frac{1}{R_2C_1} + \frac{1}{R_2C_2} \\ p_1 \cdot p_2 &= \frac{1}{R_1C_1R_2C_2} \end{aligned} \quad (3)$$

In addition, the relationship of the two residues and the two poles can be rewritten as

$$\begin{aligned} k_1 &= \frac{p_1 \cdot p_2}{p_2 - p_1} \\ k_2 &= \frac{p_1 \cdot p_2}{p_1 - p_2} \end{aligned} \quad (4)$$

Supposing that, in time domain, the input voltage $V_i(t)$ of this circuit is a unit step signal, the output response $V_o(t)$ in term of the two poles and residues can be expressed as follows.

$$V_o(t) = 1 - \frac{k_1}{p_1}e^{-p_1t} - \frac{k_2}{p_2}e^{-p_2t} \quad (5)$$

If we know two operating points (v_1, t_1), (v_2, t_2) in the voltage curve of the gate output $V_o(t)$, with equation (4), p_1 and p_2 can be derived from the above equation. The two specific points are so chosen that the value of their voltages are 20% and 80% power supply V_{DD} of the circuit, respectively. By substituting (v_1, t_1), (v_2, t_2) into the above equation, we can get the following two functions of p_1 and p_2.

$$1 - \frac{k_1}{p_1} e^{-p_1 t_1} - \frac{k_2}{p_2} e^{-p_2 t_1} = 0.2 \tag{6}$$

$$1 - \frac{k_1}{p_1} e^{-p_1 t_2} - \frac{k_2}{p_2} e^{-p_2 t_2} = 0.8 \tag{7}$$

Under the assumption that $p_1 < p_2$, the second point (v_2, t_2) is quite near the end of the exponential tail area of gate output, thus the third term in equation (7) is negligible compared to the second term. Hence, p_2 can be expressed in term of p_1

$$p_2 = \frac{p_1}{1 - 5e^{-p_1 t_2}} \tag{8}$$

By substituting the above equation and (4) into equation (6), we can obtain a function, in which p_1 is the only unknown parameter. After getting the value of p_1, we can derive p_2 from equation (7), however, in most cases, it only sacrifices $10^{-4} \sim 10^{-5}$ accuracy to solve p_2 directly from equation (8).

Obtaining p_1 and p_2 is not enough for solving the four unknown parameters in this circuit, i.e. R_1, R_2, C_1 and C_2. We need two more functions in term of these parameters. Thus, we load the gate with a capacitance C_L and denote p_1' and p_2' as the two poles in the loaded circuit. Supposing that two operating points are obtained from the output curve of this loaded circuit, whose voltages of these two points are still 20% and 80% of V_{DD}, respectively, then p_1' and p_2' can be derived from these two points by the same method applied to p_1 and p_2. The relationship between p_1', p_2' and the circuit parameters can be expressed by the following two equations

$$\begin{aligned} p_1' + p_2' &= \frac{1}{R_1 C_1} + \frac{1}{R_2 C_1} + \frac{1}{R_2 (C_2 + C_L)} \\ p_1' \cdot p_2' &= \frac{1}{R_1 C_1 R_2 (C_2 + C_L)} \end{aligned} \tag{9}$$

The four parameters in the circuit of gate model can be deduced from functions (3) and (9) as follows.

$$\begin{aligned} C_2 &= \frac{p_1' p_2' \cdot C_L}{p_1 p_2 - p_1' p_2'} \\ R_2 &= \frac{\frac{1}{C_2} - \frac{1}{C_2 + C_L}}{p_1 + p_2 - p_1' - p_2'} \\ R_1 &= \frac{p_1 + p_2 - \frac{1}{R_2 C_2}}{p_1 p_2 \cdot C_2} - R_2 \\ C_1 &= \frac{1}{p_1 p_2 \cdot R_1 R_2 C_2} \end{aligned} \tag{10}$$

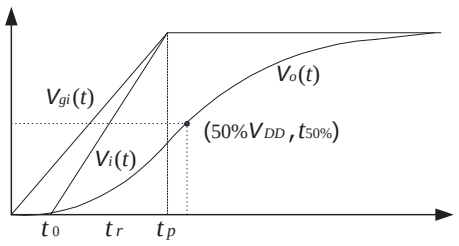

Figure 4: The gate input signal $V_{gi}(t)$ and output signal $V_o(t)$, the model circuit input signal $V_i(t)$. When the input signal of the gate is $V_{gi}(t)$, $(50\%V_{DD}, t_{50\%})$ is the point in the gate output waveform, whose voltage is 50% of power supply V_{DD}.

In the above loaded circuit, the value of C_L can be chosen in the range of maximum load that the gate may drive. Moreover, in the calculation process of the first two poles, p_1 and p_2, we may also load the gate with a capacitance C_{min} instead of zero load. This capacitance value can be set as the minimum load that the gate may drive, e.g. minimum value of input capacitance among all the receivers (sink gates). In this situation, every C_2 needs to be replaced by $C_2 + C_{min}$ in equation (3) and the other derivation procedure of the four circuit parameters is exactly the same as the original one.

There are two ways to get the four operating points that we need for the calculation of these poles. One way is to run SPICE twice to obtain the two groups of (v_i, t_i). We will demonstrate it later that this model can be pre-computed before any synthesis loops and it is not needed to do the modeling again after it is done even if the load of gate is changed, therefore, running SPICE twice here is affordable. The other way is to get the four points directly from the gate k-factor functions. Since the operating points at 20% and 80% of V_{DD} are mostly the interpolation points for k-factor functions, it is usually accurate enough for this two points in practical use. Although what we can get from the k-factor functions are gate delay t_d and transition time t_f, values of time at 20% and 80% V_{DD} points can be deduced from them as

$$\begin{aligned} t_{20\%} &= t_d - 0.3 t_f + 0.5 t_p \\ t_{80\%} &= t_d + 0.3 t_f + 0.5 t_p \end{aligned} \tag{11}$$

where t_p is the transition time of input signal and it is equal to 0 in the step input signal.

Assuming that the actual input signal of gate is $V_{gi}(t)$, the input signal $V_i(t)$ of the modeling circuit would not be exactly the same as $V_{gi}(t)$ since we need to take the gate intrinsic delay and signal driving ability into consideration. Supposing that the gate input is a saturated ramp waveform, whose transition time is t_p, and the gate has a positive polarity output(the same method for the negative one), we convert $V_i(t)$ to a shifted saturated ramp waveform, as shown in Figure 4. Denote t_0 as the shift time of $V_i(t)$ and define γ as t_p/t_r, where t_r is the transition time of $V_i(t)$.

Hence $V_i(t)$ can be expressed as

$$V_i(t) = \begin{cases} 0 & t < t_0 \\ V_{gi}\left(\gamma(t-t_0)\right) & t_0 < t \le t_p \\ V_{gi}(t) & t > t_p \end{cases} \quad (12)$$

In practice, $V_{gi}(t)$ does not have to be saturated ramp waveforms. For any input signal, the above function is still applicable. However, let us yet use the saturated ramp waveform as the gate input to make for brevity. In the following derivation, we will show how to obtain the parameter γ. If we set the origin of time coordinate to t_0, $V_i(t)$ can be expressed in s-domain as

$$V_i(s) = \frac{1}{s^2 t_r}(1 - e^{-st_r}) \quad (13)$$

By multiplying $V_i(s)$ with the circuit transfer function in equation (2), we can get the gate output $V_o(s)$ in s-domain as

$$V_o(s) = \frac{1}{s^2 t_r}(1 - e^{-st_r})\left(\frac{k_1}{s+p_1} + \frac{k_2}{s+p_2}\right) \quad (14)$$

The above s-domain gate output can be transformed into time domain where t_0 is the origin.

$$V_o(t) = \begin{cases} \dfrac{t}{t_r} + \dfrac{1}{t_r}\displaystyle\sum_{i=1}^{2}\frac{k_i}{p_i^2}\left(e^{-p_i t} - 1\right) & 0 \le t < t_r \\ 1 + \dfrac{1}{t_r}\displaystyle\sum_{i=1}^{2}\frac{k_i}{p_i^2}\, e^{-p_i t}\left(1 - e^{p_i t_r}\right) & t \ge t_r \end{cases} \quad (15)$$

The voltage of $V_o(t)$ is set to be zero when the time is prior to t_0.

In order to obtain γ, we need to derive the value of t_r from one of operating points in the gate output curve. Supposing that the time when the voltage of gate output reaches 50% of V_{DD} is after the transition time t_p, we record this point as $(50\%V_{DD}, t_{50\%})$. By substituting the values of this point into the second function of equation (15), we can get the function of t_r as follows. (If $t_{50\%}$ is within the input transition time t_p, we can employ the first function of equation (15).)

$$0.5t_r + \sum_{i=1}^{2}\frac{k_i}{p_i^2}\, e^{-p_i(t_{50\%} - t_p + t_r)}\left(1 - e^{p_i t_r}\right) = 0 \quad (16)$$

In the above equation, t_p is the transition time of the gate input waveform $V_{gi}(t)$, more specifically, it is the time limit when gate input signal comes out transition area. The waveform of $V_{gi}(t)$ is intentionally chosen before the process of calculating t_r, thus $V_{gi}(t)$ is a known waveform, and t_p is a known parameter. Moreover, since p_1, p_2 and k_1, k_2 are obtained in the previous calculation, t_r is the only unknown parameter in the above function. Once t_r is obtained, γ is determined.

Although γ is derived from a specific gate input signal, it is applicable to any other input waveform since the value of γ is mainly depended on the equivalent pull up/down resistance and parasitic capacitance of the gate, which are the fundamental factors to determine the gate intrinsic delay and signal regenerating capability. Actually, the four parameters R_1, R_2, C_1 and C_2 of the gate modeling circuit are primarily determined by the gate driving strength, too. Even when we look into the switch-resistor model, we notice the value of the linear resistance in this model is much related to inherent characteristic of the gate rather than its load. When the output equivalent impedance of gate dominates metal resistance of interconnect, this model can successfully capture the characteristic of the switching behavior of the gate, but usually fails in the output tail area since the driving strength in switching region is much different from that in exponential tail region. In [1], it is shown that this model resistance converges to a fixed value as the gate load keeps on increasing until its load capacitance dominates the parasitic capacitance of the gate. The accuracy problem of the switch-resistor model is originally caused by constructing its base on a first-order circuit and modeling the non-linear device by only one-pole approximation. This pole is determined by the gate driving resistance and the load capacitance. Thus, when the gate output impedance dominates its loading resistance, this pole can overwhelm the other poles in such circuit. However, with the resistive load of interconnect increasing, the poles induced by the resistance of interconnect become comparable to the dominant pole, the one-pole approximation begin to bring about more and more error into results of this gate model so that its accuracy is not acceptable. In order to yet employ this traditional simple model and improve its accuracy, the driving source of it has to be modified to nonlinear to fit the output of the gate. The nonlinear voltage source of the gate model is obtained from the effective capacitance of the gate load. This makes the gate modeling to be related to its load tightly. Based on this observation, we improve the model by using a second-order RC circuit as the base of the gate model. The characteristic of the gate output is fitted by exploiting a two-pole approximation and the poles of the base circuit is not dependent to the load of the gate. Experimentally, it is shown that this second-order circuit is accurate enough for the gate modeling when the resistive effect of interconnect is significant.

Remark 1

The pull-up and pull-down capability of a gate may not be identical, particularly in some circuits, such as dynamic logic circuits. They are innately unbalanced. Hence, it is better to model the gate in its rising and falling transition output separately in order to diminish the model error caused by the gate strength difference in the pull-up and pull-down state.

Remark 2

The five parameters of this model, i.e., R_1, R_2, C_1, C_2 and γ, can also be obtained by exploiting the function of "OPTIMIZE" in the transient analysis offered in Star-HSPICE [2]. This alternative approach does not need to solve the non-linear equations (6), (7) and (15) but computing them from HSPICE directly. This approach may take more time than solving the non-linear functions, however, since the derivation of parameters in the gate model circuit is the pre-computation before timing analyses and syntheses, it is

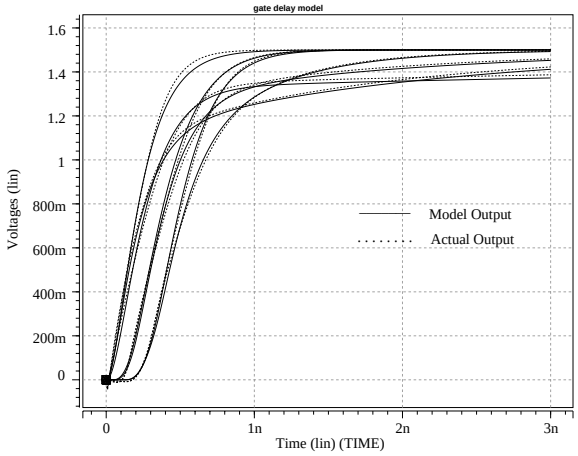

Figure 5: The output waveforms simulated by HSPICE on the gate model circuit and actual circuit of a 0.18μm technology inverter driving seven different loads. All the curves are the waveforms at gate driving point.

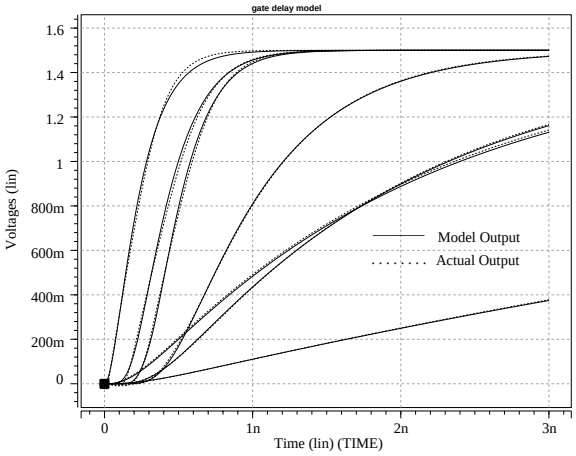

Figure 6: The output waveforms at the inverter fan-out point obtained from HSPICE simulations on the gate model circuit and actual circuit. The inverter, its load and input signal are the exactly same as the previous one.

still feasible in practice. In addition, the parameters derived from the non-linear functions can still be further optimized by this approach. In order to reduce the simulation time, the initial estimate of parameters in the gate modeling circuit is critical. We can take the known parameters of a similar gate as the initial values for the parameters derivation of a new gate model.

4. EXPERIMENTAL RESULTS

Since this new modeling technique is independent of gate load, it can be pre-computed and used as *a priori* in the delay evaluation. Thus, it does not require any repeated work on gate modeling in synthesis/optimization loops after the model is set up. On the contrary, most of the other gate models that are based on circuit of switch-resistor need to derive the ideal Thevenin voltage source from an iterative computation on the effective capacitance reduced from gate load. If the design modification changes the load, the iterative computation is needed to be repeated again to obtain a new driving source for the gate model. Therefore, for this new modeling technique, the saving of runtime spent on the gate modeling work in the synthesis/optimization loops is obvious.

Hence, in this section, we mainly focus on demonstrating the accuracy issue of this model. This new gate modeling technique is tested on buffers (positive and negative polarity) and NAND gates with different gate sizes, different fabrication technologies from $0.25\mu m \sim 0.10\mu m$, all together 36 different gates. In addition, 1,000 interconnects of different topologies are generated with wide range parameters based on the current and future manufactory technology [17, 18] and with wire length varying from $50\mu m$ to $5{,}000\mu m$. We test each gate by connecting it with 100 different interconnects randomly selected from the 1,000 interconnects being generated. The input signal is also randomly chosen from a signal library that contains 27 signals of different transition times. MOS transistor models used in HSPICE simulations are from level 13 to 49. Table 1 shows the average, maximum error and standard deviation(square root of the variance) of the signal delay at the driving point and fan-out points for all 3,600 experimental results. The error of this gate model are obtained from the comparison of HSPICE simulations on the model circuit and actual gate circuit. The error on the 20%-80% V_{DD} transition time is also shown in this table.

Table 1: The average, maximum error and standard deviation of the delay and transition time are obtained from the comparison of HSPICE simulations on this model and actual gate circuit at driving point and fan-out point for the 3,600 instances.

	error in delay		error in trans. time	
	d. point	f. point	d. point	f. point
Average	6.17%	3.79%	7.87%	4.90%
Maximum	14.62%	9.15%	16.61%	8.16%
Std. Dev.	8.35%	5.23%	9.52%	5.63%

trans. — transition d. — driving f. — fan-out
Std. Dev. — Standard Deviation

Figure 5 demonstrates seven waveforms obtained from HSPICE simulations on the modeling and actual circuit of a $0.18\mu m$ technology inverter. These waveforms are the inverter output at its driving point. The solid lines are the results obtained from the model circuit and the dotted lines are HSPICE simulations(Level=49) direct on the actual circuit of this inverter. In this experiment, the inverter drives seven different loads associated with three input signals of different transition times.

In the above experiment, the waveforms at fan-out point of this inverter are also obtained by applying HSPICE to the model circuit and actual circuit respectively. The seven pairs of corresponding waveforms are shown in the figure 6. It is demonstrated from this figure and figure 6 that

the output waveforms of the model circuit matches those of actual gate circuit much better at the fan-out point than at the driving point.

Furthermore, we applied our model to the timing analysis of the clock tree of a commercial IC. The results obtained from the model circuit are compared with HSPICE simulations on actual gate circuits. There are totally 1,417 subcircuits partitioned by the logic gates and buffers in the clock tree. For all these sbucircuits, the model average, maximum error and standard deviation of delay and 20%-80% V_{DD} transition time at gate driving point and fan-out point are shown in Table 2.

Table 2: The average, maximum error and standard deviation of the delay and transition time obtained from the comparison of HSPICE simulations on the modeling circuit and actual circuit for the clock tree of a commercial IC.

	error in delay		error in trans. time	
	d. point	f. point	d. point	f. point
Average	4.21%	2.75%	5.85%	3.28%
Maximum	8.29%	6.43%	9.12%	7.51%
Std. Dev.	5.69%	3.87%	6.92%	4.86%

trans. —— transition d. —— driving f. —— fan-out
Std. Dev. —— Standard Deviation

5. CONCLUSION

A new and explicit gate delay model is presented in this paper. This gate modeling technique is not dependent on its load, hence, the gate can be pre-characterized and, when the load of gate varies, there is no need to model the gate all over again once it is set up. This is a solution to the problem which is caused by the inefficient repetition of modeling work as the gate load keeps on changing in the design synthesis/optimization loops.

Since the model is compatible with interconnect timing analysis techniques, it can be seamlessly integrated into the interconnect analysis and synthesis loops. This integrated analysis will keep almost the same complexity as the original one due to the simplicity of the model circuit. There is no resistance connected to the ground in this gate model circuit, thus it can still keep the tree structure if the interconnect originally has tree topology. Furthermore, the statistical experiment results demonstrate the accuracy of this gate model in timing analyses.

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