Evolution of Low Power Electronics and Its Future Applications

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ABSTRACT

Low power technology is impacting our society by creating the newly emerging digital consumer market, which leads to the nomadic life-style. In this paper, historical review of the technologies will be provided with some examples. It is suggested that robotics will provide the major challenge for low power electronics in the coming decades.

Categories and Subject Descriptors

B.37.0 [**Integrated Circuits**]: General

General Terms: Design

Keywords

Low power technologies, Nomadic Age, Applications, Robotics.

1. INTRODUCTION

New trends in lifestyle in the ubiquitous society, which could be called as nomadic style, are wide spreading these days thanks to the rapid progress in microelectronics technology [1]. People are becoming more and more connected through communication networks and intelligent electronic terminals wherever they may be. Nomadic life style in the ubiquitous society will be more common as the constraints of time and location are broken. The low power electronics will play a key role in this nomadic age. Rather than describe and discuss the technical details of LSI chips, this paper will provide a broader and more historic view of the impact of the evolution of low power electronics and its future applications [2].

2. Figure of Merit in the Nomadic Age

Progress in semiconductor technology has led to smaller and lighter electronic devices. The trend in several such devices is illustrated in Fig. 1.

The first notable example is the electronic calculator, the size of which was reduced roughly three orders of magnitude in ten years. This drastic change was made possible by reducing the number of chips used. Electronic calculators initially used several thousands of transistors and diodes. The next generation used several tens of integrated circuits.

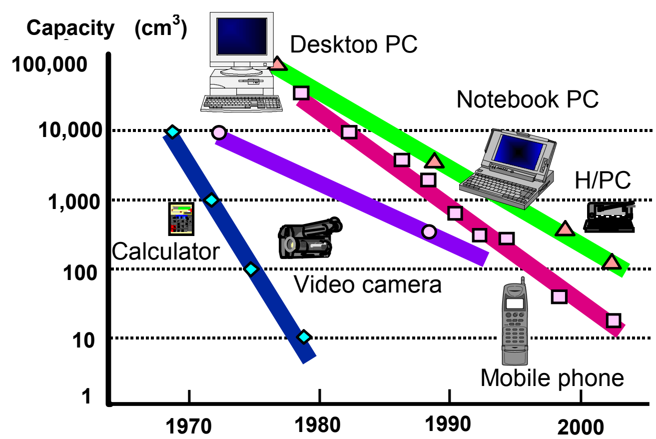

Figure 1. Electronic equipment toward smaller Size

The first LSI version, which was realized by the Rockwell-Sharp project, used four LSI chips. The current generation uses only one LSI chip to perform all the calculator functions.

Similar progress occurred with other electronic devices, including mobile phones and personal computers. Not only did electronic equipment get smaller, it got smarter. New functions were added, and the speed of operation was increased, as illustrated conceptually in Fig. 2.

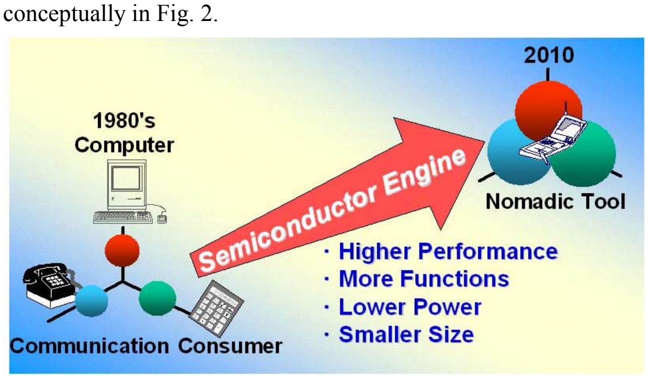

Figure 2. Nomadic tool

In the 1980's timeframe, there was a clear distinction between the markets for computers, communication terminals, and consumer devices. In the new century, we will be witnessing the introduction of tiny but powerful "nomadic tools", devices that can cover the functions of a PC, a telephone, and a calculator in the earlier days.

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The great success of *i*-mode cellular phone in Japan suggests the new development in this direction.

The basic requirements for such nomadic tools, summarized in Fig. 2, led to the formulation of a "figure of merit" for the nomadic age [3]:

$$\text{Figure of Merit} = \frac{(\text{Intelligence})}{(Size)\times(Cost)\times(Power)}$$

The ideal nomadic tool will be designed in such a way that it has more intelligence in smaller space at lower cost and at lower power. Reducing power dissipation is of primary importance in the nomadic age so as to achieve a longer battery life. This is to indicate the new direction of low power electronics in the new century, which is different from the PC-centric age in the past decade.

3. Historical Review of Low Power Technology

Since power dissipation is proportional to the square of the supply voltage, great efforts have been made to reduce the supply voltage. The trend in the supply voltage of semiconductor devices is shown in Fig. 4. A power supply of 24 volts was used in early devices in the 1960s. It was standardized at 5 volts in the mid 1970s, and 5 volts remained the most widely used supply voltage until the early 1990s. As the minimum feature size shrinks to the deep sub-micron range, the supply voltage has dropped to as low as 1.5 to 1.8 V. According to the 2002 ITRS, or International Technology Roadmap for Semiconductors, issued by the Semiconductor Industry Association [4], the supply voltage is expected be 1.2 to 0.9 V in 2005 and 1.0 to 0.6 V in 2010.

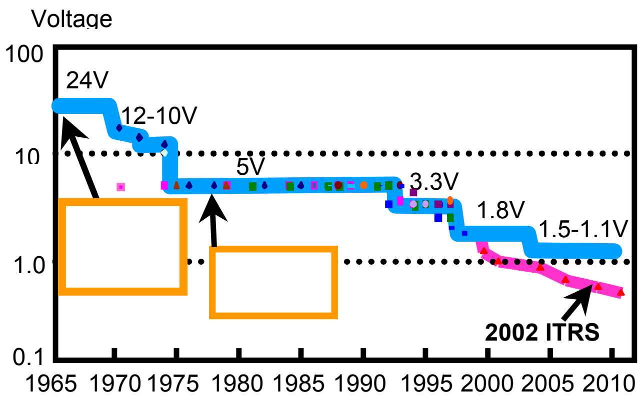


Figure 4. Trends of supply voltage

Innovation in device structure is another major approach to reducing power dissipation. Part of this progress could be called "CMOS convergence" since various device structures have been gradually converged to CMOS, except for some special applications.

CMOS has come a long way since RCA developed and introduced the device in 1963. In the initial stage of introduction, CMOS was superior in terms of power dissipation, but it was slower and more expensive. Additionally, the chips were larger than those using competitive technologies, such as NMOS.

This situation changed in 1978 when Hitachi pioneered the re-engineering of the CMOS device. Table 1 compares the features of NMOS and CMOS devices for SRAM in the late 1970's showing the superiority of CMOS over NMOS for the first time in the history [5]. Intel's 2147 chip was the fastest 4K static RAM at that time; it was based on NMOS technology and had an access time of 55-70 ns. Hitachi's 6147 chip was compatible with Intel's 2147, but was based on re-engineered CMOS technology. It had the same speed, but the power dissipation was only 1/8 that of the 2147 in active mode and 1/15,000 in standby mode. The 6147 devices from Hitachi got a lot of attention from both technical and management viewpoints. The typical comment was like this: "Hitachi's new CMOS chip would be great if it were producible in volume". Their success in volume production set the semiconductor industry on a new course.

Table 1. NMOS vs. CMOS for SRAM

	2147(1977)/Intel	6147(1978)/Hitachi
Product	HNMOS 4Kb Static RAM	HiCMOS 4Kb Static RAM
Technology	NMOS	Twin-Well CMOS
Speed	55 / 70 ns	55 / 70 ns
Iactive/Istandby	110 mA / 15 mA	15 mA / 0.001 mA
Chip Size	16.2 mm^2	11.5 mm^2

In 1981, Hitachi applied the same CMOS technology to an 8-bit microprocessor. As shown in Table 2 comparing to its NMOS counterpart, it was twice as fast, and its power dissipation was 1/30 in active mode and 1/7,000 in standby mode. It also contributed for setting the new direction of technology for microprocessors and logic devices.

Table 2. NMOS vs. CMOS Microprocessor

		680(1979)/Hitachi	6301(1981)/Hitachi
Product		8bit MPU	8bit MPU
Technology		4 micron NMOS	3 micron CMOS
Speed		1MHz	1/1.5/2MHz
Power	Active	900 mW	30 mW (f=1MHz)
	Standby	70 mW	0.01 mW
Pin Count		40 pins	40 pins

Figure 5 summarizes the history of semiconductor device structures. Simply stated, the past 30 years have been dominated by CMOS convergence. The original CMOS device developed by RCA was applied primarily to low-power devices, such as electronic watches, for which speed was not an issue. The next big market for CMOS devices was calculators with liquid-crystal displays, which also did not require high speed.

Hitachi's introduction of high-speed CMOS SRAM, 6147 in the late 1970s was the start of CMOS convergence for almost all types of products. In the 1980s, flash memory and DRAM shifted from NMOS to CMOS. The final step in CMOS convergence came in the 1990s, when servers and mainframes shifted from bipolar ECL/Bi-CMOS to CMOS. It is quite likely that CMOS will remain in the main stream of device structures for many years to come.

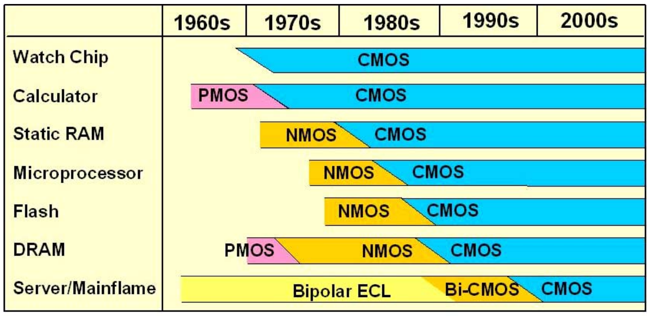


Figure 5. Shift in device structure

- 30 years for CMOS convergence-

4. Innovations in Architecture

The architectural innovations are also important for realizing the low power chips. The mainstream architecture of MPUs has been CISC because the majority of PCs was based on Intel's architecture. In the late 1980s, the RISC architecture was introduced; it was applied mainly to high-end machines such as workstations and severs. In the 1990's, re-engineering of the RISC architecture led to higher performance per unit of power, i.e., higher value of MIPS/Watt. ARM was the first product in this direction, and today, there are various architectures such as MIPS and SH in this category.

Figure 6 shows the distribution of MIPS vs. Watt for various types of processor architectures. The new generation RISC machines are far superior to the traditional CISC/RISC machines used for PCs and workstations in terms of MIPS/Watt. The power dissipation of new generation RISC micro is designed to be one or two watts or less, so that the chip can be packaged in less expensive plastic package. The net result is much improved cost effectiveness in terms of MIPS/cost. This is the main reason the new generation RISC machines are gaining in popularity for newly emerging digital consumer products.

Innovation in processor architecture is still proceeding, including the recent development of the Crusoe chip from Transmeta, which is based on an entirely new software approach and will greatly impact the direction of low power electronics.

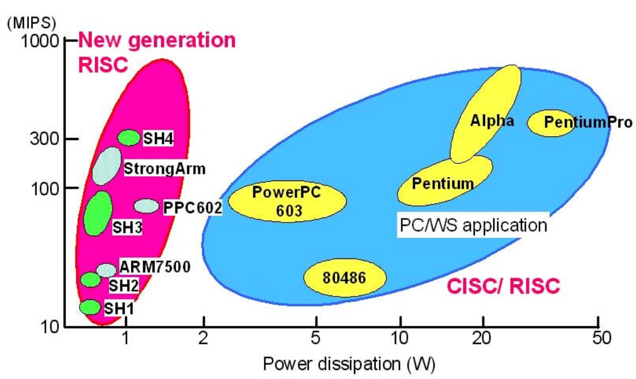


Figure 6. MIPS/Watt of various processors

Another innovation is the reconfigurable architecture for achieving the flexible low power ASPP or Application Specific Programmable Product. Dynamic reconfigurable circuit technology does not require multiple dedicated circuits for each operation. The technology enables an LSI to function according to each situation by altering its preset configuration. The basic idea is shown in Fig.7 in a conceptual way.

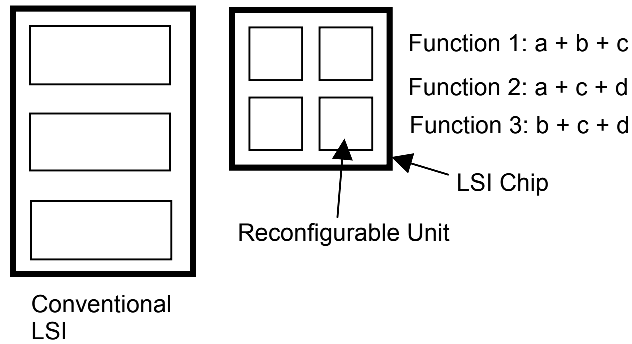


Figure 7. Schematic diagram of reconfigurable circuits

Sony's latest network walkman integrates re-configurable logic block as its audio codec engine, with the name of "Virtual Mobile Engine™". The features are shown in Fig. 8. This is the first dynamic re-configurable engine implemented in a consumer electronic product. Comparing with the DSP based system, the new device operates at 1/4 of power dissipation.

Chip Configuration	**One CPU with Embedded *"Virtual Mobile Engine™"***
Decoding Power Dissipation for ATRAC3*	**Ultra Low Power: 4mW (less than 1/4 compared to DSP)**
Feature	**Programmable**

*Audio Format

Product:NW-MS70D
W: 36.4 mm,
H: 48.5 mm
t : 18.0 mm

Figure 8. Sony's "Virtual Mobile Engine ™"

5. SoC and Emerging Markets

The "system on a chip", or SoC, will be a powerful way of achieving a low power and high performance chip. Figure 9 shows an example of SoC, a 3-D graphic chip, in which an 8Mb DRAM is integrated on a chip. When it was integrated into a single chip, the performance improved four times and the power dissipation dropped to one-fifth. These improvements are typical when shifting to a SoC from a system on board. Because of these great benefits, there will be a steady shift toward SoC, which will in turn promote the emerging market for digital consumer products, which require high performance, low power, and low cost.

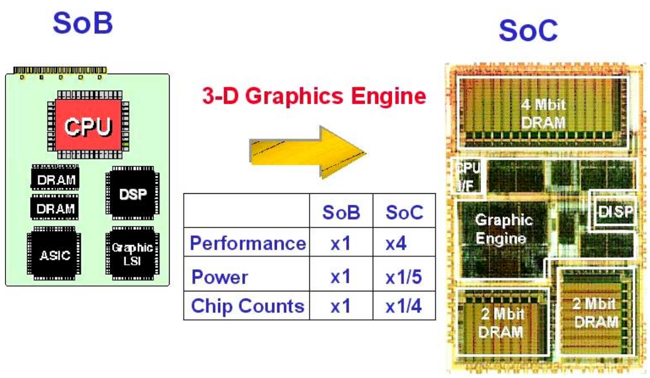
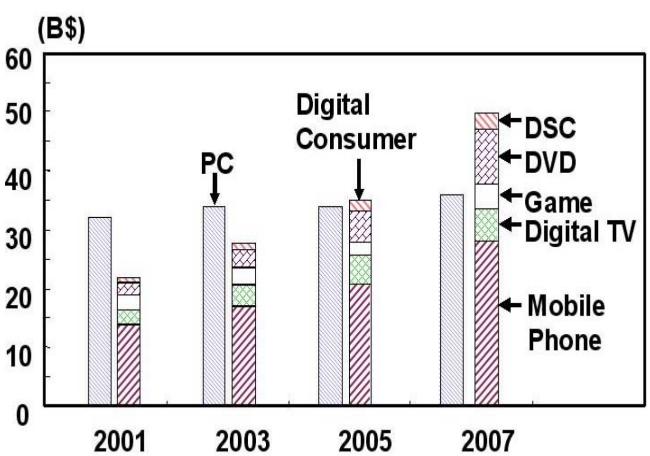


Figure 9. Example of SoC

Fig. 10 shows the trend in the semiconductor market for the Digital Consumer (DC) segment in comparison with the PC market. Mobile phones have the largest share of the DC segment today. However, various types of other products, including digital TV, game machines, DVD, digital cameras and in-car navigation systems are also gaining momentum.

The implication of the emerging DC market is that there will be a shift in the engine propelling the semiconductor market and technology, namely from PC to DC. Of course, this does not mean that the PC will disappear. However, the dominant role it played in the electronics industry during the last two decades will diminish, and it will be supplanted by DC products connected via communication networks. The low power electronics will be the most critical factor for succeeding in the emerging DC market.



Source: Future Horizons

Figure 10. Digital consumer market

7. Robotics as the Future Technology Driver

What will come after the digital consumer market? There is an increasing signal that robots will be a next driver of our industry.

Fig. 11 is to show the evolution of robot intelligence [6]. Generally speaking, the intelligence of today's robot is far inferior to human intelligence, especially in the fields of pattern recognition and language understanding.

However robot intelligence will dramatically increase in the coming decades, owing primarily to the progress of high performance and low power chip technologies. Fig. 11 shows a prediction of robot intelligence by Dr. Moravec of Carnegie Melon University [6]. Of course, it is not a simple issue to compare intelligence between a robot and a human, but this figure may give a kind of feeling of how the robot's intelligence will continue to rise. The robot will provide the biggest challenges for the low power electronics in the future, since the total power consumption is very limited in the range of several watts to several tens of watts. Therefore it is required to achieve very high value like 10^6 to 10^7 in terms of MIPS/Watt. How to achieve such figures of high target in the coming decades? That remains the major challenge for low power electronics.

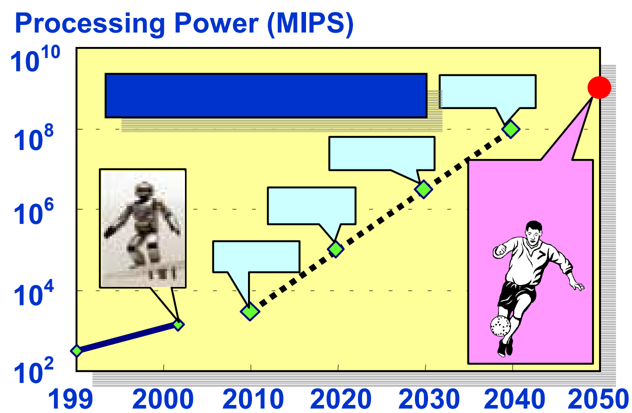


Figure 11. Evolution of robot intelligence

8. REFERENCES

[1] Tsugio Makimoto & David Manners, "Digital Nomad," John Wiley & Sons (1997)

[2] Tsugio Makimoto, "Cooler the better – New Directions in the Nomadic Age –" Keynote Address of Cool Chip III (April 24, 2000)

[3] Tsugio Makimoto, "Megatrends in The Nomadic Age," presentation material of In-stat (April, 1994)

[4] The International Technology Roadmap for Semiconductors (San Jose, SIA, 2002).

[5] T. Makimoto, "Some Aspect of Semiconductor Manufacturing in Japan," Dataquest Conference (Oct, 1981)

[6] T. Makimoto, Toshi T. Doi, "Chip Technologies for Entertainment ROBOTS – Present and Future –," Technical Digest of 2002 IEDM

[7] Peter Tester, "Universal robot: the history and working of robotics",http://www.thetech.org/exhibits_events/online/robots/apps/capek.html