Low Power RF IC Design for Wireless Communication

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ABSTRACT
In this paper, the many issues around the system and circuit design of advanced RF front ends for wireless RF applications will be discussed. After a short discussion on technology related issues, design choices linked to the different circuit/system solutions will be discussed.

Categories and Subject Descriptors
B.7.0 [**Integrated Circuits**]: general –

General Terms
Performance, Design, Experimentation, Verification

Keywords
RF, Technology, Transceivers, Wireless communication, Low power, VCO, PLL, LNA.

1. INTRODUCTION
Riding on the waves of success of both mobile phone (mobility) and the internet (interactive access), the need for portable broadband internet access emerged, to connect portable devices like laptops and PDAs to fixed stations and/or computer networks. Wireless Local Area Networks (WLAN) are currently the main driver of these applications, however the Wireless Personal Area Networks (WPAN) are coming up rapidly with standards as Bluetooth, ZigBee and Ultra Wide Band.

Linked to the rise of the mobile phone market, low power consumption of the total electronics has become extremely important for these wireless applications. In order to obtain really low power functions, measures should be taken from the very first stages of concept definition, covering all levels of the design: architecture, circuit and process technology. In contrast to purely digital electronics, which profit from the inherent power reduction of successive CMOS technology generations, RF power reduction is more difficult to obtain. RF power consumption is fundamentally linked to the required dynamic range of the received signals, and successive generations of RF IC technology, therefore, give only limited power consumption reductions. In this context it is also worth noting that the continuous power supply voltage reduction of modern bipolar and CMOS technologies to 1.0-1.2 V does *not* support lower power consumption (as we will see later). The lower voltages make it harder to reach the same dynamic range, at the expense of disproportional higher currents.

This paper will start with a discussion of all technology related issues, which affect the power dissipation of RF ICs. Then we will highlight some low power design techniques in a few RF building blocks. Finally a low power RF synthesizer and receiver will be discussed.

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2. Technology issues
Although any analog circuit performance depends on the used technology, this is especially true for RF design. High frequency designs not only rely on high performance active devices but also on passive components of high quality, like inductors, capacitors, and varactors.

Advanced BiCMOS technologies bring high performance active devices. Where the cut-off frequency f_T of a 0.5µm BiCMOS technology lies around 30 GHz, a 0.25µm BiCMOS process brings already an f_T close to 45 GHz, and the new generation SiGe BiCMOS technologies push the f_T over the 100 GHz boundary. Also the 'available bandwidth' f_A improves with newer process generations (see Figure 1) [1]. This parameter reflects the frequency at which the DC voltage gain of 20 dB drops with 3 dB and is related to the collector junction capacitance and the base resistance.

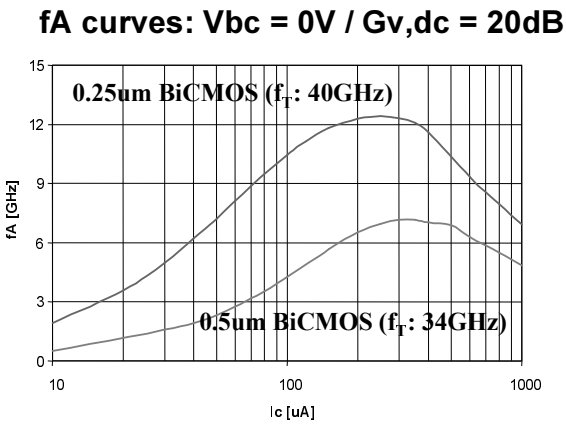

Figure 1. f_A as a function of the current for 2 bipolar devices.

The figure shows that a modern BiCMOS process allows higher operational frequencies at *lower* power dissipation.

A similar trend can be found in CMOS technology. The active devices in a deep sub micron CMOS process have good RF performances. For instance, a modern 0.18 µm process has similar f_A vs drain current behavior as the 0.25 µm BiCMOS technology of figure 1. The problem with CMOS is that the device layout determines highly the performance of the device. The choice of the folding ratio is crucial; increasing the folding factor lowers the gate resistance according to

$$R_{gate} = \frac{W \cdot R_{sheet}}{12 \cdot L \cdot fold^2} \quad (1)$$

and therefore improves the noise factor for the same current. However, too much folding lowers the cut-off frequency due to wiring parasitic capacitances, which in the end will pay off in power dissipation (see figure 2). A proper design trade-off to obtain is needed to achieve a low power design.

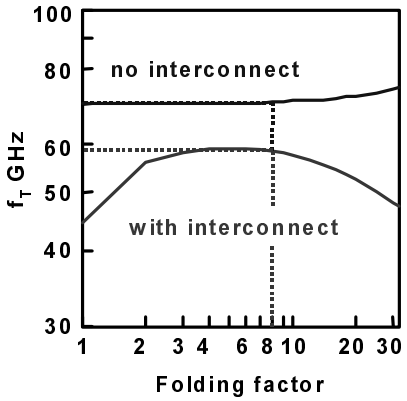

Figure 2. f_T as a function of the folding factor in 0.18µm CMOS.

Modern BiCMOS technologies provide thick top-metal layers, reducing the sheet resistance of the metal. In combination with high-resistive substrate and deep trench isolation, monolithic integrated inductors with moderate Q-factor values are possible. Furthermore, dedicated high-density MiM capacitors are offered, having less than 1% parasitic capacitance with respect to the actual capacitance. These high performance passives allow for instance fully integration of the tank circuit of the VCO, leading to a serious reduction in power dissipation. Although modern RF-CMOS processes offer similar back-end options as BiCMOS technologies, the quality of these options is less.

Although BiCMOS performs better than (RF)-CMOS, both technologies provide integrated inductors with poor/moderate quality factors. As we will see later, high quality factors help to design low-power oscillators. To improve the inductor's quality factor for a given technology geometry with parallel tracks may be chosen [2]. Due tot the parallel tracks, the path of the least resistance at low frequencies becomes the same path for the least inductance at high frequencies. An example of such structure is shown in figure 3 for two parallel tracks. Measurements indicate that a 40% improvement in quality factor can be obtained for almost the same die area, when 4 parallel tracks are used.

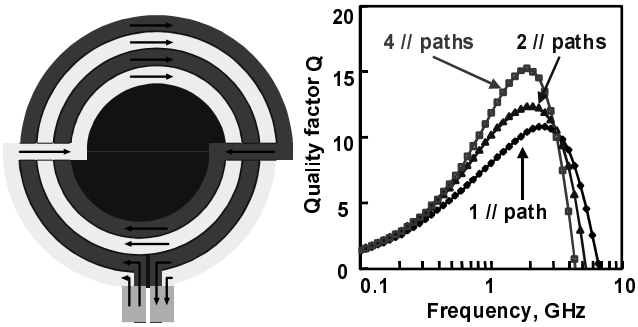

Figure 3. Geometry of a parallel track inductor and its performance in 0.18µm CMOS.

Similar performance improvements can be achieved for capacitors [3]. In this section we have indicated that low power design starts with the proper choice of the technology and the optimal layout strategy of the active and passive device solely. In the next sections we will focus ourselves to the circuit level.

3. RF building blocks

3.1 VCO

The voltage controlled oscillator (VCO) is a key RF building block, first because it will determine the maximum frequency in any tuner system and second because its spectral purity sets the signal quality in the transceiver. Figure 4 shows the basic concept of the LC-tank oscillator. The two cross-coupled active devices form a negative resistance, which must compensate the losses in the LC-tank due to positive resistance. The admittance of the active part can be calculated as a function of the transistor parameters and gives at DC

$$Y = \frac{-g_m}{2} \quad (2)$$

with gm the transconductance of the bipolar device.

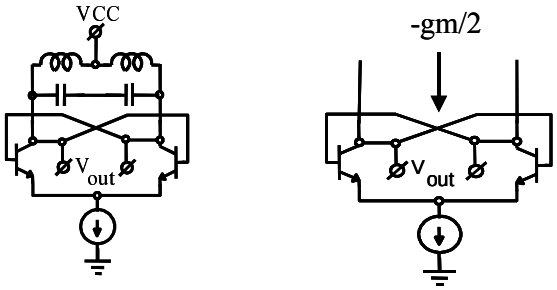

Figure 4. LC-tank oscillator (left) and active part (right).

However, at a certain frequency point f_{limit} this resistance becomes positive and oscillation is no longer possible. This limit is found to be proportional to f_T,

$$f_{limit} \propto \alpha \cdot f_T \tag{3}$$

where α is a function of transistor parameters [12]. Therefore a technology process with high f_T is favorable for high oscillation frequencies at low power dissipation levels. The phase noise PN at an offset frequency f_m from the free running oscillator frequency f_{osc} is in first order given by Leeson's equation [1],

$$PN(f_m) = \frac{1}{2} \cdot \frac{1}{Q_{LC}^2} \cdot \frac{F \cdot k \cdot T}{P_{RF}} \left(\frac{f_{osc}}{f_m} \right)^2 \tag{4}$$

where k is Boltzmann's constant and T is the absolute temperature in Kelvin. The noise factor F depends on the implementation, P_{RF} is the power dissipation and Q_{LC} the quality factor of the tank. This expression tells us that a given PN, low power VCO can be obtained using inductors with high quality factors.

For zero-IF demodulation quadrature LO signals are needed. Direct quadrature oscillators gain interest due to their inherent better phase matching. An example is shown in figure 5 [4].

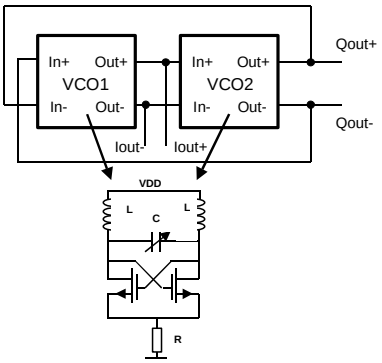

Figure 5. Block diagram of a quadrature VCO and schematic oscillator core.

The quality factor Q_{tot} of the cross-coupled oscillator is approximately given by

$$Q_{tot} = 2Q_1 \cos(\alpha) \tag{5}$$

where α is the phase shift of the LC resonator in each stage with quality factor Q_1 [5]. The phase shift in each stage should therefore be zero for optimum phase noise. However, the implementation of Figure 5 results in a phase shift close to 80 degrees, resulting in a 12 dB degradation of the phase noise. Instead of increasing the power dissipation to improve the phase noise (see (4)), one can insert a zero in the transfer function of the coupling circuitry to improve coupling [4]. This technique has been used to realize a low power, 7 mW only, quadrature VCO for Bluetooth in standard 0.18 µm CMOS. The resulting VCO has a 16% tuning range and a PN(3MHz) of -125dBc/Hz.

3.2 Frequency Dividers

Because the first stage of any frequency divider runs at the same frequency as the VCO and handles large signals, the design of this circuit is difficult and often consumes serious amounts of powers. The most commonly used prescaler configuration is based on the D-latch, as seen in figure 6. The clock signal runs at 2**f* while the output operates at *f*. When implemented in current-mode logic (CML) each latch consists out of a gate pair and a latch pair (see figure 7). At relative high current density levels to achieve peak f_T the dominant parasitic elements of the latch pair are the base-emitter diffusion capacitances, followed by the base-emitter and collector-substrate junction capacitances (see C_{par} in Fig. 7). To decrease the load, buffers can be used between two succeeding D-latches, however at the cost of power dissipation [6].

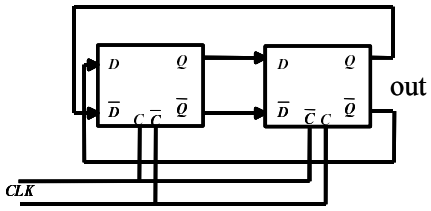

Figure 6. Frequency divider based on 2 D-latches

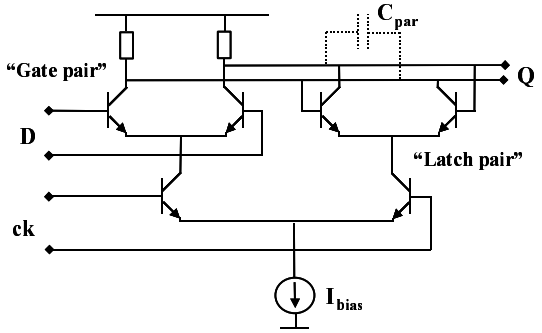

Figure 7. Schematic of one D-latch

One other option is proposed in [7] and suggests the use of separate bias currents for the gate pair and the latch pair (Figure 8). This enables the bias current of the latch pair to be set independently of the gate pair biasing current. A decrease of the latch pair parasitic junction capacitances can now be obtained by the choice of smaller transistor sizes, whereas the choice of a smaller biasing current I_{latch} results in a smaller parasitic diffusion capacitance of the latch pair transistors and a low power design.

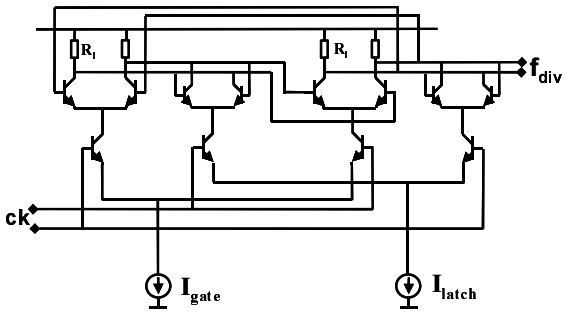

Figure 8. Adaptive divide-by-2

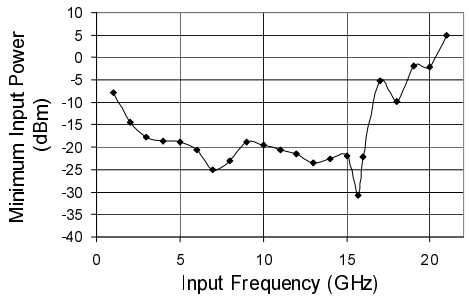

Figure 9. Measured input sensitivity

With this concept a low power 20 GHz static divider was realized in a 37 GHz f_T BiCMOS process, resulting in a high f_{in}/f_T ratio of 0.55. The measured input sensitivity is presented in Figure 9. The power dissipation is 11 mW.

3.3 Low-Noise Amplifiers

One of the key building blocks in any wireless system receiver is a low noise amplifier (LNA). The ultimate design challenge is to obtain noise match and power match for the same source impedance [1]. Deviation from ideal power match leads to reflections of the delivered power, and drop in available gain. To compensate for this lower gain more current in the input stage is needed at the cost of higher power dissipation.

This input power matching is highly related to the choice of the process in case of CMOS technology. Suppose the target specifications are a NF of less than 2 dB, a power gain of 10 dB, an input IP3 better than –10dBV and a source impedance of 50 Ω. Furthermore, for production reasons, the (external) matching network must have a Q less than 2.5 to reduce the sensitivity towards inaccuracy of the component values of the network. Figure 10 shows that for the same frequency the newer process generation will increase the power consumption, although the supply voltage drops (0.25 µm/2.5 V, 0.12 µm/1.2 V) [13]. The explanation is that for decreasing minimum gate length, the quality factor of the device's input impedance rapidly increases, due to decrease of the intrinsic gate-source capacitance. The drain current of the input device is given as

$$I_{ds} \propto \left(\frac{\omega_T}{\omega} \right)^2 \qquad (6)$$

where $\omega_T = g_m / C_{gs}$. To reduce the quality factor and achieving a good noise figure, the device's width must be increased at the cost of power dissipation. Therefore, the current is mainly determined by the restrictions on the Q of the matching network.

Extreme low power LNA designs can be obtained when the requirement of making gain at RF is made less restrictive. This gain can also be made at IF, at the cost of some noise figure performance. As example, consider once more Bluetooth. The overall noise figure for the radio must be 24 dB, a relaxed value. This means that the designer can focus more on input power match rather than noise match. Because of the low impedance level of the antenna, an impedance converter can be used (Figure 11). In CMOS it is easier to achieve high input impedance values

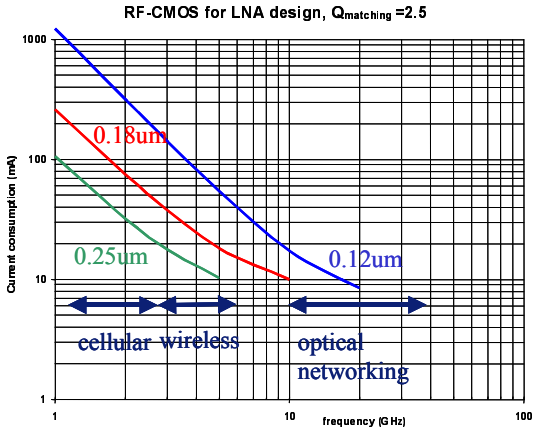

Figure 10. Current dissipation of LNA versus frequency for different processes.

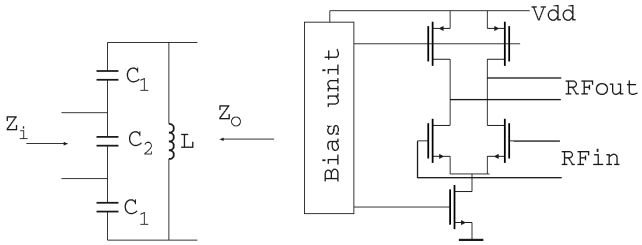

Figure 11. Low power LNA design.

rather than low input impedance values at low current levels. Assume that the output impedance of the impedance converter is 1000 Ω and the equivalent input noise impedance of the LNA is 4000 Ω, then the NF is close to 7dB, more than enough for Bluetooth applications. The equivalent noise impedance is approximately given by

$$R_n = \overline{e}_n^2 / 4kT\Delta f = \gamma / g_m \qquad (7)$$

A proper design can then lead to very low current consumptions. In a 0.18 µm CMOS technology this may lead to 0.2 mW, while achieving an input IP3 of –10 dBm and NF of 6.5 dB.

3.4 Some remarks

So far a few commonly used building blocks in RF radio systems have been discussed. We have seen that for production reasons the quality factor of the matching networks play a significant role. However, for production ESD protection is important too and may highly (negatively) affect the design of the LNA and the VCO if the tank is external. But designing high performance RF ESD structures is a challenge on its own [8]. Same holds for the choice of the package, will it be a low quality LQFP or a dedicated HVQFP, optimized for RF.

4. Low power RF synthesizer design

In this section we will demonstrate that an overall low power design can only be achieved if at all levels of design abstraction, the proper design choices have been made. As example we will take a RF frequency synthesizer for Bluetooth applications, operating from 2.4 GHz to 2.48 GHz with a channel spacing of 1 MHz.

The block architecture of a PLL frequency synthesizer is depicted in Figure 12. Single-loop integer-N architectures have the advantage of being simple and low power. Relating F_{out} to F_{div} and F_{ref} one readily obtains

$$F_{out} = N \cdot F_{ref} = N \cdot \frac{F_{xtal}}{R} \tag{8}$$

If the division ratio N is programmable in steps of 1, then F_{out} can be stepped with a minimum step size equal to F_{ref}, which is then equal to the channel spacing of the application.

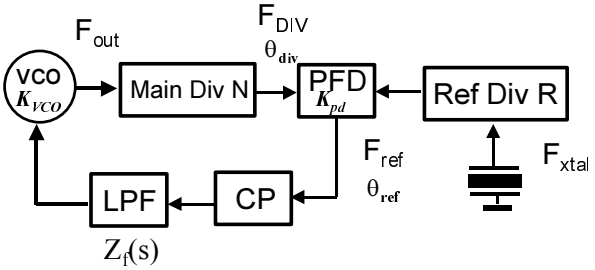

Figure 12. Block diagram of an Integer-N synthesizer.

The design requirements can be derived from the following Bluetooth system specifications: the minimum modulation depth leads to 115 kHz frequency deviation; the locking time t_{lock} is 200 µs; the PN must be less than –80 dBc/Hz at 1 MHz offset, -110 dBc/Hz at 2 MHz offset and –120 dBc/Hz at 3 MHz offset.

The settling time of the synthesizer is set by the bandwidth of the loop filter. A larger loop bandwidth gives a faster settling time and rejects more of the VCO phase noise. However, the higher the loop bandwidth, the higher the degradation of the residual FM of the closed-loop PLL in relation to the residual FM of the free-running oscillator [9]. Residual FM is an important specification in this application, as Bluetooth uses Gaussian-filtered Frequency Shift Keying (GFSK) modulation. Frequency noise is added to the received data and will degrade the SNR. Therefore, to minimize the residual FM degradation it is preferable to limit the loop bandwidth to the maximum necessary in order to comply to the settling time requirements. Following these design requirements we obtain a bandwidth of 20 kHz [10].

Now we have to find the values for the filter components and for the nominal charge pump current. Suppose a second-order passive network in order to reduce noise and power dissipation. The passive filter consists of a resistor R_1 in series with a capacitor C_1 and parallel to this capacitor C_2. There is a trade-off between the charge pump current I_{cp}, the loop filter area and the noise contribution from the charge pump and from the loop filter resistor R_1. Figure 13 shows that reducing I_{cp} results in smaller values to capacitors C_1 and C_2, enabling on-chip implementation. On the other hand, low power design requires a larger R_1 for a given value of the loop bandwidth, increasing the noise contribution from the loop filter. Besides, a lower charge pump current increases the noise contribution of the charge-pump to the equivalent synthesizer phase noise floor. An acceptable trade-off might be at a charge pump current of 8 µA. Then the residual FM in a bandwidth from 1 kHz up to 500 kHz amounts to 5 kHz.

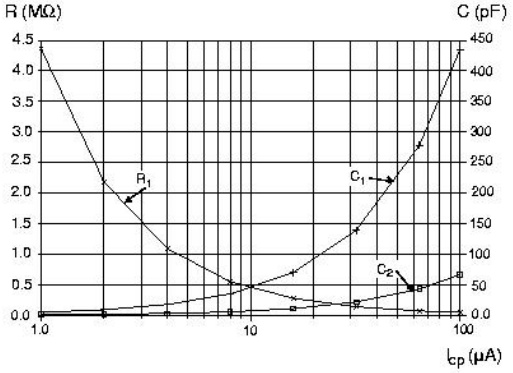

Figure 13. Loop filter component values as a function of charge pump current, for a 20 kHz open-loop bandwidth.

This reflects an SNR of $20\log(115kHz/5kHz) = 27dB$, good enough to meet the overall 18 dB SNR requirements of Bluetooth. At offset frequencies of 1 MHz and higher the spectral purity is determined by the free-running VCO phase noise performance.

The VCO of section 3.1 will be used, together with optimised frequency dividers. Figure 14 shows the die, occupying 1 mm^2 area in a 0.18 µm CMOS technology.

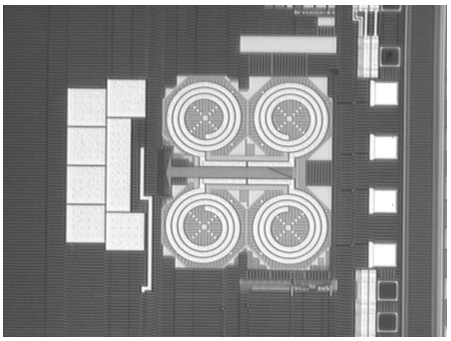

Figure 14. Die microphotograph of the synthesizer.

The complete synthesizer draws 8.2 mA from a 1.8 V voltage supply, resulting in a 15 mW power consumption. This extreme low power is achieved due to optimisation at all levels of hierarchy of the design. Figure 15 shows the phase noise for the in-phase output of the locked VCO, meeting the Bluetooth requirements. The phase noise at 3 MHz offset is below –120 dBc/Hz. The quadrature output has a similar phase noise characteristic. The closed-loop bandwidth is 20 kHz.

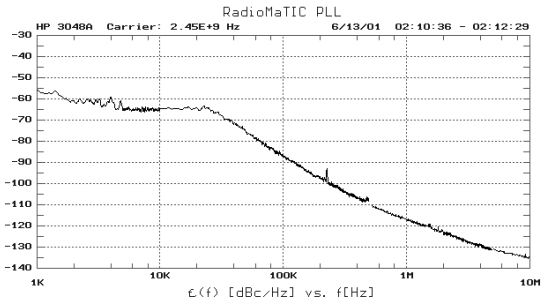

Figure 15. Measured phase noise of the in-phase output of the VCO.

5. Low power Bluetooth receiver

As already being mentioned, the Bluetooth standard is seen as the first wireless communication standard allowing System-on-Chip functionality. Several publications have demonstrated that large parts of the RF functionality and even the combination with the digital base band circuitry can be integrated in a single chip CMOS technology. Low power design is mandatory when the system is embedded with the mobile phone or other portable applications like the headphone set.

To achieve low power solutions, (near) zero-IF concepts are preferred above heterodyne architectures. The latter architecture uses often external IF filters, which demand proper impedance matching and hence cost additional power dissipation. Figure 16 shows a possible Bluetooth near zero-IF receiver, with an IF at 500 kHz. The receiver features the LNA from section 3.3 as well as the synthesizer from section 4. To improve I-to-Q leakage, two LNA's in combination with passive mixers have been used, instead of one LNA with Gilbert-type down mixers. For this application the latter option consumes more power. There are no external components except the crystal frequency. No IF filtering and AGC has been implemented to reduce even further the current consumption. A dedicated low power quadrature sigma-delta ADC has been used to perform digitization and channel filtering [11].

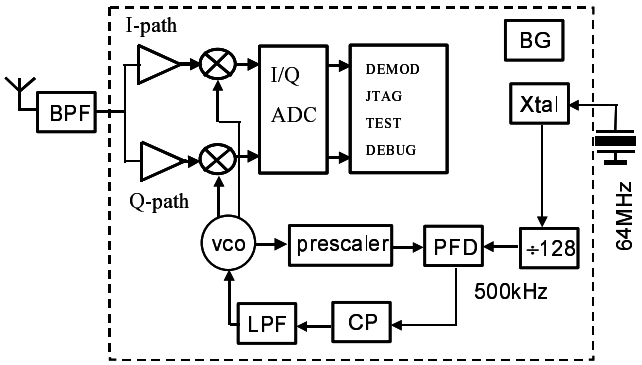

Figure 16. RF radio architecture for Bluetooth.

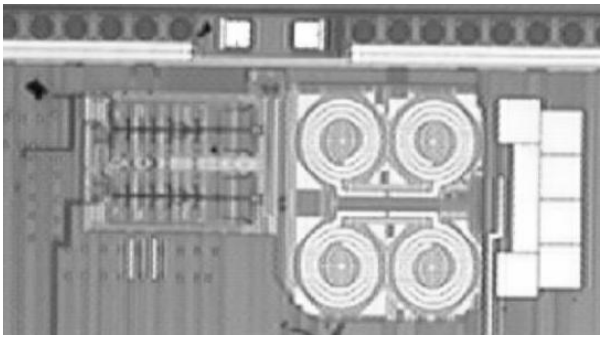

Figure 17. Die microphotograph of Figure 16. On left side the ADC, on top the LNA's and mixers.

The radio has been implemented in 0.18 µm CMOS technology and occupies 3.5 mm^2. The complete radio consumes 20 mW from 1.8 V supply voltage.

6. Conclusions

We have discussed several issues related to low power RF IC design. It is clear that real low power radios can only be obtained when taken every design step into account, starting from the most suitable technology, over proper architectural choices down to the best circuit design choices and layout issues.

7. ACKNOWLEDGMENTS

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