Elements of Low Power Design for Integrated Systems

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ABSTRACT

The increasing prominence of portable systems and the need to limit power consumption and hence, heat dissipation in very high density VLSI chips have led to rapid and innovative developments in low power design recently. Leakage control is becoming critically important for deep sub-100nm technologies due to the scaling down of threshold voltage and gate oxide thickness of transistors. In this paper, we discuss major sources of power dissipation in VLSI systems, and various low power design techniques on the technology and circuit level, logic level, and system level.

Categories and Subject Descriptors

B.7.0 **[Integrated Circuits]:** General.
B.7.0 **[Integrated Circuits]:** Types and design styles.

General Terms

Design, Performance.

Keywords

CMOS VLSI, Low Power Integrated Circuits.

1. INTRODUCTION

The PDA (Personal Digital Assistant) application of SOC (System on Chip) will substantially exceed the low power requirements of portable devices in the near future, according to the International Technology Roadmap for Semiconductors [1]. The limited battery lifetime typically imposes very strict demands on the overall power consumption of the portable systems. Revolutionary increase of the battery capacity is not expected in the near future. Therefore, reducing the power dissipation of integrated circuits through design improvement is a major challenge in portable system design. Modern microprocessors are running at clock frequency in the GHz range with 100W power dissipation [2]. Since the dissipated heat must be removed effectively to keep the chip temperature at an acceptable level, the cost of packaging, cooling and heat removal becomes a significant factor. Reliability is another concern, which points to the need for low power design. There is a close correlation between the peak power dissipation of digital circuits and reliability problems such as electromigration and hot-carrier induced device degradation [2]. Also, the thermal stress caused by heat dissipation on a chip is a major reliability concern. The methodologies which are used to achieve low power consumption in digital systems span a wide range from device level to system level. Low power techniques at different levels can be employed together to reduce power consumption.

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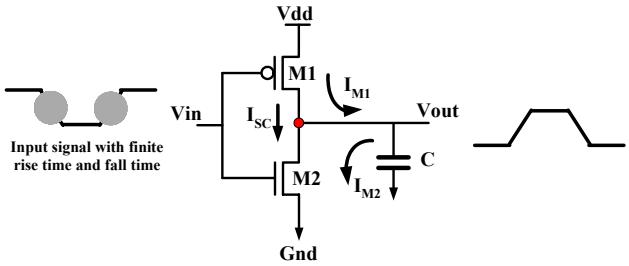

Figure 1. CMOS inverter for power analysis

The rest of this paper is organized as follows. Section 2 evaluates sources and mechanisms of power dissipation. Section 3 reviews low power design techniques at the technology and circuit level. Section 4 reviews low power design techniques at the logic level. Section 5 reviews low power design techniques at the system level, followed by a summary in Section 6.

2. BASIC PRINCIPLES

There are three major sources of power dissipation in a CMOS circuit [3]:

$$P_{total} = P_{switching} + P_{SC} + P_{leakage} \quad (1)$$

P_{total} is the total power dissipation of a CMOS circuit, $P_{switching}$ is the switching power, P_{SC} is the short circuit power, and $P_{leakage}$ is the leakage power. The switching power is the result of charging and discharging parasitic capacitances in the circuit [4]. It can be expressed as:

$$P_{switching} = \alpha C V_{dd} \Delta V f_{CLK} \quad (2)$$

where α is the node transition factor, which is the effective number of power-consuming voltage transitions experienced per clock cycle [2]. C is the output node capacitance, V_{dd} is the power supply voltage, ΔV is the voltage swing, and f_{CLK} is the clock frequency. Consider the inverter circuit in Figure 1. When input signal changes from high to low, the output node voltage makes a full transition from 0 to V_{dd} and one half of the energy drawn from the power supply is dissipated as heat in the conducting PMOS M1. When the input signal changes from low to high, the energy stored in the output node capacitance is dissipated as heat in the conducting NMOS M2. Short circuit power is due to the finite rise time and fall time of the input

signal as shown in Figure 1. When the input signal is between Vt_N and V_{dd}-$|Vt\_P|$, where Vt_N is the threshold voltage of M2 and Vt_P is the threshold voltage of M1, both M1 and M2 are turned on, and there is a short circuit current flowing from V_{dd} to ground. Short circuit power can be expressed as:

$$P_{SC} = I_{SC} V_{dd} \quad (3)$$

where I_{SC} is the short circuit current. The short circuit power can be kept less than 15% of the switching power with careful design [4, 5].

The reduction of the power supply voltage is one of the most effective ways to achieve low power design. This can be done at the circuit level using multiple V_{dd}, or it can be done at the system level using dynamic Vdd control according to system workload. The reduction of node transition factor α requires a detailed analysis of signal transition probabilities, and the use of various circuit level and system level techniques such as logic optimization, the use of a gated clock, and the prevention of glitches. The load capacitance can be reduced at the circuit level with novel circuit design or transistor sizing. The total switched load capacitance can also be reduced at the system level by clock gating or stopping certain units from useless transitions. The voltage swing ΔV can be reduced at circuit level using novel circuits. The clock frequency f_{CLK} can be reduced at the logic and architecture level by using parallel architecture to achieve the same throughput at lower clock frequency.

The leakage power can be expressed as:

$$P_{leakage} = I_{leakage} V_{dd} \quad (4)$$

where $I_{leakage}$ is the total leakage current in a CMOS circuit. $I_{leakage}$ is caused by six short channel leakage mechanisms [6]: the reverse bias pn junction leakage, subthreshold leakage, oxide tunneling current, gate current due to hot carrier injection, gate induced drain leakage, and the channel punchthrough current. Whereas scaling down of supply voltage is the most effective way to reduce power consumption, the threshold voltages of transistors also need to be scaled down to meet performance requirement. However, the lowering of the transistor threshold voltage leads to the exponential growth of the subthreshold leakage current, and the subthreshold leakage is the dominant leakage mechanism for now. As CMOS process advances to the sub-100nm regime, the gate oxide thickness of sub-20 Å prevails in CMOS processes [1]. Gate leakage may become the dominant factor for sub-100nm generations unless new solutions emerge [7].

3. TECHNOLOGY AND CIRCUIT LEVEL LOW POWER DESIGN

3.1 Leakage Control

Various circuit techniques have been developed to solve the subthreshold leakage and gate leakage problems. All these techniques decreases $I_{leakage}$ in Equation (4).

3.1.1 Subthreshold Leakage Control

3.1.1.1 MOS Threshold Voltage Control Methods

MTCMOS (Multi-Threshold CMOS) [8] circuits use two different threshold voltages for transistors in a single chip. Low threshold voltage transistors are used to improve the performance in active mode while high threshold voltage transistors are used to suppress subthreshold leakage in standby mode. MTCMOS could not be used for very low power supply voltage because the high threshold voltage transistors could not be turned on. The sizes of high threshold voltage transistors also need to be carefully sized to meet performance requirement.

Different substrate bias voltages are applied by a self substrate bias generator in VTCMOS (Variable Threshold CMOS) [9] technology. Low threshold voltage is obtained in active mode for high performance while high threshold voltage is obtained in standby mode to suppress leakage. VTCMOS requires a large voltage to change the threshold voltage by several hundred mV since the threshold voltage changes depending on the square root of the source to substrate voltage.

In DTCMOS (Dynamic Threshold Voltage MOSFET) [10], the threshold voltages are changed dynamically according to the operating state of the circuit. Even though this technique could possibly lower the supply voltage further, it uses SOI technology and suffers from increased leakage current due to inherent forward bias current for pn-junctions [11].

3.1.1.2 Gate Voltage Control Methods

SCCMOS (Supper Cut-Off CMOS) [11], Gate-Over-Driving CMOS [12], and MVCMOS (Multi-Voltage CMOS) [13] employ an on-chip boost voltage for the sleep control signal. In the standby mode, the sleep control signal is increased to about 1.5 times of power supply voltage. So the sleep PMOS transistor is reverse biased, thus leakage current could be suppressed. This method requires N-well separation and a high efficient on-chip boost voltage generator, which is hard to achieve in sub-1V region. Oxide reliability could be another issue.

3.1.1.3 Transistor Stacking Methods

For the input vector activation method [14], the standby control signal is derived from the clock gating signal and it is used to generate and store a predetermined vector in the static input latches of the circuit during standby mode so as to maximize the number of NMOS and PMOS stacks with more than one off device. Intensive simulation has to be done to determine the desired input vector and additional circuits are needed to store the desired input vector.

The stacking transistor insertion technique [15] first identifies a circuit input vector that will put most of the circuit into a low leakage state. Then, for each gate in a high leakage state, they insert a leakage control transistor between the power supply and the pull up network or between the ground and the pull down network.This method also needs intensive simulation for the desired input vector and additional latches.

For stack forcing technique [16], tradeoff between standby current and performance can be made by forcing one transistor into a two transistors stack with the same load for input. Pre-determined input vector is also required.

3.1.2 Gate Leakage Control

Inukai et al. proposed a device/circuit cooperation scheme, called boosted gate MOS (BGMOS) [17]. Low Vt transistors with thin T_{ox} are used for the core circuit, while transistors with higher Vt and thicker T_{ox} are used as low leakage switches to suppress the subthreshold leakage and gate leakage in sleep mode. A boosted gate voltage is applied to transistors with higher Vt and thicker T_{ox} to reduce the area penalty. This

scheme requires dual supply voltages and a complicated fabrication process to achieve dual T_{ox}.

Hamzaoglu et al. proposed a P-type Domino [18], which uses PMOS transistors in the logic tree instead of NMOS transistors. It is based on the fact that, under inversion bias, gate leakage through SiO_2 for PMOS transistors is an order of magnitude lower than that of NMOS transistors [19]. On the other hand, the PMOS transistors in the logic tree of a P-type Domino have to be up sized to achieve the same performance as N-type Domino, due to lower mobility. This increases the area and active power consumption. High fan-in Domino gates are often employed in performance critical units of microprocessors and other high performance VLSI circuits [20]. The OR function is performed by parallel connected NMOS transistors for the N-type Domino, while it is performed by serial connected PMOS transistors for the P-type Domino. The P-type Domino, however, may lose its advantage for high fan-in dynamic gates used for high performance.

3.1.3 Leakage-Proof Domino Circuit Design

Dual Vt techniques have been used for Domino circuits to suppress the subthreshold leakage [21]. Figure 2 shows the dual Vt implementation of a Domino OR gate.

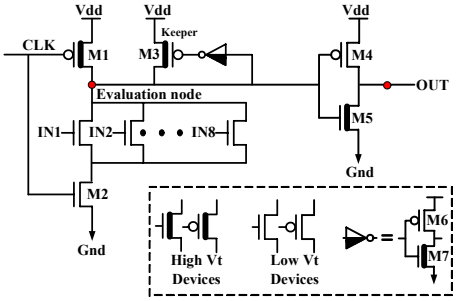

Figure 2. Dual Vt 8-input Domino OR gate

High Vt devices are in the non-critical path of a Domino circuit as shown in Figure 2. In standby mode, the clock signal and inputs to the Domino circuit should be high so that the high Vt devices are turned off to suppress the subthreshold leakage [21, 22]. Although subthreshold leakage current is reduced by high Vt devices in dual Vt Domino circuits, their gate leakage is not. Simulation based on 45nm BSIM4 models shows that standby gate leakage is about two orders of magnitude larger than the subthreshold leakage in a dual Vt Domino circuit at the 45nm node [23]. Simulation also shows that gate leakage of an NMOS transistor is about 34 times that of a PMOS transistor with the same width under a 0.8V power supply. The gate leakage of Domino circuits mainly comes from the NMOS logic tree.

In conventional Domino logic, inputs and outputs of every Domino stage are set high in standby mode to turn off the high Vt devices. The gate of the transistors in the NMOS logic tree is high, while the source and drain nodes of those transistors are low, gate-to-drain and gate-to-source tunneling currents flow in those NMOS transistors in standby mode as shown in Figure 3(a). If we can achieve the condition that gate, drain and source of the transistors in the NMOS logic tree are all low as shown in Figure 3(b), there will be no gate leakage in the NMOS logic tree. Thus, for gate leakage suppression, inputs and outputs of every Domino stage in a Domino stage chain should be low in standby mode, while high Vt devices also need to be turned off to suppress subthreshold leakage.

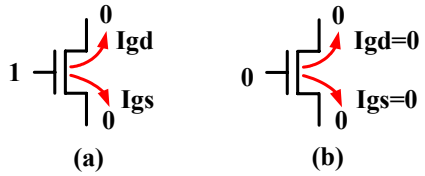

Figure 3. (a) Standby gate leakage in NMOS logic transistors of dual Vt domino. (b) Desirable condition

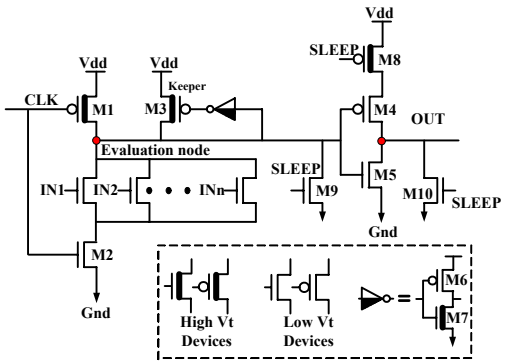

Figure 4. Proposed circuit

A new leakage-proof Domino circuit to reduce both the subthreshold leakage and the gate leakage is shown in Figure 4 [24]. In operation mode, SLEEP is low. M9 and M10 are off and M8 is on. This circuit works like the conventional dual Vt Domino. In standby mode, CLK and SLEEP are high, and all inputs to the Domino circuit are low. M1 and M8 are turned off by CLK and SLEEP. NMOS sleep transistor M9 is turned on by high SLEEP. It discharges the dynamic node to ground so that high Vt devices M3 and M7 are turned off. All potential subthreshold leakage paths are then suppressed by turned off high Vt devices M1, M3, M7 and M8.

The gate, drain, and source nodes of the NMOS transistors in the NMOS logic tree are all set low as shown in Figure 3(b). Thus, there is no gate leakage in the NMOS logic tree. The NMOS sleep transistor M10 is turned on by high SLEEP to discharge the Domino circuit output so that inputs to the next stage Domino circuits are low. Simulation results for 32-bit adders show that an adder using the proposed Domino circuits can reduce the standby gate leakage by 67%, compared to an adder using conventional dual Vt Domino circuits. 45nm BSIM4 models [23] were used in our simulation and the power supply was 0.8V.

3.1.3 Leakage-Proof SRAM Cell Design

As deep-submicron CMOS technology advances, on-chip cache has become a bottleneck on microprocessor's performance. Meanwhile, it also occupies a big percentage of processor area and consumes large power. Various SRAM designs have been proposed [25, 26, 27]. They were targeted at either power, delay, or leakage, and none of them are compromise oriented.

With a Multi-Criteria Decision Making strategy [28], new SRAM design with a special attention to leakage currents has been achieved [29]. The design process can be formulated such that the leakage current is minimized under constraints such as power and delay.

3.2 Switching Power Reduction

3.2.1 Low Power Flip-flop Design

In many VLSI chips, the power dissipation of the clocking system, including the clock distribution network and flip-flops, is often the largest portion of the total chip power consumption. The design trend is to use more pipeline stages for high throughput, which increases the number of flip-flops in a chip. Thus, it is important to reduce power consumption in both the clock trees and the flip-flops. Several small-swing clocking schemes have been proposed and their potential for practical applications has been shown [30, 31]. The previous half swing scheme requires four clock signals. It suffers from skew problems among the four clock signals and requires additional chip area [31]. A reduced clock-swing flip-flop (RCSFF) requires an additional high power-supply voltage to reduce the leakage current [30]. A single-clock flip-flop for half-swing clocking does not need high power-supply voltage but has a long latency [32]. The hybrid-latch flip-flop (HLFF) and semi-dynamic flip-flop (SDFF) have been known as the fastest flip-flops, but they consume large amounts of power due to redundant transitions at internal nodes [33, 34, 35]. To reduce the redundant power consumption in internal nodes of high-performance flip-flops, the conditional capture flip-flop (CCFF) has been proposed [36]. However, HLFF, SDFF, and CCFF use full-swing clock signals that cause significant power consumption in the clock tree.

A low-swing clock double-edge triggered flip-flop (LSDFF) [37] has been developed to reduce power consumption significantly compared to conventional flip-flops. The schematic of LSDFF is shown in Figure 5. Figure 6(a) shows the concept of the proposed clocking scheme, and Figure 6(b) shows equivalent implementation methods. For LSDFF, with a simple clocking scheme, double-edge triggering can be implemented to sample and transit data at both the rising edge and the falling edge of the clock. Hence, the clock frequency can be lowered to half and accordingly the clock network power consumption can be reduced by 50%. To prevent performance degradation of LSDFF due to low-swing clock, low-Vt transistors are used for the clocked transistors without significant leakage current problem. The power saving in flip-flop operation is estimated to be 28.6 to 49.6% with additional 78% power saving in clock network. LSDFF reduces the switching power dissipation by decreasing ΔV and f_{CLK} in Equation (2).

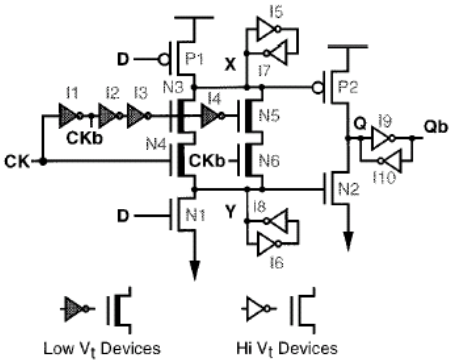

Figure 5. Schematic of LSDFF

3.2.2 Low Power Domino Design

High-speed Domino logic is now prevailing in the performance-critical block of a chip. However, Domino logic may be less power effective compared to static logic due to significant clock loading and high switching activity. Since switching power is quadratically proportional to the supply voltage, dual supply voltage techniques have been proposed for static logic, which use high supply voltage (V_{ddH}) in the critical path to obtain high performance while using low supply voltage (V_{ddL}) in the non-critical path to reduce power consumption [38, 39]. Dual supply voltage technique for Domino logic was proposed [40]. However, this technique does not consider reducing power consumption in the clock tree. It uses V_{ddH} for the clock tree.

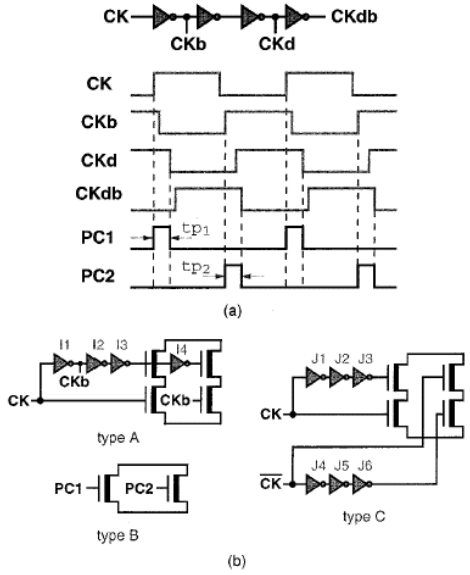

Figure 6. (a) Clock timing diagram of LSDFF. (b) Three shot pulse generation methods

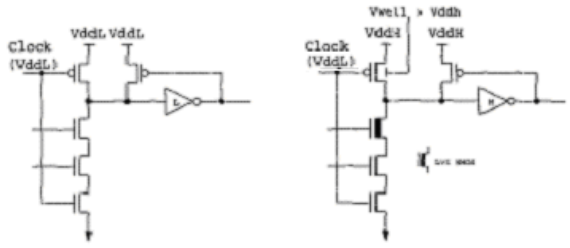

Figure 7. Low Voltage Swing Clock (LVSC) in dual supply voltage technique for Domino logic

To reduce the power consumption in the clock tree, the clock can share the supply voltage with logic gates such that a high voltage swing clock is used for high V_{dd} Domino logic gates, while a low voltage swing clock is used for low V_{dd} Domino logic gates. This clock scheme referred to as Dual Voltage Swing Clock (DVSC). In this scheme, two clock trees are required. It complicates the routing, and thus increase the effective load capacitance of the clock tree. To further reduce the power consumption in the clock tree, Low Voltage Swing Clock (LVSC) scheme [41] has been developed. Low voltage swing clock controls all domino logic gates regardless of supply voltage level of Domino logic gate as shown in Figure 7. Since low voltage swing clock controls the PMOS precharge transistor in a V_{ddH} logic gate as shown in Figure 7, PMOS cannot completely turn off. As a result, DC current flows through the PMOS transistor. To solve this problem by increasing V_t of the PMOS precharge

transistor, the well of the transistor is biased with higher voltage than V_{ddH}. The evaluation time of a Domino gate using V_{ddH}, which is in the critical path, can be degraded due to the low voltage swing clock. To compensate for such performance degradation, low V_t is applied to the NMOS transistors in the critical path. Simulation results of ISCAS85 benchmark circuits based on 0.18um CMOS process show that dynamic power saving ranges from 13% to 36%. LVSC Domino reduces the switching power dissipation by decreasing ΔV in Equation (2).

4. LOGIC LEVEL LOW POWER DESIGN

Logic level low power design has been intensively studied [42]. Path equalization is an effective technique, where a logic network can be transformed to minimize power under the condition that the critical path is not lengthened. This effectively decreases node transition factor α in Equation (2). When signal paths are equalized, most gates have aligned transitions at their inputs, thereby minimizing spurious switching activities [43]. This method is good for arithmetic circuits, such as adders. For glue logic and controllers that have a wide range of delays, gate re-sizing can be used to equalize the delay of fast paths to the delay of critical path. This helps to reduce the switched capacitance C in Equation (2).

Other logic level power minimization techniques such as re-factoring, re-mapping, phase assignment, and pin swapping are local transformations [43]. They are used to reduce capacitance C and node transition factor α in Equation (2).

The precomputation method [44] adds a simple combinational circuit, which is the precomputation logic to the original circuit. The basic idea is to selectively precompute the output logic values of the circuits one clock cycle before they are required, and then use the precomputed values to reduce internal switching activity by stopping certain unites in the circuit in the succeeding clock cycle. This reduces capacitance C and node transition factor α in Equation (2).

5.SYSTEM LEVEL LOW POWER DESIGN

System level dynamic power management (DPM) is a design methodology that dynamically reconfigures an electronic system to provide the requested services and performances with a minimum number of active components or a minimum load on such components [45].

The power dissipation of the clocked components in a system is often the largest portion of the total chip power consumption. Clock gating is an effective way to reduce the switching power by reducing capacitance C in Equation (2). The Alpha 21264 microprocessor [46] uses a hierarchical clocking scheme with gated clocks. The clock signals to some arithmetic circuits are gated according to the instructions to be executed. So, there is no clock power wasted in idle components.

Supply shutdown of idle components can reduce both switching power and leakage power with the disadvantage of long recovery wake-up time due to the large time constant of the power supply line. During the sleep state of the StrongARM SA-1100 chip [47], the power supply of the CPU core and the majority of the functional units are shutdown to save power.

Multiple and Variable power supplies can be used for components that are not idle, but have varying performance with time. Usami et al. employed a multiple power supply in their work [48], and Nielsen et al. used variable supply voltage [49].

The PowerWise [50] technology of National Semiconductor uses adaptive voltage scaling in a closed loop manner, which relies on an embedded Adaptive Power Controller (APC) that tracks the performance variations of the system processor. The power management unit then adaptively adjusts the supply voltage of the system processor based on performance requirements.

The above system level power supply control methods reduce power consumption by reduce V_{dd} in Equation (2) and (4).

Recently, it was demonstrated that an interesting combination of an array of single electron transistors and CMOS circuits (CMOS-SET) could be effectively used for low power system design [51].

SUMMARY

In this paper, we have reviewed low power design techniques at technology and circuit, logic, and system levels. These techniques are geared to reduce the node transition factor α, the node capacitance C, power supply voltage V_{dd}, voltage swing ΔV, clock frequency f_{CLK}, and leakage currents. The use of high dielectric gate materials may help contain the gate leakage problem. Novel system level design, such as the PowerWise and CMOS-SET hybrid system can significantly reduce the overall power consumption.

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