Integrated DC-DC Converter Design for Improved WCDMA Power Amplifier Efficiency in SiGe BiCMOS Technology

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ABSTRACT
We present a DC-DC converter design for on-chip integration with a WCDMA power amplifier to provide supply voltage modulation and efficiency enhancement. It operates from a 3.3V supply using 0.35µm 'high-breakdown' CMOS transistors available in IBM's SiGe BiCMOS 6HP process. Five selectable output voltage levels are available ranging from 1.3V to 3.3V. The converter is optimized for operation at 88.7MHz. Simulation results show an average efficiency of 78.8% over power amplifier operating conditions and a peak enabled efficiency of 86%. CCM-DCM mode switching and transistor width switching are used to minimize losses at the different output voltage and current load levels.

Categories and Subject Descriptors
B.7.1 [**Integrated Circuits**]: Types and Design Styles – *VLSI (very large scale integration)*.

General Terms: Design.

Keywords: DC-DC Converter, Power Amplifier, Efficiency, W-Switching, CCM-DCM, WCDMA.

1. INTRODUCTION
Power Amplifier (PA) efficiency is a key limiter of wireless device battery lifetime. Typical wireless device power amplifiers provide efficiencies on the order of 30-40% at maximum power output levels; however they do not operate at these levels the vast majority of the time and as such their average efficiency is much lower, as shown in Figure 1. Since the full supply voltage is not required for lower RF power output levels, it has been shown that this average efficiency (and hence battery lifetime) can be dramatically improved by decreasing the supply voltage of the PA when large output power levels are not required, decreasing the DC power draw [3, 6].

Therefore, by integrating a DC-DC converter to vary PA supply voltage as the required output power varies, overall system efficiency can be improved and hence battery life can be extended. DC-DC converters will be essential in future low power wireless systems, to increase transmitter efficiency and improve battery life.

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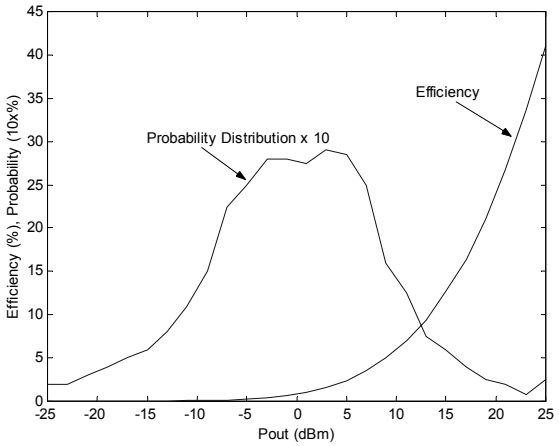

Figure 1. Typical PA efficiency and P_{out} probability distribution, based on [3,6]

To the best of our knowledge, this concept has not been demonstrated with the power converter integrated on-chip with the power amplifier. The development of this converter is intended for single chip integration with a WCDMA power amplifier using IBM's SiGe BiCMOS 6HP process.

2. DESIGN REQUIREMENTS
Detailed converter specifications were derived from PA performance simulations, as outlined in Table 1. To optimize performance five discrete output voltage states were chosen. Converter output current ranges in each state are also provided. These current levels were represented by an average load resistance in all calculations and simulations.

Table 1. Required converter output characteristics

	I_{out}		P_{out}		
V_{out}(V)	I_{min}(mA)	I_{max}(mA)	P_{min}(mW)	P_{max}(mW)	R_{load}(avg) Ω
3.3	190	250	625	825	15
2.8	150	180	420	505	17
2.3	115	150	265	345	17.4
1.8	80	115	145	205	18.5
1.3	50	80	65	105	20

3. DESIGN METHODOLOGY

3.1 Topology Selection

A number of topologies were considered to satisfy the step-down converter requirements set by the PA. A synchronous rectifier (SR) based buck converter topology was chosen due to its simplicity, efficiency and ability to provide large output power levels. The basic circuit topology is shown in Figure 2. Using an n-channel MOSFET as a SR switch instead of a diode rectifier, and controlling it to turn on when a typical diode would, the series resistance associated with conduction can be decreased resulting in a reduction in conduction losses [4].

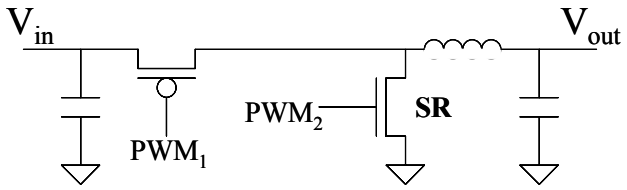

Figure 2. Buck SR converter topology

3.2 Switching Frequency Selection

In a Buck SR switching converter the switching frequency for the pulse-width modulated (PWM) MOSFET drive signals shown in Figure 2 must be carefully selected. The factors affecting the choice of this frequency are:

(1) The required size of the passive components (inversely proportional to frequency)

(2) Unwanted in-band interference that may result from switching harmonics

(3) Switching and gate charge/discharge losses (proportional to frequency)

Therefore, there is a perceived trade-off in selecting the converter switching frequency: higher frequencies result in smaller passives, which improve integration density, but they also result in greater switching losses.

The switching frequency should also be selected such that the harmonics fall outside the transmit band of the PA (e.g. 1920-1980MHz for WCDMA applications [7]) and such that the output voltage ripple mixing with the transmitted signal does not produce any products that may also fall within the transmit band. For the target application, this requires a switching frequency greater than 60MHz. It can be shown that for a PWM signal of any duty cycle, only odd harmonic components exist. As such, analysis was performed to determine the size and location of frequency windows greater than 60MHz that exclude odd harmonics that would fall in the transmit band. The results of this analysis are shown in Figure 3, where a value of one (1) corresponds to an available frequency range and a zero (0) corresponds to a range where odd harmonics would fall in the transmit band.

It can be ascertained from Figure 3 that the higher the frequency the wider the available bands, decreasing oscillator tolerance requirements. However, higher frequencies also produce greater switching losses. Therefore, the 5.2MHz band from 86.1MHz to 91.3MHz was chosen as a compromise between these requirements (11.3ns nominal period). This frequency also yields reasonably small passive components (in the nH and nF ranges).

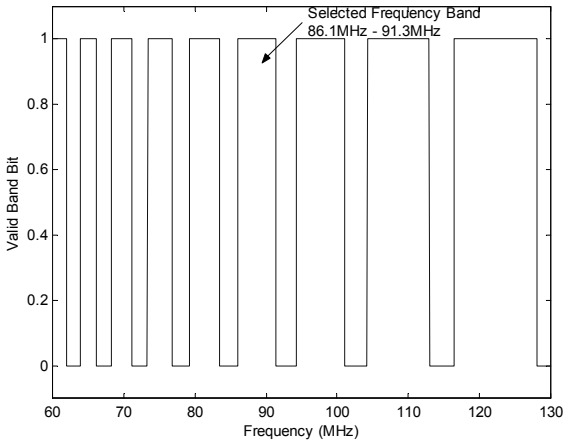

Figure 3. Frequency bands available for switching with no transmit band harmonics

3.3 Active Device Sizing

When sizing the power transistors, it has been shown that to minimize losses the transistor size and switching frequency should be selected such that the switching losses (from charging and discharging the MOSFET gates) match conduction losses [11]. Hence, some have suggested decreasing the switching frequency at low load currents to maintain optimum efficiency [14]. However, in this application the PWM frequency must be fixed to avoid in-band harmonics (and simplify control), so the frequency cannot be varied to match the switching losses to the large variations in conduction losses that result from the wide range of load currents. To solve this problem the size of the power transistors (the effective device width) is switched with load current to provide optimum efficiency at different load conditions, as suggested by Williams et al in [12], using a technique called 'W-switching'. In this way, when the load current decreases the power transistor can be made smaller, thereby decreasing gate charge/discharge losses. Although this does increase conduction losses overall losses can still be decreased. By redistributing losses in this way overall losses can be minimized and higher overall efficiency can be achieved.

3.4 Passive Component Selection

It is desirable to integrate the converter passives on-chip as well, to simplify packaging. In fact, the final inductor value (9.1nH) is small enough to be integrated on-chip. Unfortunately, the series resistance of on-chip inductors (1-2 Ω) is far too large for a power converter application. The losses (and voltage drop) associated with an on-chip inductor would make the efficiency too low (and the output voltage too variable with load current) for practical use. As a result, the output inductor and capacitor are implemented off-chip. This does, however, provide the advantage of connecting the converter output directly to an off-chip choke inductor for the PA output stage, which provides higher PA efficiency than an on-chip choke inductor.

3.5 PWM Signal Characteristics

Inductor series resistance can usually be considered approximately proportional to the inductance value for a given inductor implementation. As such, smaller inductors will have lower series resistance and produce less loss, so a small inductor value is desirable. The disadvantage of using smaller inductors is that at low load currents the inductor current will go negative each cycle, resulting in increased losses as some of the output capacitor charge is shunted to ground through the SR. One way to solve this problem is to turn off the SR when the current through the inductor goes to zero so that the charge is not lost to ground but rather charges up the node common to the SR, inductor and PFET. This mode of operation is known as the discontinuous conduction mode (DCM) and has been shown to significantly improve low load current efficiency relative to continuous conduction mode (CCM) designs [13]. DCM operation is used in this converter at lower load current levels, while CCM is used at higher load currents.

Through the use of W-switching and DCM operation, the converter efficiency at the minimum output current level increased by 20% (from 44% to 64%) and the average converter efficiency over all operating conditions increased by almost 12%.

4. DETAILED DESIGN

The five states listed in Table 1 represent four step-down switching states and a 'disabled' state where the PFET is always on and the power supply is coupled directly to the PA through the PFET and the converter's off-chip inductor. The converter requires two state input bits (S1 and S0 as defined in Table 2) to define four enabled V_{out} states. The state bits are used for W-switching purposes. Along with the two state bits, the control circuitry also generates the two PWMs (one each for the PFET and SR NFET) to correlate with the state bits. When the converter is disabled, all PWMs and state bits are grounded such that the maximum PFET width is on, minimizing series resistance (Rds(on)).

Based on the work of Stratakos et al [11], attempts were made to match the conduction losses to the switching losses to minimize overall losses. The matching was traded off with the desire to make W-switching increments constant to simplify layout. The resulting transistor widths in each output voltage state are listed in Table 2. The width-switching increment was selected to be 100µm for the PFET and 40µm for the NFET. Minimum length high breakdown devices were used for all transistors (L_p=0.34µm, L_n=0.40µm).

The PWMs were optimized to generate the proper output voltage, and limit losses by using DCM operation in the lower current load states and also by providing a dead time between PFET turn-off and NFET turn-on (break-before-make). This dead-time is the maximum tolerable fixed delay between the waveform rising edges, while still avoiding body diode conduction in the SR [5]. The PWM characteristics are illustrated in Figure 4. The PWM pulse widths are listed in Table 2.

Table 2. State characteristics for the pre-defined output voltage levels

V_{out} (V)	S1	S0	W_p (µm)	W_n (µm)	P1 (ns)	P2 (ns)	D (ns)
3.3V	0	0	700	280	N/A	N/A	N/A
2.8V	0	0	700	280	1.4	1.0	0.3
2.3V	0	1	600	240	5.9	1.6	0.3
1.8V	1	0	500	200	8.0	2.0	0.3
1.3V	1	1	400	160	9.3	2.5	0.3

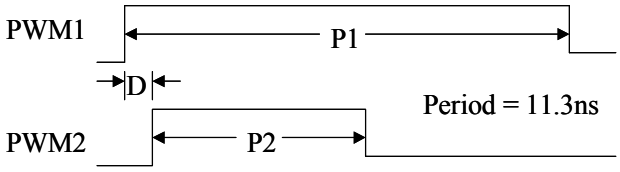

Figure 4. PWM signal characteristics

The inductor was sized to be as small as possible, while limiting the peak inductor current to acceptable levels (in this case <540mA from the inductor specification [9]). Small inductor size limits series resistance losses in the inductor, which are crucial to the overall converter efficiency. A 9.1nH inductor with 0.14Ω series resistance in an 0402 package was selected. A 1nH bond wire was also assumed in series from the chip to the external inductor. According to Amkor [2], a 1.2mil gold bond wire 1mm long will have this inductance and handle up to 850mA of current, so this is a reasonable assumption. This results in a series inductance of 10.1nH and a maximum inductor current of 462mA, which is less than 540mA, as desired.

Output voltage ripple is largely determined by the output filter capacitance. Since the output filter inductor is an off-chip 0402 size component, it is reasonable to use a similarly sized capacitor. As such, an 0402 sized 100nF capacitor was selected. This results in a voltage ripple of less than 0.5%.

5. CIRCUIT IMPLEMENTATION

The overall circuit is depicted in Figure 2, where the inductor and capacitor are off-chip components. To accomplish W-switching, seven identical converter blocks with an integrated enable are configured in parallel. The enable is set through the use of some simple static control logic that takes the state bits (S1, S0) as inputs. A single converter block is depicted in Figure 5.

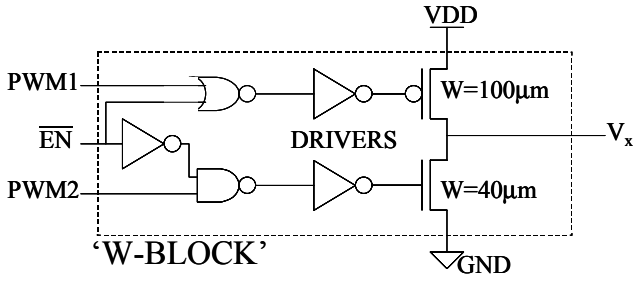

Figure 5. Single W-switching converter block (W_p=100µm, W_n=40µm)

The entire converter configuration is depicted in Figure 6, where the 'W-BLOCK' is the block defined in Figure 5.

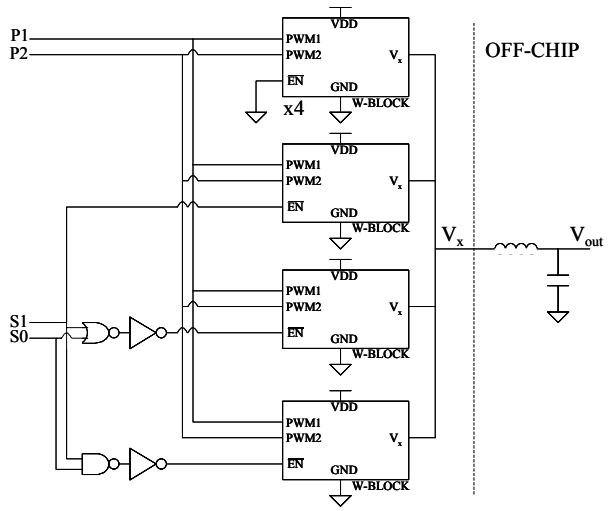

Figure 6. Complete converter configuration

6. SIMULATION RESULTS

Using the settings in Table 2, and the selected passives, the final simulated losses and efficiencies in each state are summarized in Table 3. These results were generated with the converter driven by the actual control circuit blocks, such that finite rise-time effects that will result from RC time constants in the circuitry and their effects on efficiency should be considered in the results.

Table 3. Efficiency and loss breakdown for DC-DC converter

V_{out} (V) Goal / Simulated	P_{out} (mW)	P_{in} (mW)	Efficiency (%)	Total Loss (mW)	Gate Charge Loss (mW)	Conduction Loss (mW)	R_{load} (Ω)
3.3 / 3.151	661.91	693.33	95.5 %	31.42	0	31.42 **(R = 0.71)**	15
2.8 / 2.794	459.20	533.60	86.1 %	74.40	43.04	31.36	17
2.3 / 2.299	303.76	383.46	79.2 %	79.70	36.35	43.35	17.4
1.8 / 1.804	175.91	241.30	72.9 %	65.39	30.38	35.01	18.5
1.3 / 1.355	91.80	142.23	64.5 %	50.43	24.13	26.30	20

Efficiency versus output current is plotted in Figure 7. The state jumps are clearly shown. The parabolic peaks in the efficiency in each range indicate that the converter operates at or near peak efficiency in each case.

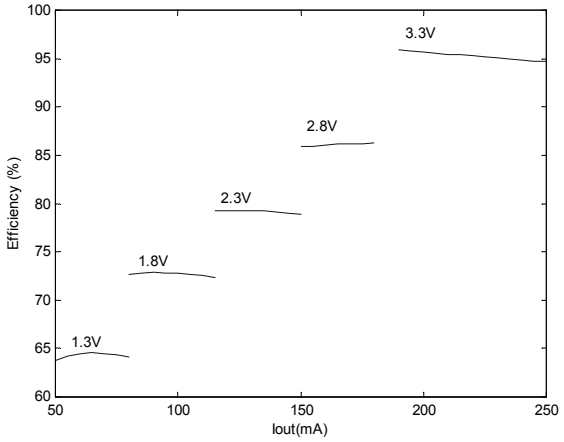

Figure 7. Efficiency versus output current

The overall characteristics of the implemented converter are summarized in Table 4. Average efficiency is calculated based on the probability of the PA transmitting at each output power level, as given in [3], and the converter state as a function of the PA's RF output power, which has been defined for the overall circuit architecture.

Table 4. Summary of DC-DC converter characteristics

Parameter	Value
Operating Frequency	88.7MHz
L (off-chip)	9.1nH
C (off-chip)	100nF
Die Size (without pads)	700µm x 215µm
Average Efficiency	78.8%
Output Voltage Ripple	< 0.5%

Figure 8 shows simulated waveforms for the V_{out}=1.8V case, including V_x, Inductor Current (I_L), V_{out}, PWM1 and PWM2. The other converter states produce similar waveforms.

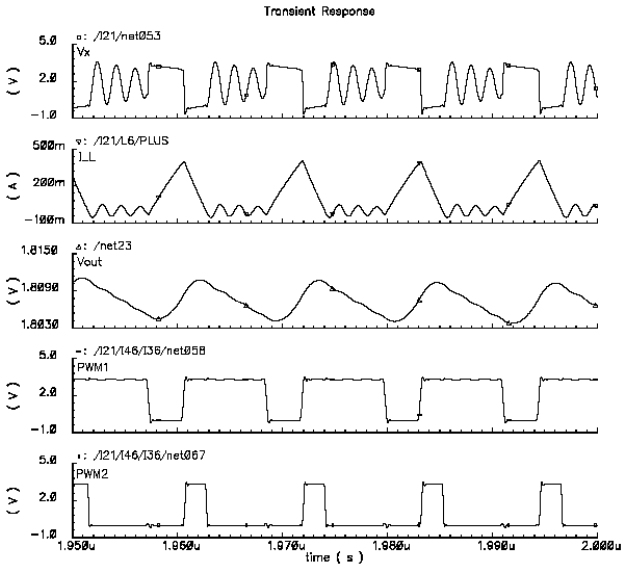

Figure 8. Simulated converter waveforms (V_{out} = 1.8V, R_{load} = 18.5Ω)

Simulations were also performed to evaluate the effects of changes in the load current, which was simulated by changing the load resistance. From Figure 9 it can be seen that over the range of expected currents at 1.8V, the output voltage was regulated within 5% and the response to the change in load current took less than 1µs to settle out.

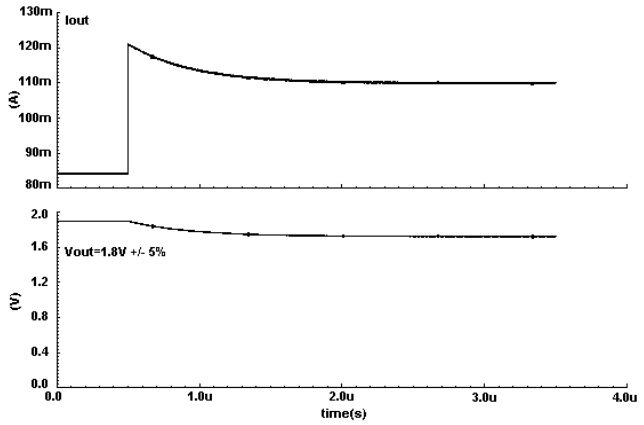

Figure 9. Output Voltage (1.8V state) as the load current changes form 85mA to 110mA

The time required to switch from one output voltage state to another was also evaluated via simulation. Such a state change is depicted in Figure 10, where the output voltage switches from 2.8V to 2.3V and the state bits S0 and S1 are also shown. The results show that a state change takes approximately 1μs to complete, which is acceptable considering the power update rate for 3G systems is between 800 and 1600 Hz [8].

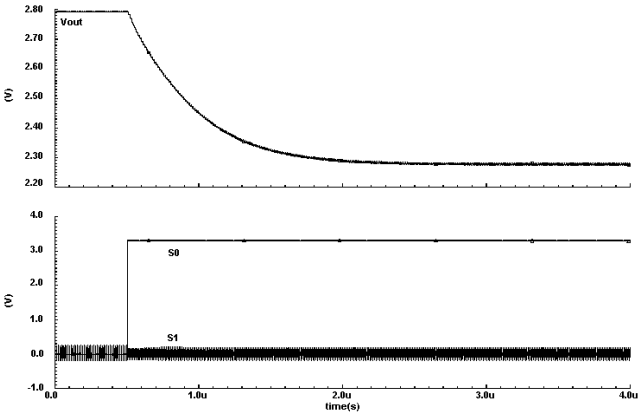

Figure 10. Output voltage transient response to a state change from 2.8V to 2.3V

7. LAYOUT

The complete converter layout is shown in Figure 11. It measures 700μm x 215μm within the pad frame. The small feature size of the MOSFETs used (0.35μm) allows for a small converter layout area with reasonable Rds(on) values for the power transistors.

The size of the switching nodes (e.g. V_x) was made large enough to satisfy electromigration and series resistance requirements, but not much larger, as these nodes are antennas and can generate unacceptable levels of radiated EMI if they are too large[10]. Therefore, there is a trade-off in the sizing of these nodes. Distributed drive circuitry has been used; laying out each of the seven 'W-BLOCK's separately to decrease RC delays which would slow the PWM edges and decrease efficiency, as pointed out by [1]. The seven 'W-BLOCK's can clearly be seen in the layout in Figure 11.

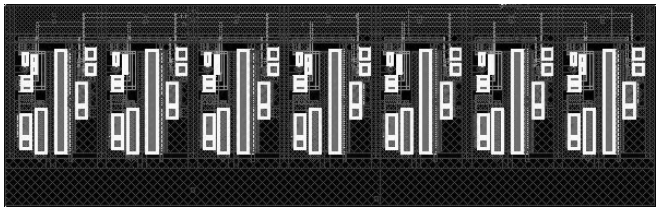

Figure 11. Complete converter layout (Vx at bottom; VDD, GND and control signals at top)

8. CONCLUSIONS

A DC-DC converter has been designed that can be monolithically integrated with a WCDMA power amplifier, which has been designed in a SiGe BiCMOS technology. A synchronous rectifier (SR) buck converter topology has been implemented using off-chip passives and operated at a nominal PWM period of 11.3ns. The converter provides five possible output voltages between 1.3V and 3.3V. Good overall efficiency is achieved through the use of CCM-DCM mode switching and power transistor width switching (W-switching) to optimize the converter efficiency at a fixed PWM frequency. The use of integrated converters of this type in future low power wireless systems will increase transmitter efficiency and improve battery life. Experimental results were not available before the paper deadline but will be provided as part of the oral presentation.

9. ACKNOWLEDGEMENTS

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