A 0.75-mW Analog Processor IC for Wireless Biosignal Monitor

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ABSTRACT
This work presents a single-channel analog processor IC for the wireless biosignal monitor. This chip occupies a small die area of 0.52 mm^2 and has a low power consumption of 0.75 mW at a 5-V supply voltage. The wired and wireless systems constructed by using the designed processor chip and commercial discrete ICs have been validated in this study. Experimental results indicate that the integrated single-chip processor system can amplify, filter, transmit, and receive the simulated ECG signal. Compared to the wired prototype system, wireless transmission provides better long-distance, long-term measuring, recording, and monitoring the biosignal.

Categories and Subject Descriptors
B.7.m [**Integrated Circuits**]: Miscellaneous

General Terms: design

Keywords
analog processor, IC, wireless, and biosignal monitor.

1. INTRODUCTION
As the integrated circuits (IC) industry develops, the design of the analog signal processing module on chip is becoming more important in biomedical instruments. The trend is to integrate all the analog front-end circuits in a single chip to minimize the chip area and improve the reliability of the system for biomedical applications [1] – [3]. Wireless data transmission represents the current trend in biomedical system applications for long-term, long-distance measuring, recording, and monitoring of biosignals [4]. The physiological signals input to a biomedical system, like ECG, EEG, EMG, or EOG signals, are very low amplitude and low frequency, as shown in Table I [5]. The performance of the system depends on amplifying, filtering, transmitting, and receiving ECG signals. Additionally, a analog processor IC is designed for this wireless biosignal monitoring system.

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Table 1. Medical and Physiological Parameters

Parameters	Principal measurement range	Signal frequency range	Standard method
Electrocardio-graphy (ECG)	0.5 – 4 mV	0.01 – 250 Hz	Skin electrodes
Electroencephalo-graphy (EEG)	5 – 300 μV	DC – 150 Hz	Scalp electrodes
Electromyography (EMG)	0.1 – 5 mV	DC – 10 kHz	Needle electrodes
Eye Potentials (EOG)	0.05 – 3.5 mV	DC – 50 Hz	Contact electrodes

Core analog building blocks, based on a closed-loop operational amplifier (OP) structure, have been developed successfully, including an instrumentation amplifier (IA), a gain-control amplifier (GCA) and a switched-capacitor lowpass filter (SCLPF). Based on the design technique of the wide-swing cascode, the analog processor achieves a high power-supply rejection ratio (PSRR), and can be operated at a supply voltage between 3 V and5 V. The wired and wireless systems built from the designed

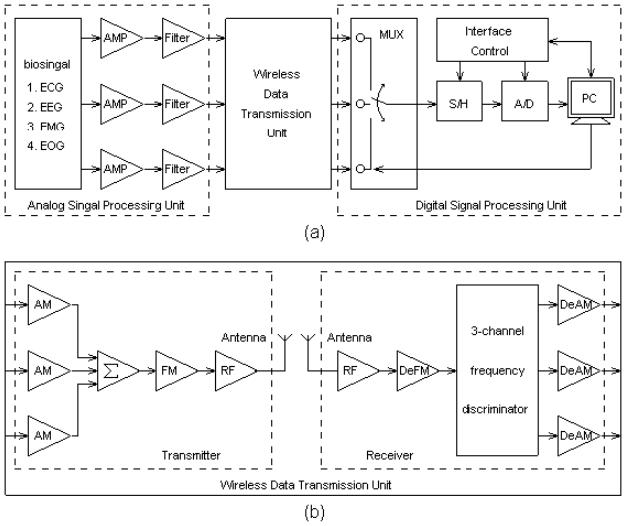

Figure 1. Block diagrams of the wireless biosignal monitor. (a) whole system, and (b) wireless data transmission unit.

processor chip and commercial discrete ICs were verified. The simulated ECG signals were used to evaluate the performance of both the wired and the wireless systems.

2. SYSTEM DESCRIPTION

Figure 1(a) shows block diagrams of the wireless biosignal monitor, including an analog signal processing unit, a wireless data transmission unit and a digital signal processing unit. The wireless data transmission unit consists of a transmitter and a receiver, as shown in Fig. 1(b). For a wired system, the input biosignal is directly transmitted from the analog processing unit to the digital processing unit. The wired system is used only for the short-distance or in-house biosignal monitoring. Multi-channel input biosignals are applied to the analog signal processing unit and amplified to a sufficient amplitude by the amplifier (AMP), which includes an IA and a GCA. The LPF is used to filter high-frequency noise because most biosignals have a frequency of less than 250 Hz. In a wireless data transmission unit, biosignals are modulated to successively higher frequency bands by amplitude modulation (AM) by carriers of different frequencies. These modulated waves are summed using an adder circuit (Σ) and then be modulated by frequency modulation (FM). The radio frequency (RF) power amplifier is employed to transmit the modulated signal through the antenna. An RF receiver receives the emitted signal, and then frequency demodulation (DeFM) is performed. A frequency discriminator separates the signal into three different frequencies and a bandpass filter filters other noise. Amplitude demodulation (DeAM) is then performed to recover the signal. In the digital signal processing unit, a multiplexer (MUX) selects the single-channel biosignal and transmits it to the sample-and-hold (S/H) circuit and the analog-to-digital converter (ADC). The interface control circuits process the signals between the ADC and the personal computer (PC). Finally, the measured data can be saved in the PC and then transferred to remote hospitals for monitoring.

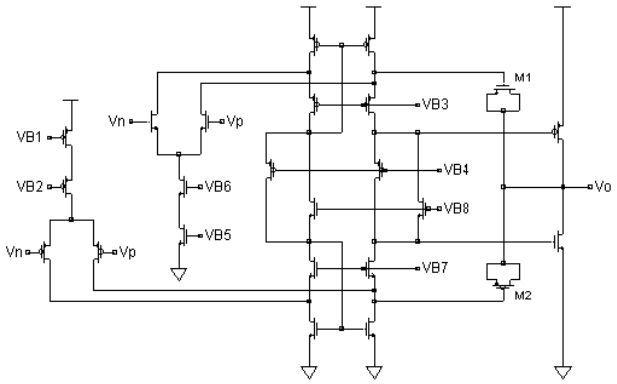

Figure 2. Schematic diagram of the two-stage OP.

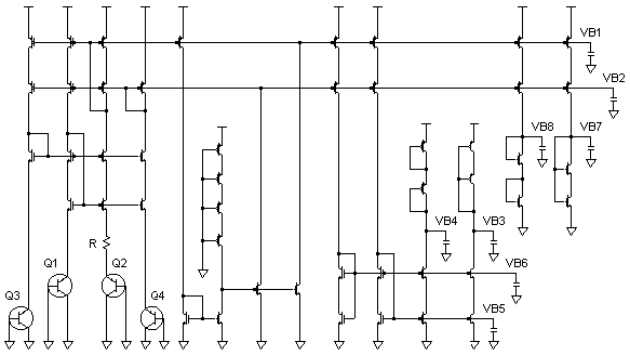

Figure 3. Schematic of the wide-swing cascode bias circuit.

3. CIRCUIT IMPLEMENTATION

3.1 Operational Amplifier and Bias Circuit

A two-stage cascode OP with rail-to-rail input/output stages and high PSRR, as shown in Fig. 2 [6], is used to construct all building blocks of the processor IC. The output impedance can be greatly reduced by the negative-feedback architecture. MOS transistors M1 and M2 with source and drain short connected serve as the compensation capacitors. To achieve low-power consumption, the operating points VB1-VB2 and VB5-VB6 of OP operate in the moderate inversion region, satisfying 0 mV < $(V_{gs} - V_T) < 50$ mV and 0 mV < $V_{ds} - (V_{gs} - V_T) < 25$ mV, where V_{gs} and V_{ds} are the gate-source voltage and the drain-source voltage of a MOS transistor, respectively, and V_T represents the threshold voltage. The simulated tail current in both the P-channel and the N-channel input pairs of the OP is only 0.225 μA. The optimal biasing design and the maximum layout area of the input MOS transistors and the current-mirror load are implemented to achieve a low offset voltage.

The wide-swing cascode bias circuit is realized to provide a stable bias current for the OP, as shown in Fig. 3. Assume that the emitter-area ratio of the bipolar junction transistors (BJTs) Q2/Q1 = m; then, the current that flows into the emitter of BJT Q2 can be expressed as (3-1)

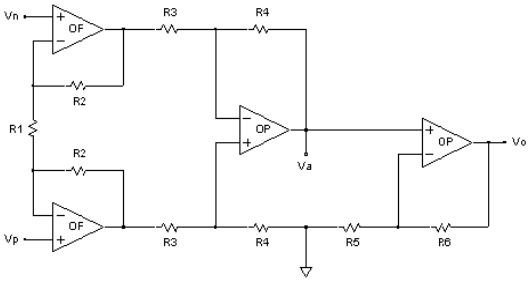

Figure 4. Schematic of the designed AMP.

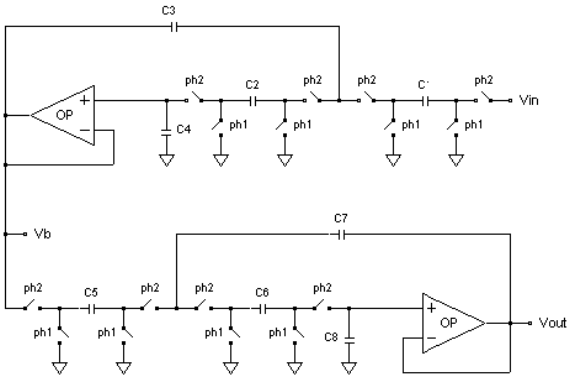

Figure 5. The fourth-order SCLPF realized in this work.

$$I = \frac{V_T[\ln(m)]}{R} \tag{3-1}$$

This bias current is mirrored to the OP for producing the operating points. Noise from the power supply can be reduced by connecting additional capacitors to VB1-VB8 to stabilize the operating points. A start-up circuit is included; it affects only the bias circuit in the case all currents in the loop are zeros.

3.2 Instrumentation Amplifier and Gain-Control Amplifier

As shown in Fig. 4, an AMP consists of an IA and a GCA. The IA, based on the conventional structure of three OPs and resistors, is used to amplify the input biosignals. V_p and V_n represent the input voltages at the positive and negative terminals, respectively. The output voltage V_a of this IA can be derived as (3-2)

$$V_a = \frac{R_4}{R_3}(1+\frac{2R_2}{R_1})(V_p - V_n) \tag{3-2}$$

where R1 = R3 = 1 kΩ, R2 = R4 = 2 kΩ, and the gain of this IA is 20 dB. This IA exhibits a very high PSRR and CMRR. The closed-loop architecture makes this IA stable at all times, and the offset voltage is not amplified to the point at which the outputs of each OP in this IA saturate. The non-inverting GCA consists of an OP and two resistors. The gain of the GCA can be derived as (3-3)

$$\frac{V_o}{V_a} = 1 + \frac{R_6}{R_5} \tag{3-3}$$

Resistors R5 = 2 kΩ and R6 = 58 kΩ are used in this design to achieve a DC gain of 30. This GCA is also a closed-loop circuit.

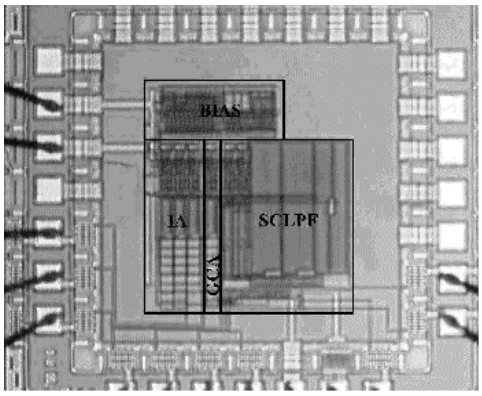

Figure 6. Photomicrograph of the fabricated test chip.

3.3 Switched-Capacitor Lowpass Filter

Figure 5 presents the designed fourth-order SCLPF, which is implemented by cascading two second-order filters. Without a standard architecture of the SC biquad, this filter is realized using some basic building blocks of SC filters, including OPs, switches and capacitors. The NMOS transistor and its dummy transistor, with the drain and source shorted together, constitute the switches. The channel width of the dummy transistor is half of that of the NMOS transistor for a given channel length, eliminating the channel charge injection [7]. Minimally sized switches reduce the error voltage from the clock feedthrough. A parasitic-insensitive scheme for realizing the SC-simulated resistor greatly decreases the second-order errors. The two-phase nonoverlapping clock schemes of ph1 and ph2 activate the MOS transistors' switches. Figure 6(b) depicts the nonoverlapping clock generator and two-phase clocking schemes for this SCLPF. As shown in Fig. 5, the transfer function of $V_b(s)/V_{in}(s)$ is derived as (3-4)

$$\frac{V_b(s)}{V_{in}(s)} = \frac{(\frac{C_1C_2T^2}{C_3C_4})}{s^2 + s(\frac{C_1+C_2}{C_3T}) + (\frac{C_1C_2T^2}{C_3C_4})} \tag{3-4}$$

C1 = C2 = C5 = C6 = 5 pF, C3 = C7 = 56.27 pF, C4 = C8 = 28.135 pF, and a clock period of T = 50 μs yield a passband frequency of 200 Hz.

4. EXPERIMENTAL RESULTS

Figure 6 illustrates the photomicrograph of the fabricated test chip, including a bias circuit (BIAS), an IA, a GCA, and a SCLPF. It was implemented in a 0.5 μm silicon-gate n-well CMOS technology, and has a die area of 0.52 mm^2. With the wide-swing cascode bias circuit design, this processor IC can be operated at a single supply voltage in the range between 3 V and 5 V. Measured power consumption of this chip is 0.42 mW and 0.75 mW at a supply voltage of 3 V and 5 V, respectively.

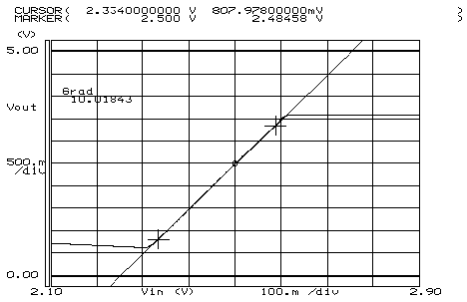

Figure 7. DC measurement of the IA.

Table 2. Measured Results of the IA.

Specifications	Power = 3 V	Power = 5 V
Designed DC gain (10)	9.985	10.018
DC offset	1.28 mV	1.54 mV
CMRR (at DC)	> 100 dB	> 98 dB
PSRR (at DC)	> 105 dB	> 102 dB
Current consumption	56 μA	63 μA
Die area	0.11 mm^2	0.11 mm^2

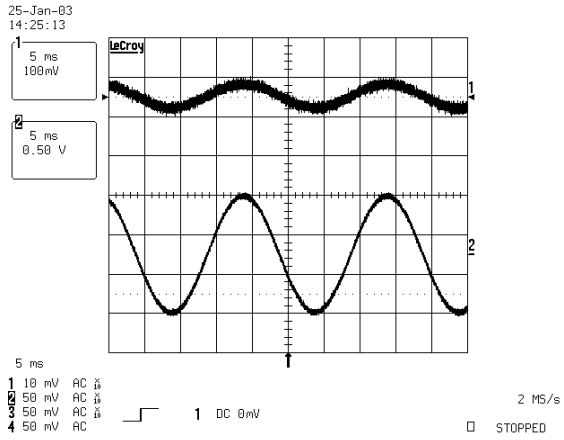

Figure 8. Measured result of the GCA.

Figure 7 shows the results measured with a 5-V supply voltage and a 2.5-V analog ground. The horizontal axis represents the positive input voltage V_{in} of the IA with a negative input terminal connected to the analog ground, while the vertical axis stands for the output voltage V_{out} of this IA. The gradient (Grad) specifies the DC gain of the IA, while the markers indicate the measured total equivalent output offset voltage V_{OS} at a V_{in} of 2.5 V. As shown in Fig. 7, the measured V_{OS} induced by each OP of this IA yields an equivalent input offset voltage of 1.54 mV. The IA has a measured DC gain of 10.01843. Table II summarizes the measured specifications of the IA at supply voltages of 3 V and 5 V. Average measurements were obtained over six samples. The table implies that the designed IA excels in high CMRR and PSRR, and achieves a low DC offset and an accurate DC gain. This IA has a low power consumption of 0.315 mW at a supply voltage of 5 V, and occupies a small chip area of 0.11 mm^2. Figure 8 plots the results measured for GCA at a 5-V supply voltage.

Table 3. Measured Results of the GCA.

Specifications	Power = 3 V	Power = 5 V
Proposed DC gain (30)	29.328	29.536
DC offset	1.92 mV	2.27 mV
CMRR (at DC)	> 95 dB	> 93 dB
PSRR (at DC)	> 90 dB	> 87 dB
Current consumption	22 μA	26 μA
Die area	0.03 mm^2	0.03 mm^2

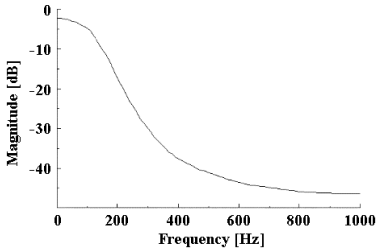

Figure 9. Measured frequency response of the SCLPF.

Table 4. Measured Results of the SCLPF.

Specifications	Power = 3 V	Power = 5 V
DC gain	-1.97 dB	-1.89 dB
DC offset	2.85 mV	2.37 mV
Band Width	>100 Hz	>100 Hz
Current consumption	8.2 μA	9.7 μA
Die area	0.3 mm^2	0.3 mm^2

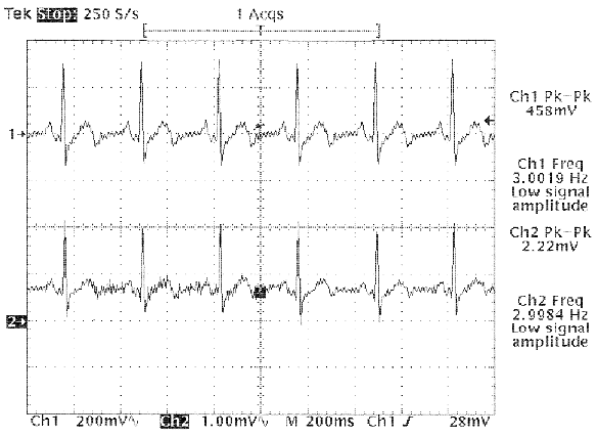

Figure 10. Measured result of the analog processor.

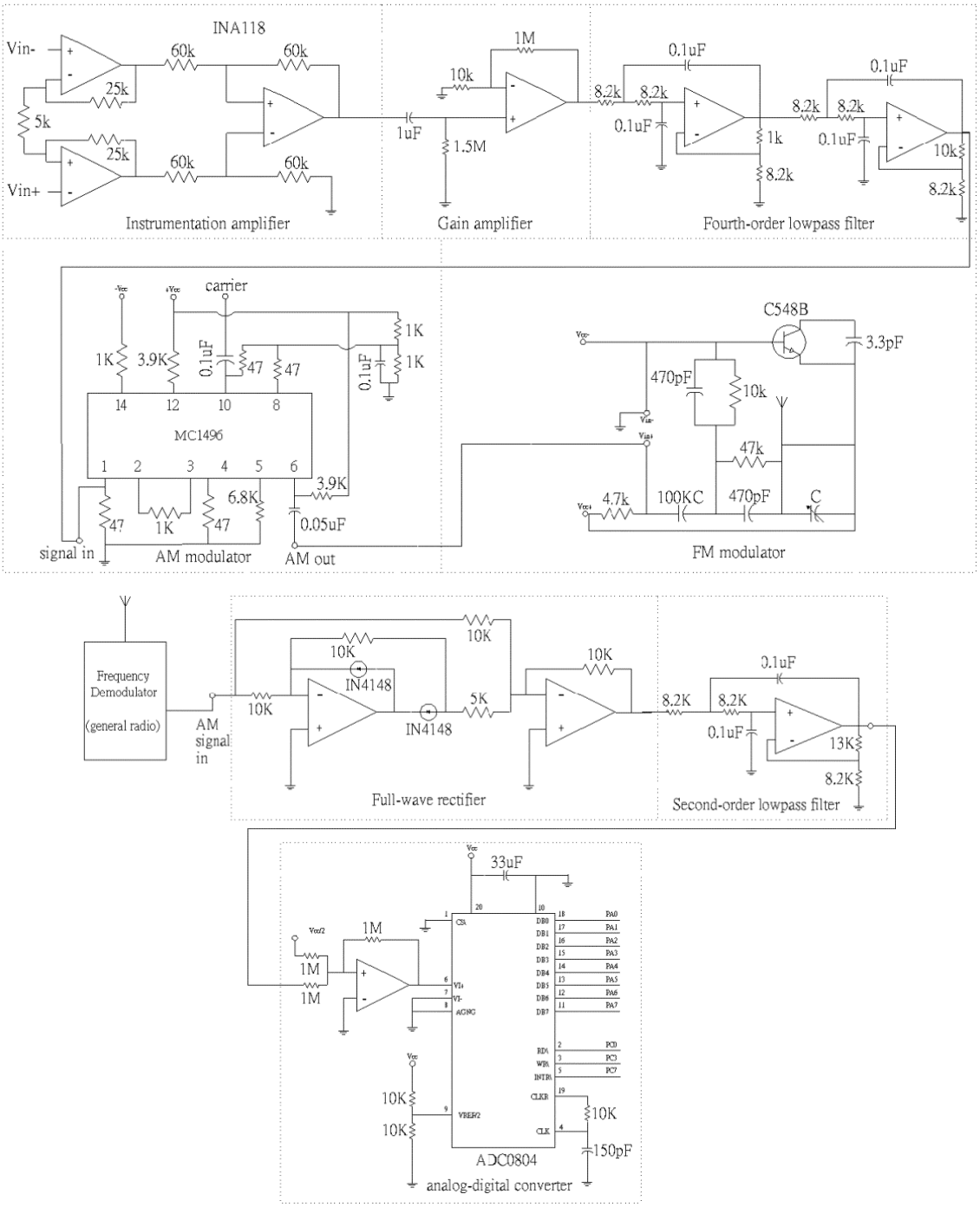

Figure 11. Validation of the single-channel wireless biosignal monitor constructed using on-board commercial discrete ICs.

Channel 1 shows the input signal of 50 mV_{P-P}, and channel 2 shows the measured output sinusoidal signal of 1.5 V_{P-P}. This GCA has an amplification of 30 times. Table III lists the measured data for the designed GCA at supply voltages of 3 V and 5 V, and results were averaged over six samples. This GCA has a low power consumption of 0.13 mW at a supply voltage of 5 V, and occupies a small chip area of 0.03 mm^2. This designed GCA also achieves a high PSRR. The frequency response of the SCLPF was measured at a supply voltage of 5 V, as shown in Fig. 9. The result shows that the bandwidth is more than 100 Hz, and the attenuation of the filter is –1.89 dB at DC. Table IV lists other measured characteristics of this SCLPF at supply voltages of 3 V and 5 V, averaging results over six samples. This SCLPF has a low-power

consumption of 0.0485 mW at a supply voltage of 5 V, and occupies a small chip area of 0.3 mm^2.

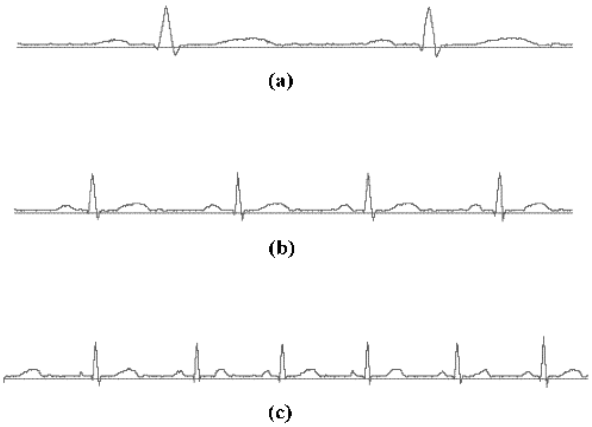

Figure 12. Measurement of the integrated on-chip single-channel wireless biosignal monitor with a 1-kHz carrier. Frequencies of the input ECG signal are (a) 1 Hz, (b) 2 Hz, and (c) 3 Hz.

The input ECG signal from the ECG simulator is applied to the analog processor IC to verify the circuit's performance. As shown in Fig. 10, channel 2 depicts a 2.22-mV_{P-P} input ECG signal with a frequency of 2.9984 Hz, while channel 1 illustrates the measured output ECG signal of 458 mV_{P-P} with a frequency of 3.0019 Hz. The measured signal amplification is within the design tolerance of the system. The single-channel wireless and wired systems constructed using on-board commercial discrete ICs have also been verified in this work, as shown in Fig. 11. A commercial IC INA118 realizes the IA, which has a DC gain of 11. The output terminal of the IA is connected to a highpass filter, which consists of a 1-μF capacitor and a 1.5-MΩ resistor. The GCA is realized by connecting the commercial OP TL062, and two resistors of 10 kΩ and 1 MΩ, to yield a non-inverting gain of 101. The commercial OP LM324 and some RC components are used to implement a second-order Butterworth LPF. Two cascading second-order LPFs constitute a fourth-order filter. The wireless data transmitter, including an AM modulator realized by an MUX IC MC1496, is used to multiply the biosignal and the carrier, and an FM modulator is realized by an C548B IC and RC components. An antenna is connected to the FM module to transmit the modulated signal. The wireless data receiver is constructed from a general radio as a frequency demodulator and an amplitude demodulator that includes a full-wave rectifier and a second-order LPF. A commercial IC ADC0804, connected to an adder circuit, is used to implement the digital signal-processing unit, which includes an MUX, an S/H circuit and an A/D converter. The software can control the measured data and which then saved in a PC. Measurement of the integrated on-chip single-channel processor system with a 1-kHz carrier has been illustrated in Fig. 12. The input ECG signals applied to the processor IC have the frequencies of 1 Hz, 2 Hz and 3 Hz, respectively. Experimental results show the input ECG signal can be amplified, filtered, transmitted, and received by the wired and wireless system design.

5. CONCLUSIONS

In summary, the wireless data transmission provides a more flexible way to measure the physiological signals of patients than the wired system. The proposed single-chip analog processor solves the component mismatch and performance degradation problems of the biosignal monitoring system built from discrete ICs. It can be operated at single supply voltage in a range between 3 V and 5 V, and has a low power consumption of 0.42 mW and 0.75 mW, respectively. The ECG signals were simulated to validate the wired and wireless systems, proving that the on-board system with the single-chip analog processor had achieved low power consumption, minimum chip size and low system cost.

6. ACKNOWLEDGMENTS

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