A 0.123 mW 7.25 GHz Static Frequency Divider by 8 in a 120-nm SOI Technology

Jean-Olivier Plouchart, Jonghae Kim, Hector Recoules, Noah Zamdmer,
Yue Tan, Melanie Sherony, Asit Ray, Lawrence Wagner

IBM Semiconductor Research and Development Center
2070 Rout 52, Hopewell Junction, NY 12533 USA
Phone: +1-845-892-9323 FAX: +1-845-892-6899
Email: plouchar@us.ibm.com

ABSTRACT

A static frequency divider by 8 was fabricated in a 120 nm SOI technology. The highest operation frequency achieved is 8.25 GHz at 1.5 V power supply. The lowest core power consumption achieved is 0.016 mW at 4 GHz when the lowest operating voltage supply of 0.75 V is used.

Categories and Subject Descriptors

B.7.1 [**Integrated Circuits**]: Types and Design Styles – *Advanced technologies, VLSI Integrated Circuits*

General Terms: Design

Keywords

Low Power, SOI CMOS, RF Circuit, Frequency Divider, CML

1. INTRODUCTION

High-frequency and low-power latches are fundamental building blocks for digital processing for mobile applications. They can also be used for communication applications to build frequency dividers. Owing to the lithography improvement CMOS technology is continuously improving the power consumption and the speed of such digital circuits. In 1993 a 50 ③W 1.2 GHz divider by two was reported using a 0.15 um SOI technology [1]. We fabricated and measured a divide by 8 in a 0.12 ③m SOI technology. The frequency divider by eight operates up to a maximum frequency of 8.25 GHz. At 0.75 V supply voltage, it operates up to 4 GHz for a 16 ③W power consumption.

2. FREQUENCY DIVIDER DESIGN

The architecture of the divider is based on six latches, and an output buffer (Fig. 1). Figure 2 shows the latch implementation, it is a based on a modified architecture presented by Fujishima [1].

ISLPED '03, August 25-27, 2003, Seoul, Korea.

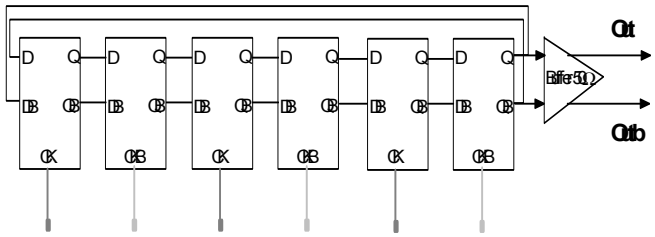

Figure 1 Divider architecture

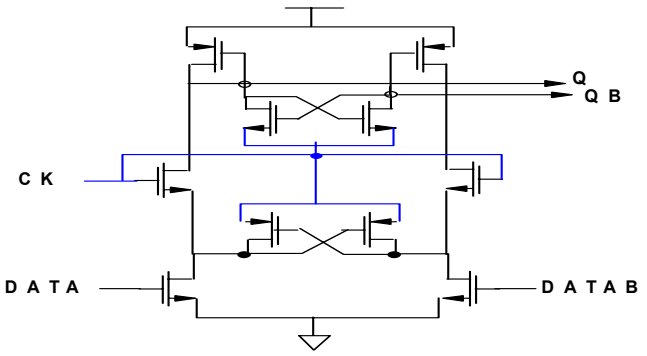

Figure 2 Latch schematic

One of the main differences with Fujishima's divider architecture is that two phases are required instead of one phase clock. The clock signal is single ended unlike in CML dividers where differential clock are used. Single-ended clock signals are more sensitive to common mode fluctuations, but since a full swing, ground to Vdd clock signal is used, the signal to noise ratio is high enough. The advantage of this type of divider is that the complexity is lower than other CMOS static dividers based on complex-gate, thus reducing area, gate, drain and parasitic capacitors. It is worth to note also that the complexity is slightly higher than CML latches, but CML logic has the issue of having always current flowing into the latches. Overall, it is a very suitable architecture for low-power applications. For input data and ouput signals (DATA, DATAB, Q and QB), differential signals are used. The transparent mode is set when CLOCK is high (Fig. 3 (a)) the two input transistors sense DATA and DATAB.

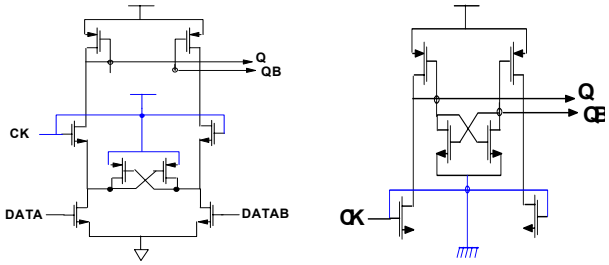

Figure 3 (a) Sense mode **(b) latch mode**

A cross-coupled PFET transistor pair allows faster switching time owing to the higher gain available in small signal mode. This pair is power by the clock itself. The hold mode appears when CLOCK is low (Fig. 3 (b)). The PFET cross-coupled pair is short circuited to ground but the top NFET cross-coupled pair becomes active. Therefore, the differential voltage value is maintained. DATA and DATAB are isolated from the outputs because the CLOCK transistors are off. The important point in this latch is the use of two cross-coupled pairs in both operation modes. Their activity is set by the clock input, which saves power. In order to optimize the divider-speed the transistor size were optimized. The NFET cross-coupled pair has a width of 0.35 ③m to achieve low parasitic capacitance at the output node. The PFET cross-coupled pair has a width of 4 ③m, and is a trade off between small signal gain and RC time constant. The PFET cross-coupled pair size is also a trade-off with the DATA NFET width of 4 ③m required to maintain strong input sensing devices. Finally the output buffer consists of three inverters in series, followed by a differential pair with 50 ⦸ resistor loads. For the layout, symmetries were respected, as much as possible. The master and slave latches are superposed vertically in order to respect the high-speed CLOCK signal direction and limit the length of the signal paths. The circuit was implemented in a 120nm CMOS SOI technology, described in [2, 3]. In order to avoid any limitation by the CMOS inverter speed, the full-swing two-phases clock signals are generated outside of the chip.

3. MEASUREMENT RESULTS

The circuit was measured on-wafer. The key issue is the generation of the full-swing two-phase clock signals. Figure 4 shows the measurement set-up. The sinusoidal signal coming from the synthesizer is divided using three 50 ⦸ power-dividers to generate the trigger, the sampling-scope clock, and the two delay lines signal. Each delay line has an adjustable delay between 0 and 160 pS. A 50 pS mismatch between the two clock-cables was measured. In order to generate the two clock-phases, the delays were adjusted at each frequency to compensate the cables mismatch and to add 180 degrees of phase shift. In this divider no input matching impedances were used, which is supposed to boost the amplitude on the incoming clock. The power of the synthesizer was adjusted at the highest operating frequency to achieve division. A synthesizer power of 15 dBm was used for all the measurements. Since the synthesizer generates only AC signals a bias–tee was used to shift the sinusoidal signal between ground and Vdd (fig. 4).

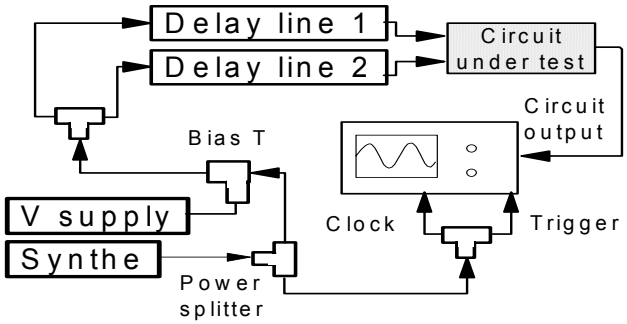

Figure 4 Measurement set-up

A Clock bias voltage equal to half of the voltage supply was used for all the measurements. At room temperature, the divider by eight is functional for a supply variation between 0.75 and 1.5 V. The maximum division frequency at 0.75 and 1.5 V is 4 and 8.25 GHz respectively (fig. 5).

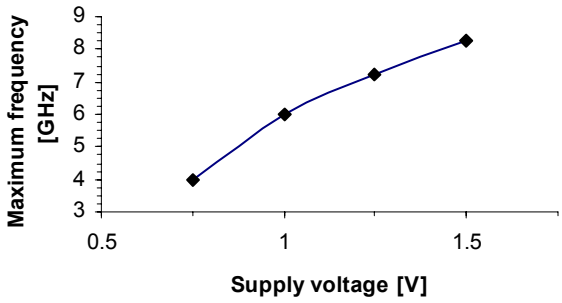

Figure 5 Maximum frequency vs. Supply voltage

Figure 6 shows the measured input and output signal waveforms for an input signal frequency of 8.25 GHz. The 8.25 GHz input-signal is correctly divided by eight.

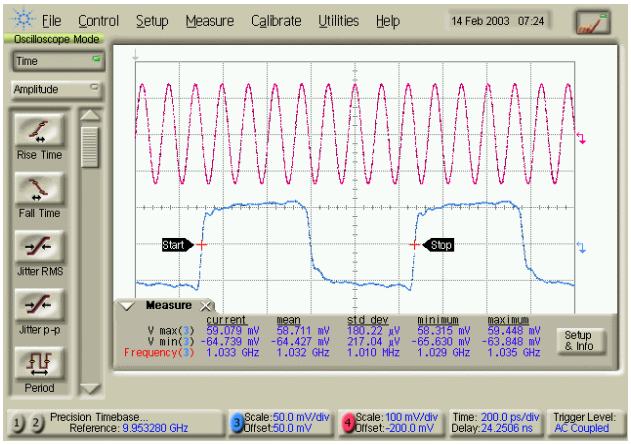

Figure 6 Sampling scope clock and output waveforms for an input clock frequency of 8.25 GHz and a 1.5 V voltage supply

The design includes two separate Vdd pins, one for the six latches and another one for the output buffers so that the current consumption from the core circuit and the output buffers can be

monitored separately. At maximum operating frequency and for a supply voltage of 0.75 and 1.5 V a core current consumption of 0.021 and 0.165 mA respectively is measured.

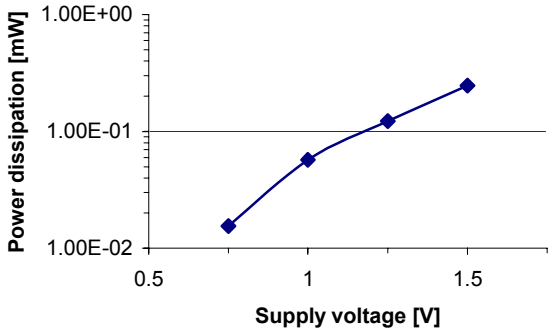

Figure 7 Power dissipation vs. Supply voltage

As shown in figure 7, this is equivalent to a power consumption of 0.016 and 0.247 mW at 0.75 and 1.5 V respectively. At 1.25 V the power consumption is 0.123 mW at the maximum 7.25 GHz operating frequency.

Table 1- Comparison of state of the art frequency dividers

Reported Circuit	Frequency (GHz)	Core Power (mW)	Supply Voltage (V)	Power Delay (fJ)
0.15 um SOI divider by2 [1]	**1**	**0.05**	**1**	**50**
0.12um SOI CML divider by 2 [4]	**25**	**2.7**	**1**	**108**
This work divider by 8	**4**	**0.016**	**0.75**	**4**

The measured output buffer current consumption is 7.7 to 8.6 mA from a 0.75 to 1.5 V supply respectively. The buffer generates 100 mV peak to peak square-wave waveforms on 25 ohms (50 ohms on chip resistor in parallel with 50 ohms sampling scope load).Table 1 compares state of the art frequency dividers. Despite that the divider by eight has more latches than a divider by two, a lower power delay product of only 4fJ is achieved. This architecture provides also lower power delay product than Current Mode Logic architecture but the maximum operating frequency is much lower. At 1 V the maximum operating frequency is 6 GHz versus 24 GHz for the CML architecture. Figure 8 shows the microphotograph of the chip and the input and output CPW lines.

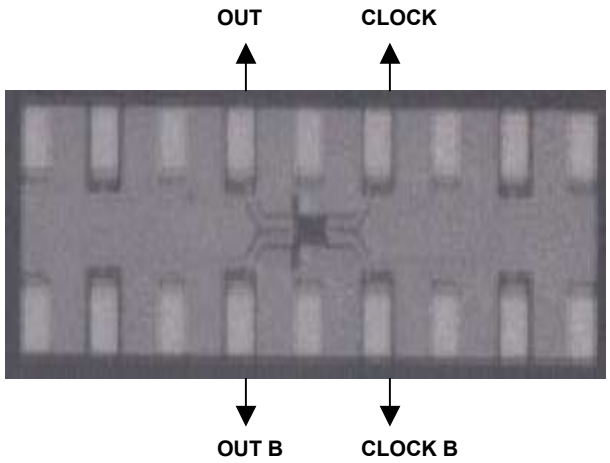

Figure 8 Divider (8:1) microphotograph (Dimensions: 0.4mm x 1.4 mm)

4. CONCLUSION

A static frequency divider by 8 was fabricated in a 120 nm SOI technology. The highest operation frequency achieved is 8.25 GHz at 1.5 V and for a 0.247 mW power consumption. The lowest core power consumption achieved is 0.016 mW at 4 GHz when the lowest operating voltage supply of 0.75 V is used. This is equivalent to a 4fJ power delay product.

5. ACKNOWLEDGEMENT

The authors would like to thank the contribution of our colleagues at the Advanced Semiconductor Technology Center, and the support of Daniel Friedman, Mehmet Soyuer, Susan Chaloux, G. Shahidi, and B. Davari.

6. REFERENCES

[1] Fujishima, M.; Asada, K.; Omura, Y.; Izumi, K.; "Low-power 1/2 frequency dividers using 0.1-µm CMOS circuits built with ultrathin SIMOX substrates," IEEE Journal of Solid-State Circuits, Volume: 28 Issue: 4, pp. 510-512 ,April 1993.

[2] Zamdmer, N.; Ray, A.; Plouchart, J.-O.; Wagner, L.; Fong, N.; Jenkins, K.C.A.; Jin, W.; Smeys, P.; Yang, I.; Shahidi, G.; Assaderaghi, F. , "A 0.13-um SOI CMOS technology for low-power digital and RF applications," VLSI Technology Symposium, Digest of Technical Papers, pp. 85-86, June 2001.

[3] N. Zamdmer, JO. Plouchart, J. Kim, "Suitability of Scaled SOI for High-Frequency Analog Circuits," IEEE ESSDERC., pp. 511-514, September 2002.

[4] Jean-Olivier Plouchart, Jonghae Kim, Hector Recoules, Noah Zamdmer, Yue Tan, Melanie Sherony, Asit Ray, Lawrence Wagner "A Power-Efficient 33 GHz 2:1 Static Frequency Divider in 0.12-µm SOI CMOS," IEEE2003 Radio Frequency Integrated Circuit Symposium, June 2003