A New Architecture for Rail-to-Rail Input Constant-g_m CMOS Operational Transconductance Amplifiers

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ABSTRACT
A new architecture for constant-g_m rail-to-rail(R-R) input stages is presented that has less than 5% deviation in g_m over the entire range of the input common-mode voltage. Furthermore, a new structure for folded cascode amplifier based on the use of a floating current source is presented. Employing these techniques a low-power operational transconductance amplifier(OTA) with 100MHz unity-gain bandwidth, 106dB gain, 60° phase margin, 2.65V swing, and 6.4nV/√Hz input-referred noise with R-R input common-mode range is realized in a 0.8μm CMOS technology. This amplifier dissipates 10mW from a 3V power supply.

Categories and Subject Descriptors
Integrated circuits

General Terms
Design

Keywords
Rail-to-rail, transconductance, current summation, floating current source, input stage, operational transconductance amplifier.

1. INTRODUCTION
Operational amplifier is one of the most widely used functional blocks for high-level analog and mixed-signal integrated circuit design. One design issue of many circuits or systems is that their overall achievable performance directly depends on the used op amps. High-speed operational transconductance amplifiers with R-R input common-mode range have a wide range of applications in high-speed continuous-time filters and equalizers where the OTA-C architecture is sometimes the only candidate.

At large supply voltages, there is a trade off among speed, gain and power of an operational amplifier. Signal swing becomes yet another performance metric to be considered when designing operational amplifiers at low supply voltages [1].

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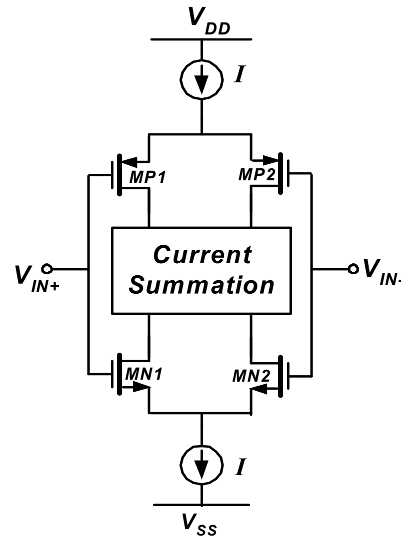

Figure 1. A simple rail-to-rail input stage

For designing high swing op amps in low supply voltages, output swing is not usually a problem because a class-A or class-AB output stage or even a folded cascode architecture can drive loads close to power supply voltage. However, opamps with high-swing input stages are still challenging to design.

To have a R-R input common-mode range, two complementary differential pairs are required to form the input stage (Figure 1) [2]. However, this circuit suffers from some drawbacks. The total input transconductance, g_{mT}, is given by the sum of the transconductances of the NMOS and PMOS differential pairs. At the extreme input voltage ranges, only one input pair is active, so the effective transconductance is halved. Therefore, the deviations in g_{mT} as a function of input common mode voltage, V_{CM}, can be as much as 100%. This is not desirable because it complicates the frequency compensation and also results in harmonic distortion [3]. Furthermore, at large signal regime, the large signal output current is also halved at the extreme input ranges. This means that the slew rate of a conventional single-stage or two-stage amplifier with this input stage will be a function of V_{CM}.

Limitations of Figure 1 were incentive for analog designers to innovate input stage topologies that have constant input transconductance over the whole range of V_{CM} [3-7]. Additionally, because of some other limitations, using these input stages in single stage amplifiers does not result in good performance with respect to power dissipation. Indeed, almost all of the R-R constant-g_m operational amplifiers have been realized in two or three stage configurations, which this limits the bandwidth and speed of amplifier.

In this paper, in Section 2, we present a new R-R constant-g_m input stage that has superior performance compared to the other configurations. Besides, a new architecture for current summation circuit based on the use of a floating current source is presented in Section 3. By the use of these new architectures, a low-power single-stage operational transconductance amplifier with R-R input common-mode range and almost constant-g_m capability is proposed. In Section 4, simulation results are presented to illustrate the effectiveness of the approaches, and Section 5 is the conclusion.

2. INPUT STAGE ARCHITECTURE

A popular approach for designing constant-g_m R-R input stages is to sense that one of the input pairs has lost needed gate bias for proper operation, takes away the unused tail current of that pair through a bypass transistor, amplify it by a factor of 3 with a current mirror and add it to the tail current of the active pair [5].

In spite of the simplicity of this approach, it has several shortcomings. The main drawback of this method becomes important in submicron processes in which square law equation in an MOS transistor is no longer valid. Amplification of tail current by 3 and addition of this to the tail current of active pair is not good enough to realize R-R input stages, as in submicron CMOS processes, short channel effects mean that the factor 3 should be 5 or 6, depends on the technology. As a result, at the extreme input voltage ranges, the power consumption becomes considerably high. Furthermore, this makes the design of current summation (folded cascode) circuit difficult.

There are some structures [6-7] which their operation are not based on MOS squre law equation, however, their input transconductance are subject to large variations. The operation of the novel architecture presented here is not also based on the MOS square law equation. Besides, it maintains a nearly constant g_m in the whole range of V_{CM} and shows superior performance copared with other structures.

The principle of this new technique is to activate another pair similar to the active pair when one pair has lost required gate bias for proper operation. As a result, at extreme supply voltage ranges that one of input pairs turns off, two similar pairs of other polarity generate signal current in parallel, and so the input transconductance doubles. To implement this approach, as it is shown in Figure 2, three differential pairs of each polarity are used. All the PMOS differential pairs have equal *W/L* and all the NMOS differential pair transistors are also identical.

When V_{CM} is at the midway of supply voltages, amongst the NMOS transistors, *MN1* and *MN2* generate signal current, and among the PMOS transistors, the pair *MP1-MP2* does this work. In this region of operation, the current of the source I_{N3} flows through transistors *MN5* and *MN6* and sinks all the tail current of the pair *MP3-MP4*, and switches off this pair. On the other side, the current of the source I_{P3} flows through transistors *MP5* and *MP6* and supplies all the tail current of the pair *MN3-MP4*, and also this pair switches off. Hence, only four devices *MN1*, *MN2*,

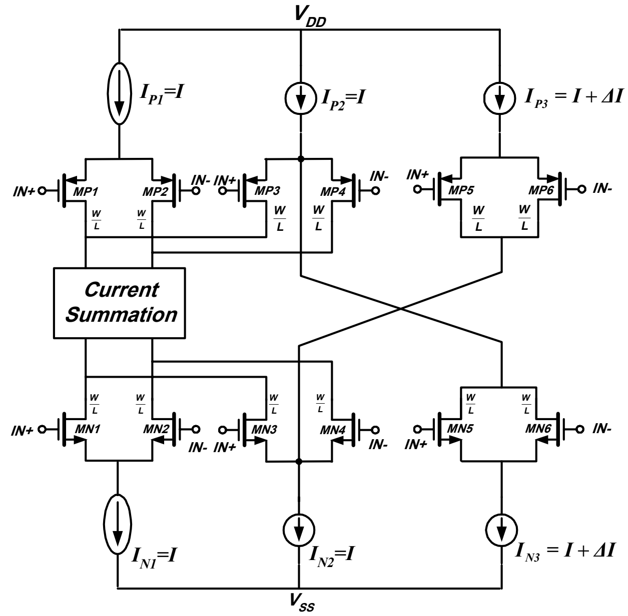

Figure 2. New constant-g_m rail to rail input stage

MP1, and *MP2* are generating signal current and g_{mT} is equal to the sum of input NMOS transistor transconductance, g_{mn}, and input PMOS transistor transconductance, g_{mp}.

If the sizes of the PMOS and NMOS transistors are chosen such that g_{mn}=g_{mp}=g_m, then g_{mT} is equal to 2g_m. There is also a total current of *2I* available for the current summer when the circuit is in slew-limited regime.

When V_{CM} is near V_{DD}, none of the PMOS transistors have sufficient V_{GS} to remain active. Since there are no other path for tail current sources I_{P1} and I_{P3}, these current sources are deactivated. Therefore, the tail current source I_{N2} is not supplied from anywhere and flows through the pair *MN3-MN4*. So this pair turns on and works in parallel with the main pair *MN1-MN2*. As a result, g_{mT} is equal to 2g_{mn} which is equal to 2g_m. There is also a total current of *2I* available in the limiting situation.

At the other extreme point of V_{CM}, similarly, I_{N3} is pushed to be off and I_{P2} flows through *MP3* and *MP4*. So the equivalent transconductance is 2$g_{mp.}$ There is also a total current of *2I* available in the slew-limited regime.

If because of transistor mismatches, the current value of I_{N2} and I_{P2} becomes slightly higher than *I*, or the current value of current sources, I_{N3} and I_{P3}, becomes slightly lower than *I*, the pairs *MN3-MN4* and *MP3-MP4* will turn on when V_{CM} is in the midway of supply voltages. This undesired activation of pairs *MN3-MN4* and *MP3-MP4* increases g_{mT} and enhances the g_{mT} deviations of input stage. By adjusting the current of current sources I_{P3} and I_{N3} slightly higher than *I*, i.e. *I*+*ΔI*, above problem will be eliminated.

In this new circuit, by handling the *W/L* and V_{GS} of the transistors of the tail current sources, the g_{mT} deviation can be more reduced. The principle of decreasing the g_{mT} deviation is shown in Figure 3. The solid and the dotted lines are the g_{mT} and its components before and after the improvement, respectively. The overhangs in the g_{mT} curve are because of the large slope in the g_m of differential pairs in turning on and off intervals. As it is shown in the Figure 3, if the slopes of the curves are decreased, the g_{mT} curve becomes smoother. For example when the pair *MN3-MN4* is turning on, the other pair, *MP1-MP2*, is turning off. If the slopes of g_m when these pairs are turning on and off are constant and equal, by adding the two curves the g_{mT} will be constant, but the curve of g_m in the zone that the pairs are turning on or off is similar to a parabola. As it is shown in Figure 3, by decreasing the slope of the curves, the deviation in g_{mT} will be reduced more. To decrease this slope, i.e. the slope of the g_m-V_{CM} curve of a differential pair when turning on, the effective voltage, $V_{DS,sat}$, of the tail current source transistor should be increased. That is, the effective voltages of the transistors which realize the current sources I_{N1} and I_{P1} should be increased. This can be done simply by reducing their *W/L* and increasing their V_{GS}.

By cascoding the tail current sources I_{N2}, I_{N3}, I_{P2}, and I_{P3}, the deviations in g_{mT} reduce more. With this topology, the g_{mT} deviations could be less than 5%. The simulated result of the g_m of the new input stage is shown in Figure 4.

3. CURRENT SUMMATION CIRCUIT

Another important block in an OTA with R-R input common-mode range is the current summing circuit. The conventional approach for realizing this circuit is shown in Figure 5.

However, when this circuit is used in single-stage amplifiers, some problems are caused in frequency compensation of the amplifier. These problems can be addressed as follows:

Regarding the Figure 5, The bias current of *M1* and *M2*, I_B, must be able to supply the current of NMOS input device, I_N, and bias current of *M3-M6*, I_F. The current of the input NMOS stage, can vary from zero for minimum values of V_{CM} to more than $2I_n$ for values close to the positive rail; where I_n is the current of the NMOS input stage for mid-range values of V_{CM}. As a result, the bias current of transistors *M1* and *M2* must be able to supply these increments in the quiescent current of the NMOS input and also the minimum quiescent current for the transistors of the current summation circuit.

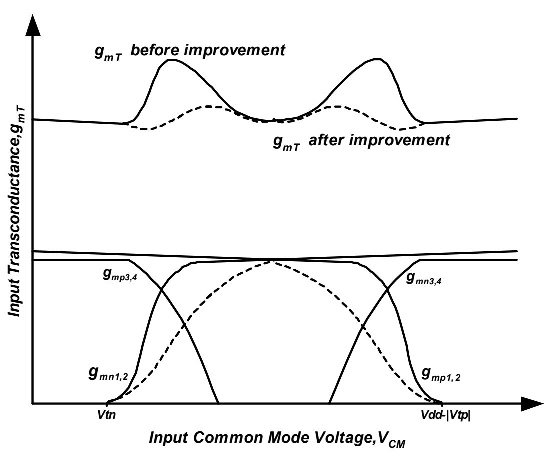

Figure 3. The principle of reducing the g_{mT} deviations in new R-R input stage.

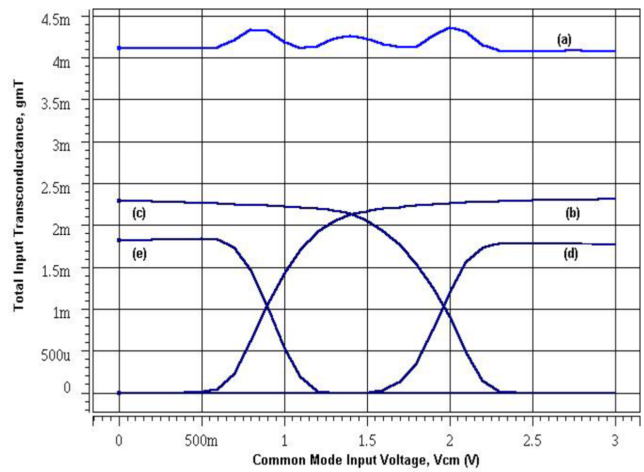

Figure 4. g_{mT} and its components versus V_{CM}, (a) *gmt*, (b) $g_{mn1,2}$, (c) $g_{mp1,2}$, (d) $g_{mn3,4}$, (e) $g_{mp3,4}$.

Note that, when V_{CM} is in the midway of supply voltages or close to the negative supply rail, the additional bias current of *M1* and *M2* flows through transistors *M3-M8*, and considerably changes their quiescent current and therefore their transconductance and output resistance. These variations lead to large variations in pole-zero locations and also the low-frequency gain of the amplifier.

These large variations in pole-zero locations complicate the frequency compensation and prevent the optimum usage of power in order to enhance the bandwidth. Here we can have a glance on the on the pole-zero location and gain of this amplifier. The poles and zeros of this opamp with reference to Figure 5 are located at:

$$P_1 = -\frac{1}{C_{out}R_{out}} \qquad P_2 = -\frac{g_{m4}}{C_X} \qquad P_3 = -\frac{g_{m6}}{C_Y}$$

$$P_{4,5} = -\frac{g_{m5}}{2C_Y}\left[1 \pm \sqrt{1 - \frac{4g_{m7}C_Y}{g_{m5}C_M}}\right]$$

$$Z_1 = -\frac{g_{m4}g_{m6}\left(g_{mn} + g_{mp}\right)}{g_{mn}g_{m4}C_Y + g_{mp}g_{m6}C_X} \qquad Z_{2,3} = -\frac{g_{m5}}{2C_Y}\left[1 \pm \sqrt{1 - \frac{8g_{m7}C_Y}{g_{m5}C_M}}\right]$$

where C_X, C_Y, C_M and C_{OUT} denote the total parasitic capacitances at nodes X, Y, M and OUT respectively. g_{mi}, g_{mn} and g_{mp} denote the transconductances of transistor *Mi*, the NMOS input stage and the PMOS input stage, respectively, and R_{out} is the output resistance of the amplifier obtained from:

$$R_{OUT} = (g_{m4}r_{O4}(r_{O2} \,||\, r_{ON})) \,||\, (g_{m6}r_{O6}(r_{O8} \,||\, r_{OP}))$$

where r_{oi} is the output resistance of transistor *Mi*. As it is obvious in above equations, any variations in the bias current of transistors considerably change the low-frequency gain as well as the frequency response of the amplifier.

These variations in the bias current of the current summation transistors are not very important in two- or multi-stage amplifiers that use R-R input stage. This is mainly due to the fact that in two- or multi-stage amplifiers the voltage swing in the output node of the first stage is not restrictive. Consequently, the aspect ratio of the output transistors of the first stage should not be high and the

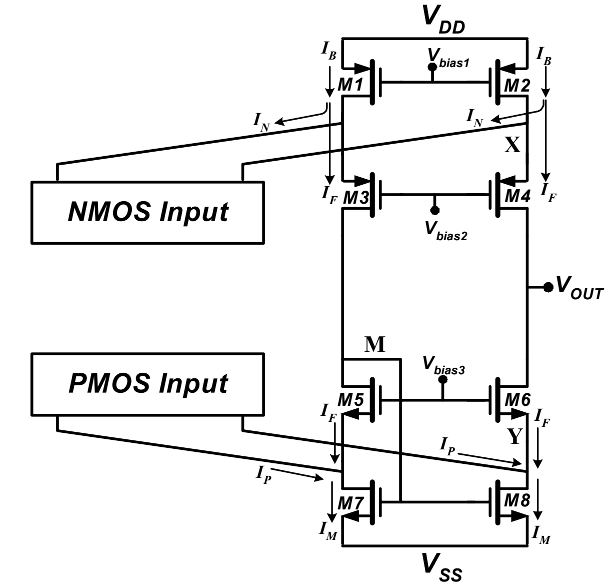

Figure 5. Conventional method for biasing current summation circuit.

parasitic capacitances in nodes X, Y, and M are negligible. So the poles due to these nodes are located at high enough frequencies to neglect the effects of their variations. Indeed, in these amplifiers the bandwidth of the amplifier is restricted to the poles of the second or other stages, which inherently are in lower frequencies.

However, when designing high swing single stage amplifiers, the voltage swing in the output node of the current summation circuit which is the output node of the amplifier should be high enough. Hence, the aspect ratio of the devices *M1-M8* and therefore the parasitic capacitances at nodes X and Y are increased and the small-signal parameters of these devices affect the frequency response of the amplifier considerably. For optimizing

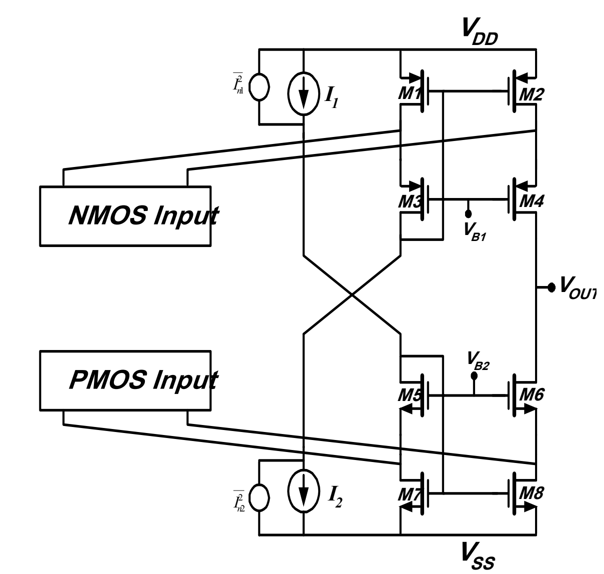

Figure 6. A simple approach for biasing current summation circuit.

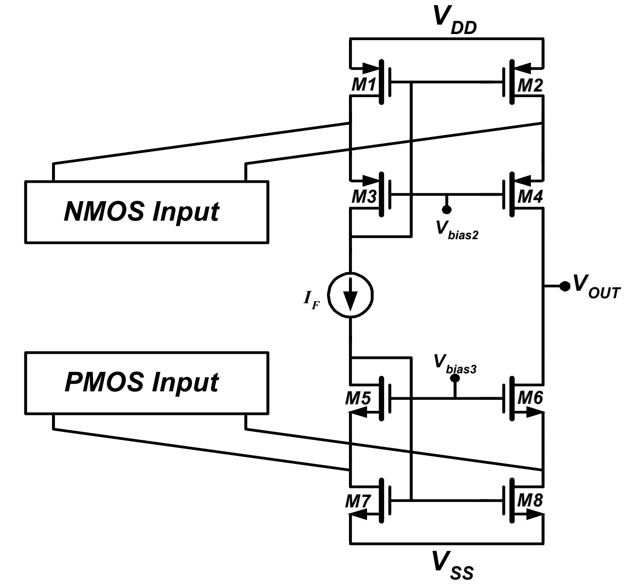

Figure 7. Using a floating current source for biasing the current summation circuit.

the power consumption of the opamp, the variations in the pole-zero locations due to the variations in the bias current, should be minimized to the possible extent. By a detail analysis, it is clear that the location of poles, P_2, P_3, $P_{4,5}$ and zeros, Z_1, $Z_{2,3}$ is directly related to the transconductance of transistors *M3-M6*. In fact, the transconductance and output resistance of these transistors have the most important role in the gain and pole-zero locations of the amplifier. Therefore, stabilizing the quiescent current of these transistors helps so much in optimizing the frequency compensation and reducing the harmonic distortion of the amplifier.

For this reason, both NMOS and PMOS cascoded transistors are used as current mirrors. Note that the current value of the current mirror changes automatically by the changes in the input differential pair currents. The remaining problem is biasing the current summation circuit.

The first approach is the use of two independent current sources as depicted in Figure 6. A drawback of this approach is that the bias current sources of the current mirrors contribute to the noise of the amplifier because the current gain between the current sources and the drain currents of the input transistors is equal to one. Besides, Any mismatches in the bias current sources will also increase the offset of amplifier [5].

By using a floating current source between the drain of transistors *M3* and *M5*, as shown in Figure 7, the mentioned problems are alleviated considerably. Besides, the bias current of transistors *M3-M6* becomes nearly constant. The circuit realization of floating current source with complete diagram of the entire amplifier is shown in Figure 8. The value of this floating current source is determined by the MOS translinear loops *M7*, *M9*, *M12*, *M11* and *M1*, *M10*, *M13*, *M14*. The use of floating current source has been used for the design of class AB amplifiers previously [5-6], however, in this paper, it has been employed to bias the current summation circuit.

Gain boosting has been also employed to ensure enough gain for the amplifier. Indeed, by two auxiliary folded cascode amplifiers, the output resistance of the amplifier increases extremely without degradation of frequency response [8]. However, in designing those auxiliary amplifiers, some precautions should be met to prevent slowing down the transient response.

The main parameter in designing the auxiliary amplifiers is their unity-gain bandwidth that should be about half of the frequency of the folding poles. That is, the unity-gain bandwidth of the auxiliary amplifiers X and Y should be chosen about half of the frequency of the poles P_2 and P_3, respectively [9].

4. AMPLIFIER SPECIFICATIONS

The proposed single-stage amplifier with constant-g_m R-R input stage has been implemented in a 0.8 μm double-poly, double-metal CMOS technology

It occupies a die area of 500*400(μm)^2 and consumes a total power of 10mW from a 3-V supply. The g_m of the input stage as shown in Figure 4 has a deviation of less than 5% over the entire R-R range of the input common-mode voltage. Figure 9 shows the simulated frequency response of the operational amplifier with a 5pF capacitive load. It shows that the unity-gain frequency is about 100 MHz. The variations of the unity gain bandwidth and phase margin versus V_{CM} are shown in Figures 10 and 11, respectively. Figure 12 shows the step response of the amplifier in unity gain feedback configuration. The 0.1% and 0.01% settling times of the amplifier are 15ns and 30ns, respectively. Besides, the slew rate of the amplifier is 150 V/μS, the output swing is 2.65V and input referred noise is 6.4nV/√Hz. The amplifier characteristics are summarized in Table 1.

Table 1. Amplifier characteristics(post-layout simulation) with a 3-V Supply voltage and 5pF capacitive load.

PARAMETER	VALUE
Gain (dB)	102
GBW (MHz)	100
Phase Margin(deg)	60
Settling Time 0.1(nS)	15
Settling Time 0.01(nS)	30
Slew Rate (V/μS)	150
Swing (V)	2.65
CMRR @ 1 KHz (dB)	121
Input noise voltage (nV/√Hz)	6.4
g_m variation(%)	5
Power dissipation (mW)	10

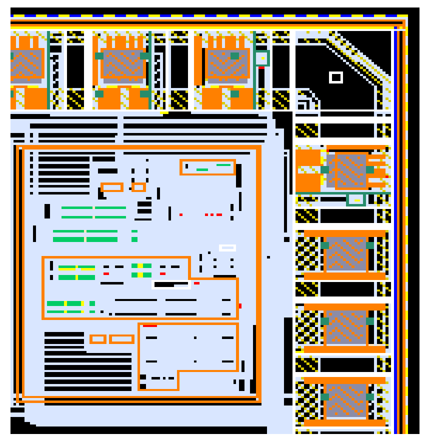

Fig. 10. Layout of the amplifier.

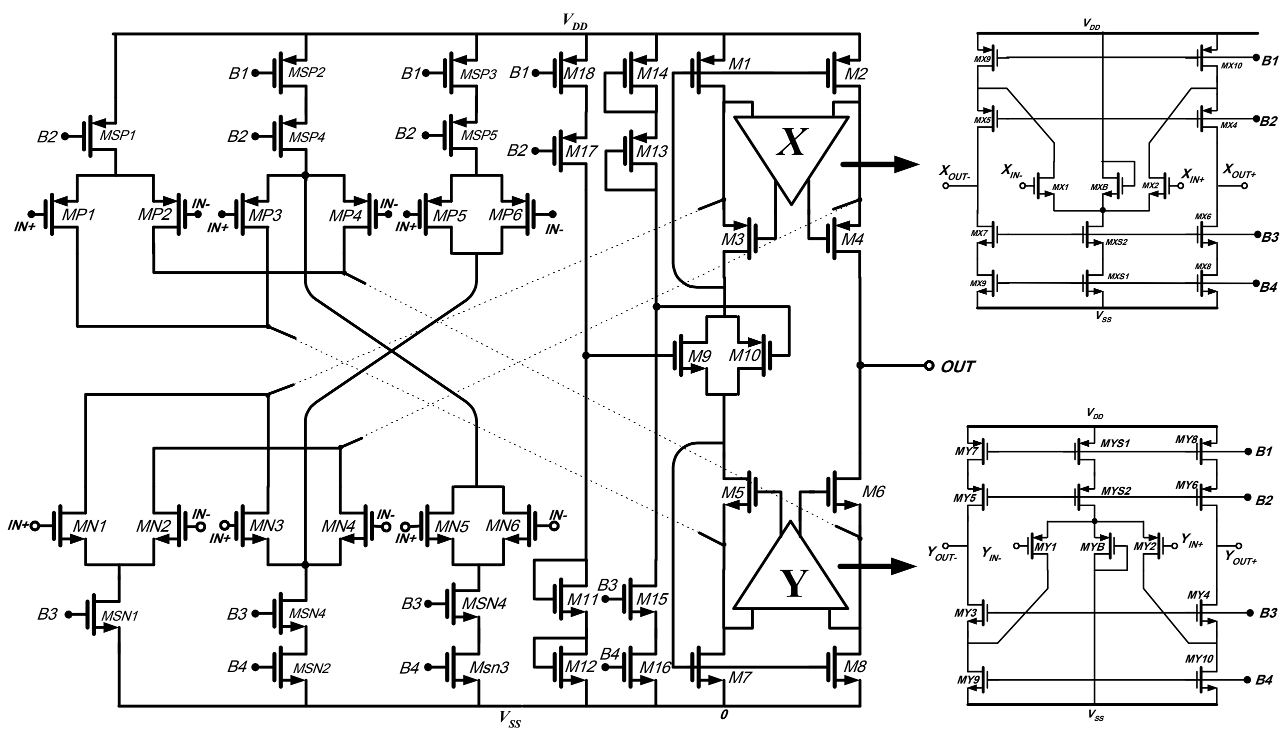

Figure 8. Complete schematic of the amplifier: the floating current source is realized by transistors *M9* to *M18*. There are two gain-boosting amps, X and Y. The circuit realizations of the amplifiers X and Y are shown in right hand of the figure.

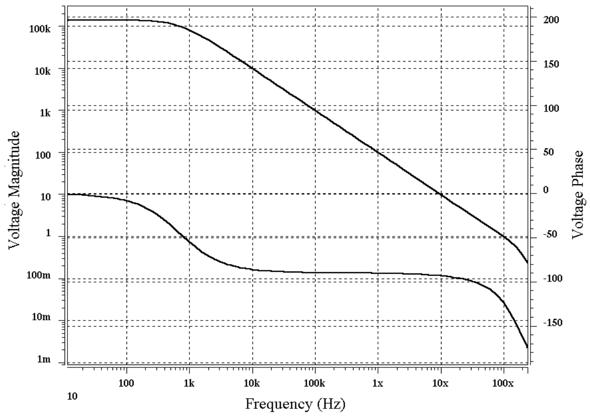

Figure 9. Frequency response of the designed amp.

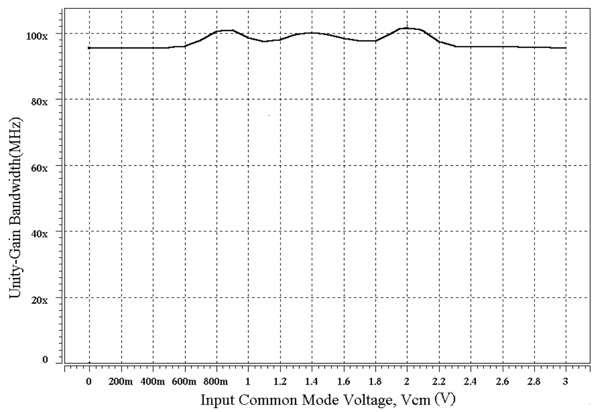

Figure 10. Unity-gain bandwidth deviations with respect to V_{CM}

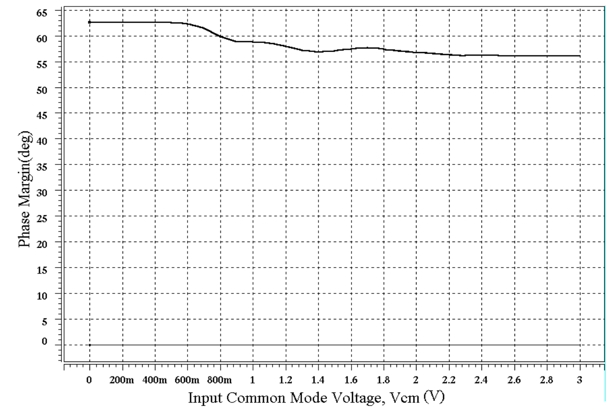

Figure 11. Phase margin deviations with respect to V_{CM}

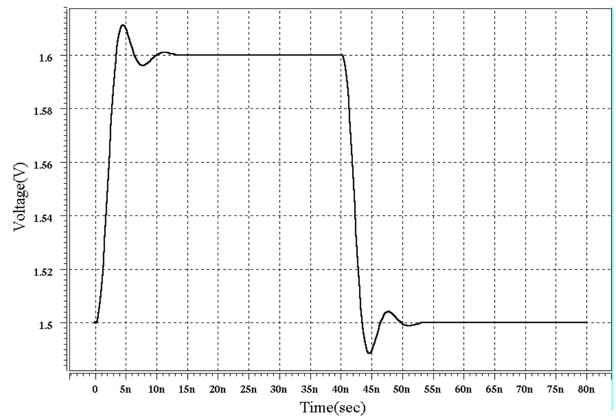

Figure 12. Small signal step response of the designed amp

5. CONCLUSION

In this paper, a new architecture for R-R constant-g_m input stages is presented, which not only its operation is not based on the MOS square law equation, but also has superior performance compared with other ones. Additionally, based on the use of a floating current source, a new architecture is presented for designing single-stage operational transconductance amplifiers. This floating current source biases the output transistors of the amplifier with minimum changes in the pole-zero location of the amplifier. Employing these new architectures, a low power, high swing, high speed, and high gain single-stage operational transconductance amplifier is designed and implemented in a 0.8μm double poly double metal CMOS process which consumes less than 10mW from a 3-V supply

6. REFERENCES

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