A Low-Power Design Methodology for High-Resolution Pipelined Analog-to-Digital Converters

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ABSTRACT

In this paper a general method to design a pipelined ADC with minimum power consumption is presented. By expressing the total static power consumption and the total input-referred noise of the converter as functions of the capacitor values and the resolutions of the converter stages, a simple optimization algorithm is employed to calculate the optimum values of these parameters, which lead to minimum power consumption while a specified noise requirement is satisfied. To determine the bias current values of operational amplifiers, a novel optimal choice for settling and slewing time parameters is proposed applicable to both single-stage and two-stage Miller-compensated opamp structures. Using the proposed methodology, the optimum values for capacitors, the resolutions and the opamp device sizes of all stages are determined in order to minimize the total power consumption. Design examples are presented and compared with conventional approaches to show the effectiveness of the proposed methodology.

Categories and Subject Descriptors

B.7.1 [Integrated circuits] Types and Design Styles *VLSI (very large scale integration)*

General Terms

Design

Keywords

Low-Power Design, Pipelined Analog-to-Digital Converters, Operational Amplifiers

1. INTRODUCTION

Pipelining is one of the best approaches to implement high-speed low-power analog-to-digital converters. Design approaches to reduce the power consumption of pipelined ADCs are therefore of great importance to realize medium-to-high resolution high-speed A/D converters with the least possible power consumption. Several approaches have been proposed in literature for systematic design of pipelined A/D converters. In [1] it has been concluded that to minimize the power consumption of a pipelined ADC, the resolution of all the stages can be chosen equal to 1.5 just in converters with resolutions of less than 10 bits. In [2] a systematic design methodology has been proposed where resolutions higher than 1.5 have been proposed for the front-end stages of the high-resolution converters but the capacitor values of the stages are not optimized and a predefined noise distribution is assumed. In [3] the effects of the capacitor scaling, parallelism, and non-identical resolutions per stages on the pipelined ADC power consumption are investigated separately. In the latest reported automatic design tool for pipelined ADCs [4] the converter is optimized to minimize the power consumption and area using geometric programming. However, the latter algorithm is applied to a converter with identical resolution per stages. As far as we understood it appears that neither of the proposed approaches are as general yet simple as the approach proposed in our work.

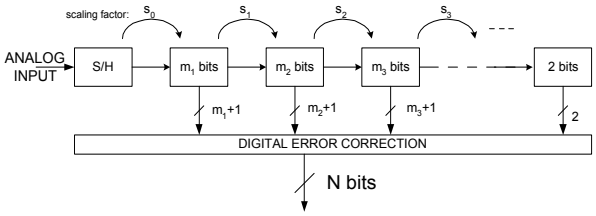

Figure 1. The pipeline ADC structure

In this paper with no specific constraint, arbitrary capacitor scaling as well as non-identical resolution per each stage is utilized in the design of the converter as shown in Fig. 1. Effective equations are presented to optimally determine the capacitor value and the resolution of each stage, in order to minimize the power consumption of the converter, which makes use of operational trans-conductance amplifiers (OTAs) with optimized settling and slewing times.

First, a closed-form equation for the bias current value of a single-stage or two-stage Miller-compensated opamp is derived employing an innovative dynamic allocation of the small- and large-signal settling time parameters. Then the total static power dissipation of the pipelined ADC is calculated. In section 3, the total input-referred noise of the converter is derived. Then a design methodology is presented to minimize the power consumption with a defined signal-to-noise ratio (SNR). The input parameters of the optimization CAD tool and related considerations are addressed. Finally optimization examples confirming the efficiency of the proposed methodology are presented and the dependency of the power consumption on the specifications of the converter is investigated.

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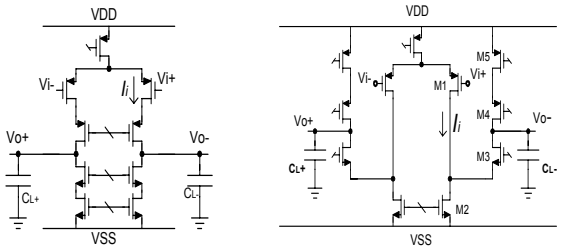

(a) (b)

Figure 2. The (a) telescopic- and (b) folded-cascode configurations

2. OPTIMUM CURRENT OF THE OTA'S

2.1 Optimized bias current of a single OTA

In a switched-capacitor circuit, the outputs of the operational transconductance amplifiers have to settle to within a very small fraction of their final values (e_{ss}), depending on the required accuracy of the OTA, in a definite interval called the settling time. The total settling time including the small-signal (t_{ss}) and the large-signal (t_{ls}) settling times should be less than half of the clock period, i.e.

$$t_s = t_{ss} + t_{ls} = T_{clk}/2 - t_{other} \quad (1)$$

where t_{other} is the rest of the half-period for non-overlapping of two clock pulses. While t_{ls} is due to the limited op-amp slew rate, t_{ss} depends on the finite op-amp bandwidth. These two parameters both affect the value of the op-amp current consumption.

Conventionally, these time parameters are predefined statically, e.g. one third of the total settling time is reserved for slewing [5]. Using such an approach one of the settling regimes is dominant in determining the current consumption. However it is shown here that the small- and large-signal settling times can be chosen dynamically so as to have the minimum possible current consumption. The utilized algorithm can be applied to single-stage and two-stage miller-compensated architectures as follows.

For a single-pole op-amp or a two-pole op-amp where the second pole is sufficiently larger than the unity-gain bandwidth, the small- and large-signal settling times are related to the op-amp characteristics as:

$$t_{ls} = \frac{V_{FS}}{SR} \quad \text{and} \quad t_{ss} = n.\tau = n.\frac{1}{2\pi f_{-3dB}} = n.\frac{1}{2\pi.\beta.f_u} \quad (2,3)$$

where V_{FS} is the full-scale signal range, f_{-3dB} the -3-dB bandwidth, β the feedback factor, f_u the unity-gain bandwidth of the op-amp and n the number of the time constants to be spent to achieve a desired accuracy, equal to $\ln(1/e_{ss})$. For a single-stage fully-differential telescopic- or folded-cascode op-amp (Fig. 2), the above-mentioned parameters can be related to the current of the input devices by [6]:

$$t_{ls} = \frac{V_{FS}}{SR} = \frac{V_{FS}}{I_i / C_{load}} \quad \text{and} \quad t_{ss} = n.\frac{1}{\beta g_{mi} / C_{load}} \quad (4,5)$$

where SR is the op-amp slew rate, I_i is the current of the input transistors, g_{mi} is the trans-conductance of the input devices, and C_{load} is the load capacitor at each output node. With the equation expressed above, V_{FS} is the single-ended voltage swing, half of the differential full-scale voltage.

The required current of the input devices required to satisfy the large- and small-signal settling criteria is therefore obtained from:

$$I_i = \frac{V_{FS}.C_{load}}{t_{ls}} \quad \text{and} \quad I_i = n.\frac{V_{eff,i}.C_{load}}{2\beta.t_{ss}} \quad (6,7)$$

where $g_{mi}=2I_i/V_{effi}$ and V_{effi} is chosen as the smallest effective voltage that keeps the input transistors in the strong inversion region and satisfies the other op-amp specifications such as gain. If t_{ls} and t_{ss} are predefined statically [5], I_i should be chosen as the maximum value of the above two, i.e.

$$I_i = \max\left\{\frac{V_{FS}.C_{load}}{t_{ls}}, n.\frac{V_{eff,i}.C_{load}}{2\beta.t_{ss}}\right\} \quad (8)$$

leading to some power being wasted. However, if the two settling contributions are determined dynamically such that the two above terms for the current are equal, some power can be saved. Therefore the optimum value for the bias current of the OTA becomes:

$$I_{OTA,opt} \propto 2I_{i,opt} = 2\frac{V_{FS}.C_{load}}{t_S}.\left(1+\frac{\ln(e_{ss}^{-1}).V_{eff,i}}{2\beta.V_{FS}}\right) \quad (9)$$

where $t_{ls}+t_{ss}=t_S$ (the total settling time). This equation shows the dependency of the optimized current of a telescopic-cascode OTA (or a folded-cascode OTA where the current value of the folded branch is assumed proportional to that of the input branch) on the load capacitor, the settling time and settling error, the full-scale voltage and the feedback factor of the operational amplifier.

2.2 Expansion of the approach to other structures

This relation will be still true even if gain-boosting amplifiers are utilized [7] provided that the current consumption of those amplifiers is proportional to the current of the main OTA. A proportional closed-form formula can also be extracted if two-stage Miller-compensated OTAs are used assuming that the compensation capacitors are chosen equal to the load capacitors and the current values in the second stages of the amplifier are proportional to the currents of the input stages. Such an assumption will be true when either the second stages currents are high enough to satisfy the slewing requirements of the output nodes, or class-A/AB amplifiers are used as the output stages [8].

The current values obtained with this relation are always smaller than what obtained by the conventional methods. This power saving can be sometimes considerably large compared to conventional techniques where settling and slewing times are not optimized.

2.3 The total current of the ADC OTAs

In order to express the total current of the OTAs in the entire ADC versus the ADC parameters, the load capacitors seen by each OTA should be calculated. Fig. 3 shows the m-bit residue amplifier in a pipelined ADC. For an OTA used in the residue stage shown in Fig. 3, the total capacitive load seen by the opamp in the amplifying phase can be obtained from:

$$C_{load} = \frac{(C_S + C_{op})C_F}{C_S + C_{op} + C_F} + C_{next-stage} + C_{comp} + C_{out\_op} \quad (10)$$

where C_F and C_S are the feedback and sampling capacitors of the amplifier and C_{op} is the input parasitic capacitance of the opamp. $C_{next\text{-}stage}$,C_{comp} and C_{out_op} are the input capacitance of the following stage, the input capacitance of the comparators of the following stage sub-ADC, and the output capacitance of the OTA, respectively. It is instructive to note that when the jth residue stage is in its hold mode, the (j+1)th stage is in sampling phase; thus the input capacitor of that stage is obtained from:

$$C_{next-stage,j} = C_{S_{j+1}} + C_{F_{j+1}} = 2^{m_{j+1}} C_{F_{j+1}} \quad (11)$$

reminding that the ratio of the C_S to the C_F of each stage is 2^m-1.

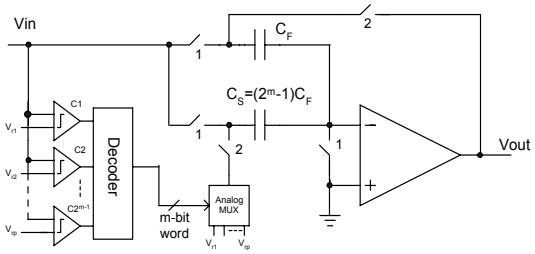

Figure 3. The schematic of the residue stage

Considering the fact that the number of required comparators for an m-bit residue stage is "2^{mj}-1" and for an m_j-effective-bit residue stage with one redundant bit is at least "2^{1+mj}-2", the total load capacitor of the jth OTA assuming bit redundancy is calculated from:

$$C_{load_j} = 2^{m_{j+1}} C_{F_{j+1}} + \frac{(2^{m_j} - 1 + \gamma_j)}{(2^{m_j} + \gamma_j)} C_{F_j} + (2^{1+m_{j+1}} - 2)C_{cu} + C_{out\_op} \quad (12)$$

where C_{cu} is the input capacitor of each comparator and γ_j represents the ratio of C_{op} to C_F. If the output capacitance contribution is regarded as an excess value represented by the excess coefficient ε, the load capacitance can be rewritten as:

$$C_{load_j} = C_{F_j}\left(2^{m_{j+1}} s_j + \left(\frac{2^{m_j} + \gamma_j - 1}{2^{m_j} + \gamma_j}\right)\right)(1+\varepsilon) + (2^{1+m_{j+1}} - 2)C_{cu} \quad (13)$$

where the scaling factor of the jth stage, s_j, is the ratio of the capacitors of the $j+1$th stage and those of the jth stage ; i.e. $s_j = C_{j+1}/C_j$.

In this switched-capacitor amplifier, the feedback factor of the OTA in the amplification phase, can be written as:

$$\beta = \frac{C_F}{C_S + C_F + C_{op}} = \frac{1}{2^m + \gamma} \quad (14)$$

Therefore the total current consumption of the OTAs in the n-stage pipelined converter, using (9) for single-stage amplifiers can be obtained from:

$$I_{OTAs} = \frac{2\alpha V_{FS}}{t_S} \sum_{j=1}^{n^*-1} \left\{ 1 + \frac{\ln(e_{ss_j}^{-1}).V_{eff}(2^{m_j} + \gamma_j)}{2V_{FS}} \right.$$

$$\left. .[C_{F_j}\left(2^{m_{j+1}} s_j + \left(\frac{2^{m_j} + \gamma_j - 1}{2^{m_j} + \gamma_j}\right)\right)(1+\varepsilon_j) + (2^{1+m_{j+1}} - 2)C_{cu}]\right\} \quad (15)$$

$$+ (n - n^*).I_{OTA^*}$$

where α is the correction factor due to the extra current consumption of the peripheral circuits such as the bias circuit. In this equation, n* is the number of the stages in which the capacitor scaling is performed reminding the fact that the scaling stops as soon as the capacitors are determined by the minimum required capacitor matching or the output parasitic capacitances become dominant. The total contribution of the OTAs in the current consumption of the converter is expressed versus the full-scale voltage of the converter, the total settling time (a little smaller than the sampling half-period), the minimum allowed overdrive voltage of the input devices, the unit capacitor of the first stage (C_{F1}), the stage resolutions, scaling factors and finally the input capacitor of the comparators. In the above equation it has been assumed that the comparators used in different stages are all similar. The problem can be easily generalized to a case where different comparators are used for different stages.

Another important consideration is the sample-and-hold (S/H) stage. The current consumption of this stage can be calculated in a similar fashion with a resolution of m equal to zero. Just the feedback factor of the OTA in the S/H amplifier should be corrected due to the architecture utilized. For example for a flip-around SHA architecture the feedback factor is smaller than unity calculated form (14).

The total power consumption of the converter excluding the power dissipated in the reference buffers and the digital error correction and calibration blocks, can thus be obtained from (15) plus the current consumption of the comparators, i.e. $\sum_{j=1}^{n} (2^{1+m_j} - 2).I_{cu}$ where I_{cu} is the current consumption of a single comparator and m_j is the number of *effective* bits resolved by the jth stage. Note that the power dissipated in the OTAs and the comparators is the major part of the total power consumption of the ADC [2].

3. NOISE CALCULATIONS

3.1 Input-referred noise of a residue stage

The input-referred thermal noise of a switched-capacitor amplifier has two main sources, the on-resistance of the switches and the operational amplifiers. It can be shown that the input-referred noise due to switches in the switched-capacitor amplifier of Fig. 3 is obtained from [8]:

$$\overline{v}_{ni,sw}^2 = 2kT \frac{C_S + C_F + C_{op}}{(C_S + C_F)^2} \quad (16)$$

Reminding that in an m-effective-bit residue stage $(C_S+C_F)/C_F = 2^m$ and the ratio of C_{op} to C_F is represented by γ then (16) can be rewritten as:

$$\bar{v}_{ni,sw}^2 = \frac{2kT}{C_F}.(2^{-m} + \gamma 2^{-2m}) \quad (17)$$

Besides, the input-referred thermal noise of a switched-capacitor amplifier due to the operational amplifiers thermal noise is dependent on the OTA architecture. With a fully-differential single-stage OTA, the input-referred thermal noise of the residue-amplifier due to the OTA noise can be obtained from [9]:

$$\bar{v}_{ni,op}^2 = 2 \cdot 4kT \cdot R_{noise} \cdot F \cdot BW_{eq} \frac{1}{\beta^2}\left(\frac{C_F}{C_S + C_F}\right)^2 \quad (18)$$

In this equation F is the architecture-dependent excess noise factor due to the non-input devices of the OTA. As an instance, in the folded-cascode configuration of Fig. 2-b this factor is calculated from:

$$F = 1 + \frac{g_{m2}}{g_{m1}} + \frac{g_{m5}}{g_{m1}} \quad (19)$$

For a single-pole OTA or a two-pole structure where the second pole is sufficiently larger than the unity-gain frequency, the equivalent bandwidth can be obviously obtained from:

$$BW_{eq} = \frac{\pi}{2} \times \frac{g_{m1}}{2\pi C_{load}} \times \beta \quad (20)$$

and $R_{noise}=2/3g_{m1}$. Therefore the input-referred thermal noise of the residue amplifier due to the OTA noise, can be expressed as:

$$\bar{v}_{ni,op}^2 = \frac{4}{3} F \frac{kT}{C_{load}}.(2^{-m} + \gamma 2^{-2m}) \quad (21)$$

Hence, the total input-referred noise of the switched-capacitor residue amplifier can be calculated from:

$$\bar{v}_{ni,residue}^2 = \left(\frac{4}{3} F \frac{kT}{C_{load}} + 2\frac{kT}{C_F}\right)\left(2^{-m} + \gamma 2^{-2m}\right) \quad (22)$$

The same equation can be derived for a two-stage miller-compensated OTA if the compensation capacitor is chosen equal to the load capacitor.

3.2 Input-referred noise of the total ADC

In a pipelined A/D converter, the noise power of any stage when referred to the input is divided by the power gains of the preceding stages. Since the voltage gain of the ith residue amplifier, G_i, is equal to 2^{mi} , the total input referred noise of the converter can be expressed as:

$$\bar{v}_{ni,t}^2 = \bar{v}_{n_1}^2 + \frac{\bar{v}_{n_2}^2}{G_1^2} + \frac{\bar{v}_{n_3}^2}{G_1^2.G_2^2} + \frac{\bar{v}_{n_4}^2}{G_1^2.G_2^2.G_3^2} + \ldots$$
$$= \sum_{j=1}^{n} \frac{\bar{v}_{n_j}^2}{\prod_{i=1}^{j-1} G_i^2} = \sum_{j=1}^{n} \frac{\bar{v}_{n_j}^2}{\prod_{i=1}^{j-1} 2^{2m_i}} = \sum_{j=1}^{n} \frac{\bar{v}_{n_j}^2}{2^{2\sum_{i=1}^{j-1} m_i}} \quad (23)$$

The total input-referred noise of the converter will be therefore calculated as:

$$\bar{v}_{ni,t}^2 = kT \sum_{j=1}^{n} \frac{\left(\frac{4}{3}\frac{F}{C_{load,j}} + \frac{2}{C_{F,j}}\right)\left(2^{-m,j} + \gamma_j 2^{-2m,j}\right)}{2^{2\sum_{i=1}^{j-1} m_i}} \quad (24)$$

Making use of the relation derived for the load capacitor of the jth stage, the above equation can be simply expressed versus the values of the capacitors and the resolutions of stages when the OTA configuration and therefore an estimation for the excess noise factor F is known. When optimizing, the modification parameters of ε_j and γ_j are primitively defined and then corrected in a few iterations.

4. OPTIMIZATION METHODOLOGY

4.1 Design procedure

In the previous sections, closed-form equations for the total input-referred noise and the optimized current consumption were extracted as functions of the ADC capacitors and the resolutions of the stages. Using MATLAB, a simple optimization CAD tool has been developed by the authors to implement an optimization problem of the form:

Find the optimum values of the capacitors and the resolutions of different stages, in order to minimize the total power consumption of the ADC, while the total input-referred noise requirement is satisfied.

The main parameters of the sub-blocks of the converter including the capacitor values and the resolutions of different stages are *simultaneously* optimized while no limiting assumption is imposed. It is only assumed here that the front-end stages are all calibrated in order to meet the required accuracy of high-resolution converters. Note that the calibration circuitry has usually a negligible effect on the total power dissipation of the converter. For the rms value of the required input-referred thermal noise voltage one choice, employed here, is an equal value with the quantization noise voltage calculated from

$$\sqrt{\bar{v}_{ni_q}^2} = \frac{V_{LSB}}{\sqrt{12}} = \frac{2V_{ref}}{2^N\sqrt{12}} \quad (25)$$

This choice will lead to 3dB degradation in the value of SNR of the ideal ADC. Note that the signal-to-noise ratio is obtained from:

$$SNR = 10\log_{10}\left(\frac{V_{ref}^2/2}{\bar{v}_{ni_q}^2 + \bar{v}_{ni_{th}}^2}\right) \quad (26)$$

where V_{ref}, the reference voltage, is equal to the single-ended full-scale voltage swing. By using bit redundancy the maximum comparator offset is permitted to be:

$$V_{offset} \le \frac{V_{ref}}{2^{m+1}} \quad (27)$$

where m is again the effective number of bits resolved by the stage. Since the comparator offset must always meet the above relation, after choosing a specific architecture for the comparators, depending on the maximum input offset, the maximum allowed resolution of the residue stages is determined.

The input parameters for tha CAD tool including N (the resolution of the converter), V_{ref}, C_{min} (the minimum required value to satisfy a specified matching behavior dependent on the fabrication process), C_{cu} (the input capacitance of a single comparator), I_{cu} (the current dissipation of a single comparator), m_{max} (the maximum permitted value for the resolution of a residue stage

determined due to the maximum offset of the comparator), $\vec{\gamma}$ (the vector of γ_i's), $\vec{\varepsilon}$ (the vector of ε_i's), F (the excess noise factor dependent on the opamp architecture), and V_{eff} (the minimum value for the overdrive voltage of the input devices) should be initially determined for the optimization tool. The optimization tool will determine the optimum values for all capacitors, C_F's, and the stage resolutions and also the optimum values for the bias currents of the stages. The input transistors are then optimally sized using the optimum values for the currents and the overdrive voltages (V_{eff}). It should be mentioned that some of the input parameters such as the parameters of the comparators and if permitted the reference voltage can be even optimally chosen using the methodology presented here. Since the values of $\vec{\gamma}$, $\vec{\varepsilon}$ and F were just the initial estimations, a few iterations accompanied with circuit simulations are required to modify the optimized values of the parameters.

4.2 Design Examples

In order to illustrate the effectiveness of this methodology, a few high-resolution examples are presented and compared with conventional designs here.

Consider a 12-bit 3.3-V 50M-Samples/sec pipeline ADC. With a full-scale voltage swing of $2V_{p\text{-}p,diff}$ (i.e. V_{ref}=1V) that can be conveniently realized using single-stage telescopic-cascode opamps, the least-significant-bit (LSB) value is $2/2^{12}$=488μV and the optimization program suggests a resolution distribution of [3 2 1 1 1 1 1 2]. Note that the mentioned resolutions are the effective number of bits and one redundant bit is generated in all stages. The last stage only consists of three comparators to form a 2-bit flash ADC [9]. It is assumed here that the required DC gain of more than 72dB=2^{12} for the first residue-stage operational amplifier can be realized with such opamp configuration which is verified by HSPICE simulation results using BSIM3v3 model parameters of a 0.25μm CMOS process. Circuit simulations also verified the settling behavior of the opamps. Assuming that the minimum allowed capacitance to meet the matching requirements is equal to 0.1pF, the feedback capacitors of different stages are suggested as [0.5p 0.1p 0.1p … 0.1p]. The sampling capacitors are chosen according to the required resolutions. In this problem the current consumption of a single comparator with a dynamic structure is assumed equal to 100uA.

Using the proposed approach, the total current consumption of the opamps (including the current consumption of their bias circuits) and the comparators of the converter is estimated to be 14mA. If the converter was conventionally designed using 1.5-bit residue stages such that the noise contribution allocated to each stage is half of the previous one while the contribution of the first stage is half of the total input-referred noise [10], then the scaling factors of all stages should be chosen equal to 0.5 using identical comparators, and to achieve similar SNR with the previous example, the feedback capacitors of the stages would be [10p, 5p, 2.5p, 1.25p, 0.625p, …, 0.1p] and the total current consumption of the OTAs and the comparators would be larger than 35mA! If the resolution of the first stage is chosen equal to 2 effective bits and all the following stages resolve 1.5 bits, the total current consumption with the same scaling factors (i.e. 0.5) will become 25mA, again much larger than the optimized value. These specifications were derived assuming no dedicated S/H stages used in the front-end provided that the input signal changes less than one LSB voltage of the first stage between the sampling instance of the residue amplifier and the decision time of the sub-ADC comparators. However, if a dedicated S/H stage is to be used, the resolutions of the stages for the previous example changes to [0 3 2 2 1 … 1 2] while the capacitor values will be as what depicted in Fig. 4 changing from 4.2pF for the S/H stage to 0.5pF for the second stage and 0.1pF for the remaining stages. Fig. 4 shows the current consumption of the OTA and the comparators of different stages for two cases with and without the S/H front-end stage. It can be seen that if the front-end S/H amplifier is allowed to be omitted [11], considerable amount of power will be saved. For converters with resolutions of not larger than 10, the optimization CAD tool suggests a resolution of 1 effective bit (i.e. 1.5 bits) for all stages. This is exactly the same as what proposed by Lewis [1] nevertheless the capacitor values are optimized here. The developed tool can be used not only to optimize an ADC but also to calculate the power consumption of arbitrary design cases with specific values for the resolutions, the capacitor values, the full-scale voltages, the comparator power dissipations or the OTA noise excess factors. For example consider a 12-bit converter with a supply voltage of 2.5V. The designer can choose the maximum allowed number of bits per stages, m_{max}, equal to 5 provided that low-offset power-hungry comparators are utilized instead of dynamic structures with usually higher offset voltages but with m_{max} of 3.

As another example, consider an ADC where the full-scale (reference) voltage can be chosen by the designer (and is not governed by the total system specifications). With a specific supply voltage the optimization program can easily help the designer to choose a two-stage opamp architecture (with higher power and probably higher excess noise factor (F)) with a larger full-scale voltage swing or a single-stage configuration with smaller power dissipation for the opamps but with a smaller V_{FS} (of course provided that both opamps are able to meet the required speed).

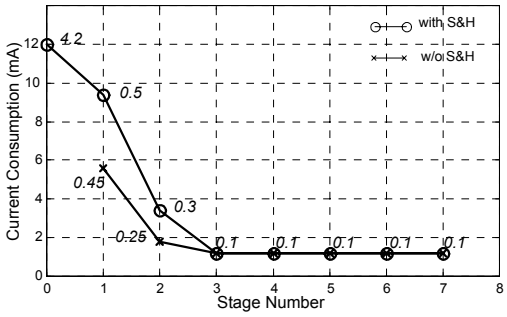

Figure 4. The values of the current consumptions and the capacitors of the stages (with and without the dedicated SHA)

4.3 Power dependency on the ADC specifications

Using the developed CAD tool the dependency of the total current consumption of the ADC on the overall resolution and also the full-scale voltage swing can be conveniently investigated. Fig. 5 shows the current consumption of the 50M-Samples/s converter verses its resolution when dedicated sample-and-hold front-end

stages are used. It can be observed that by adding one bit to the overall resolution, the current consumption is increased with a higher rate in higher resolutions. This is mainly due to the fact that in low resolutions the capacitor values are mainly determined by the required matching rather than the *kT*/*C* noise. However at higher resolutions the thermal noise determines the capacitor values. When the resolution is increased by a single bit, the magnitude of the LSB voltage is halved and the thermal noise power should become one fourth. Thus the capacitor values are to become four times larger. From (15) it can be concluded that the OTA contributions in the total current consumption becomes approximately four times larger however the number of comparators is not multiplied by four. Hence the total current is increased by a factor less than four. The dependency of the power dissipation on the full-scale voltage can be also investigated as shown in Fig. 6 for a 12-bit 50MS/s example. It can be seen that if the full-scale voltage is halved, the current consumption is increased by a factor of more than two. This behavior can be clearly predicted from the optimized value for the current consumption given by (9) keeping in mind the dependency of C_{load} on the full-scale voltage. Therefore the *power* consumption of the ADC increases by scaling down the voltage.

4.4 The non-ideal frequency response

The optimized value for the current consumption of a single-stage OTA or a two-stage Miller-compensated OTA, was obtained assuming that the second pole frequency is larger than the unity-gain frequency of the amplifier not to degrade the frequency response. However it is obvious that this assumption is not always the case when the non-dominant poles are not large enough to be neglected. This fact affects not only the settling behavior but also the thermal noise equivalent bandwidth of the OTA. This non-ideal settling time can be shown to be smaller than what predicted by (3), therefore the problem has been overestimated here. The noise behavior is overestimated as well since the noise equivalent bandwidth of the OTA is smaller than what predicted by (20) if the second pole is not located much higher than the unity-gain frequency.

5. CONCLUSIONS

In this paper based on a novel approach to design the operational amplifier in a switched-capacitor circuit, a closed-form equation for the total optimized current of a pipelined ADC is presented. Besides, considering the noise sources in a residue-amplifier, a closed-form relation for the total input-referred thermal noise of the ADC is derived as well. Based on the developed equations an efficient design methodology for pipelined A/D converters is developed. The proposed approach can simultaneously determine the capacitor values and the resolutions of the residue stages of the converters with no limiting assumption. Design examples are presented to verify the effectiveness and the generality of the proposed methodology. It has been shown that the developed CAD tool can be even employed to decide about the architecture of the comparators or the optimum value for the reference voltage. The dependency of the current dissipation of the ADC on some of the converter specifications has been investigated as well to illustrate the usefulness of the presented equations.

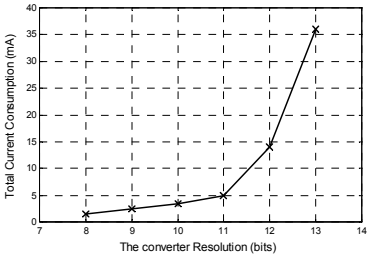

Figure 5. Dependency of the optimized current consumption of the 50MS/s converter on the resolution

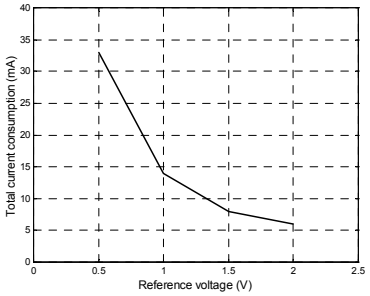

Figure 6. Dependency of the optimized current consumption of the 12-bit 50MS/s converter on the full-scale voltage swing

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