Low Power Startup Circuits for Voltage and Current Reference with Zero Steady State Current

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ABSTRACT
A class of new startup circuits for Voltage and Current Reference circuits are proposed. Unlike conventional startup circuits, the proposed circuits completely turn off once the reference circuit is started and consume no current during normal operation of the reference circuits. The circuits employ feedback from the reference circuit to ensure that the reference circuit has reached its desired operating state prior to shutting themselves off. The proposed circuits are quite useful in low power integrated circuit design. Very low startup time can be achieved. The circuits are generic in nature and can be used with any reference circuit such as bandgap voltage reference, ΔVgs/R circuit, etc.

Categories and Subject Descriptors
B.7.0 [**Integrated Circuits**]: General.

General Terms
Design

Keywords
Voltage Reference, Current Reference, Low Power Integrated Circuits, Startup Circuit.

1. INTRODUCTION
A startup circuit plays a very significant role in voltage and current reference circuits. The startup circuit brings out the reference circuit from a dead (zero current) operating point to its normal operating point and then is no longer used once the reference circuit starts operating properly. A conventional startup circuit [1-4] continues to consume constant current even after giving startup and thus increases the total power consumption of the circuit. This power can be significant when multiple numbers of bias generator circuits are employed in a single chip, consequently reducing battery life.

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The proposed startup circuits overcome the above drawback as they turn off completely once the current reference circuit starts operating properly.

2. CIRCUIT DESCRIPTION
Two different categories of startup circuits are presented, one works with a power down signal and the other with VDD ramp-up. Both categories present two different topologies and further they could be combined to realize a common startup circuit, which can be used to start the reference circuits with both a power down signal and VDD ramp-up.

2.1 Startup circuit with power down signal
Figures 1 and 2 are schematic diagrams of startup circuits designed to work with a power down signal. The Power Down (PWD) signal is used to keep the current or voltage reference circuits in idle or reset mode. When the power down signal is asserted, as shown in Figure 6, nodes PBIAS and NBIAS are pulled to VDD and VSS respectively and hence no current flows into the reference circuit. The circuit should return to its normal operation when the PWD signal is de-asserted but it doesn't happen because there is no path to discharge the node PBIAS or charge the node NBIAS. A startup circuit is needed to either charge the node NBIAS or discharge the node PBIAS, which initiates a current into the reference circuit until the circuit settles to its normal operating point.

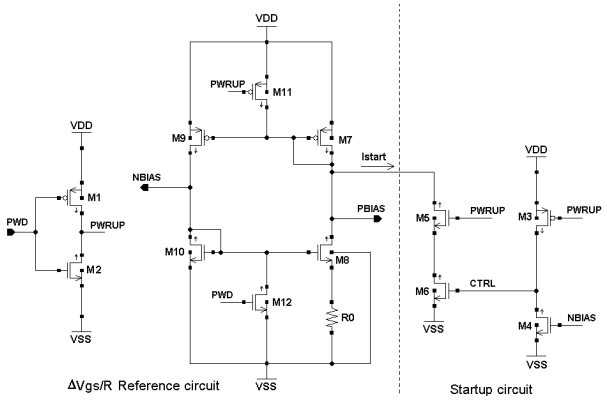

Figure 1. Startup Circuit for reference generator with PWD signal

Consider the circuit in Figure 1, the startup circuit comprises pmos M3 and nmos M4, M5 and M6. When the PWD signal is asserted, M5 is off and M3 pulls node CTRL to VDD, which turns on M6. Since M6 is in series with M5, the startup current Istart will be zero. The nodes PBIAS and NBIAS will be at VDD and VSS respectively. There will be no current in the reference circuit and M4 will be off. Now when the PWD signal is de-asserted, M3 is turned off and M5 is turned on. Since NBIAS is at VSS, M4 will remain off, and node CTRL will remain at VDD. This will cause M6 to remain on. A small capacitor of few hundred femto farads can also be added at node CTRL in order to avoid the possibility of getting it discharged due to any leakage current. Now both M5 and M6 are on and hence current Istart starts flowing from the node PBIAS, which will start discharging the node PBIAS from VDD towards VSS. This initiates a flow of current in M7 and M9. The flow of current in M9 will start charging the node NBIAS from VSS towards VDD causing a current flow in M8 and M10. As the voltage NBIAS reaches a value greater than V_T(M4), M4 is turned on and pulls node CTRL to VSS, hence turning off M6, which shuts off Istart. The value of Istart depends upon the size of M6, which can be adjusted according to the required startup time.

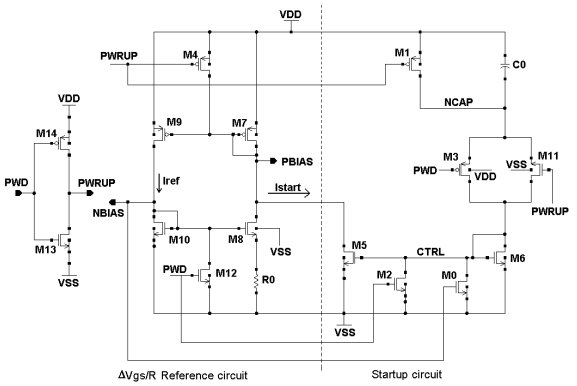

Figure 2. Startup Circuit with capacitor for reference generator with PWD signal

Now consider the circuit shown in Figure 2. The startup circuit includes pmos M1, M3, nmos M0, M2, M5, M6, M11 and a capacitor C0. M3 and M11 constitute a transmission gate. As the PWD signal is asserted, node NCAP and PBIAS are pulled to VDD, NBIAS is pulled to VSS and transmission gate is off. Since NBIAS is at VSS, M0 is switched off. To start the reference circuit, PWD is de-asserted, which makes M4 and M12 go off and the transmission gate starts charging the node CTRL towards VDD. The rate of charging of node CTRL depends upon the RC time constant of the circuit composed of C0 and the transmission gate. As node CTRL goes above V_T(M6), it turns ON and provides a path to the charge from node NCAP to flow to VSS. Thus a startup current Istart starts flowing through M6, which is mirrored in M5. Istart starts pulling the node PBIAS towards VSS which initiates a current to flow through transistors M7 and M9, which ultimately stabilize Iref to its desired value. With Iref established, NBIAS attains its desired value, which turns on M0. This brings node CTRL to VSS and M5 and M6 turn off. Thus, the startup circuit is disconnected from the reference circuit and no current flows through it. It may happen that when the reference circuit is off, node CTRL may accumulate some charge due to leakage currents. This may create a leakage current path from VDD to VSS through M4 and M5. To avoid this, M2 has been connected between nodes CTRL and VSS and goes on when the reference circuit is off. M2 discharges node CTRL to VSS and no charge can buildup at node CTRL, which prevents any leakage current from flowing between VDD and VSS.

2.2 Startup circuit with VDD ramp-up

Figures 3 and 4 are schematic diagrams of startup circuits designed to work with VDD ramp-up. When the power is turned on and starts ramping up towards VDD, the reference circuit may not start because node PBIAS continues to follow VDD, causing zero Vgs for M7 and M9, as shown in Figure 9. This happens because the practical values of parasitic resistors Rpar1 and Rpar2 are not infinite.

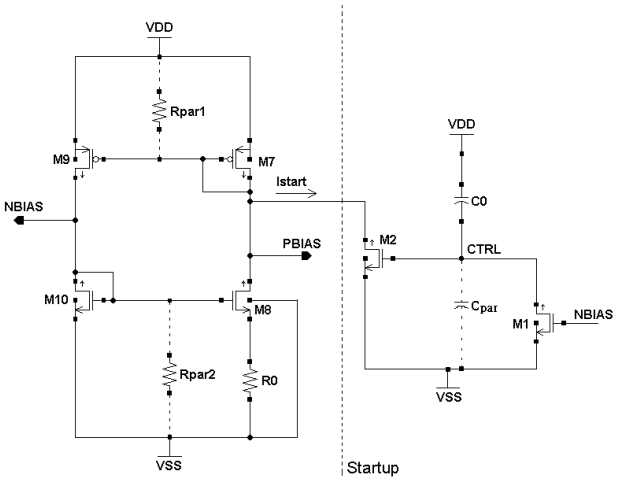

Figure 3. Startup Circuit with VDD ramp-up

Consider the circuit in Figure 3, which includes two nmos transistors M1, M2 and a capacitor C0. When VDD is ramping up from 0V, node CTRL follows to VDD to maintain zero potential across capacitor C0. The parasitic capacitance (Cpar) between node CTRL and VSS will form a voltage divider with C0. The voltage at CTRL may be written as:

$$VCTRL = VDD.C0/(C0+Cpar)$$

Normally Cpar is very low so C0 could be taken in the range of 0.5pf – 1.0pf then $VCTRL \cong VDD$.

Hence M2 will go ON as VDD rises, which will generate a startup current Istart in M2 that will start discharging node PBIAS towards VSS and the reference circuit will start. As the current starts flowing in the current reference circuit, NBIAS will start charging from VSS towards VDD and as it crosses V_T(M1), it will turn ON and node CTRL will be pulled down to VSS, which will turn off M2. Thus, the startup circuit will be disconnected from the reference circuit and no current flows through it.

Consider the circuit shown in Figure 4. The startup circuit includes of nmos M5, pmos M4, M6 and capacitor C0.

Initially, when VDD is zero, both PBIAS and NBIAS, along with node CAP will be zero and no current will flow through the circuit. As VDD starts ramping up, PBIAS also starts increasing and follows VDD. As VDD exceeds V_T(M5), M5 starts charging node CAP slowly with a time constant that depends upon the channel resistance (Rds) of M5 and the value of the capacitor C0. Since the rate of charging of C0 will be less than the rate of increase in VDD, the gate to source voltage of M6 starts increasing. As the difference between the gate and the source of M6 increases by more than V_T(M6), M6 goes on and a startup current (Istart) starts pulling NBIAS towards VDD. Thus, a voltage is developed across resistance R0 and current starts flowing through R0. The flow of current in R0 starts discharging PBIAS and it no longer follows VDD. Thus, the gate to source voltage of M7 and M9 increases and they start conducting. M5, being diode connected, can charge C0 to a maximum voltage of (VDD – Vtn), which keeps M6 ON and current Istart flowing. As VDD reaches its stable value, the current through M7, M9 and M8, and M10 stabilizes at its required value and PBIAS and NBIAS attain their stable values. This makes M4 go on, which pulls node CAP to VDD, and turns both M5 and M6 off. Thus, when the reference circuit settles at its desired operating state, the startup circuit goes off and consumes no DC current.

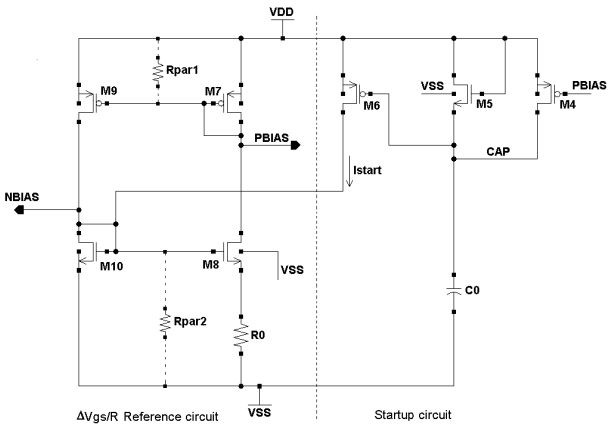

Figure 4. Startup Circuit with VDD ramp-up

In the previously proposed startup circuit with VDD ramp-up [4], the feedback from NBIAS is given to the input of an inverter to turn off the startup so it would become dependent of inverter threshold, which may fail to trip at some process corners unless its threshold is kept lower than NBIAS, which is quite difficult.

The two circuits in Figure 1 and Figure 3 can be combined to form a startup circuit (Figure 5) that can be used with both power down as well as VDD ramp-up.

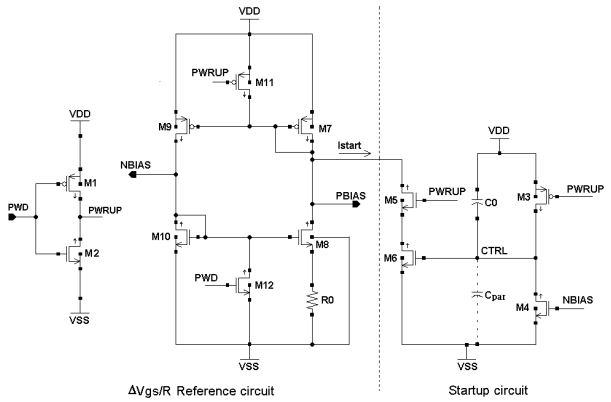

Figure 5. Startup Circuit with VDD ramp-up and PWD

3. SIMULATION RESULTS

All the proposed circuits were designed in 0.1u CMOS technology and simulations have been carried out in SPICE. The **ΔVgs/R** current reference shown with the proposed circuits has been taken as an example for simulation purpose. All the proposed startup circuits are generic and can be used in any application that needs startup circuit. The simulation waveforms of the proposed circuits have been shown in Figures. 7, 8, 10 and 11. Figures. 6 and 9 show the simulation results of **ΔVgs/R** circuit with PWD signal and VDD ramp up without a startup circuit.

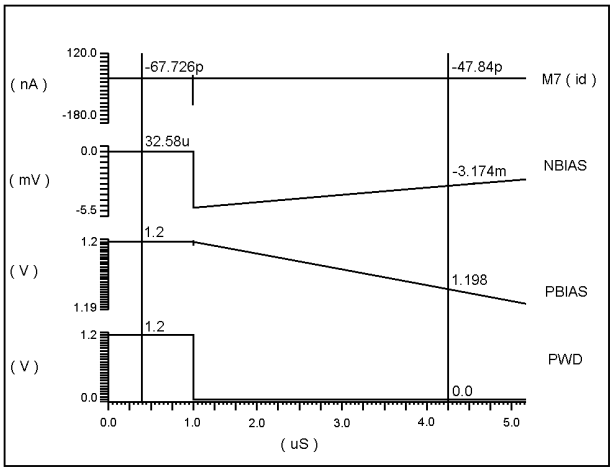

Figure 6. Simulation results of the current reference using power down (PWD) signal without startup circuit

The above waveforms show the results of current reference without startup circuit when a Power Down Signal is used. It is clear from the waveforms that the reference circuit does not start (no current through M7) even when the PWD signal is de-asserted.

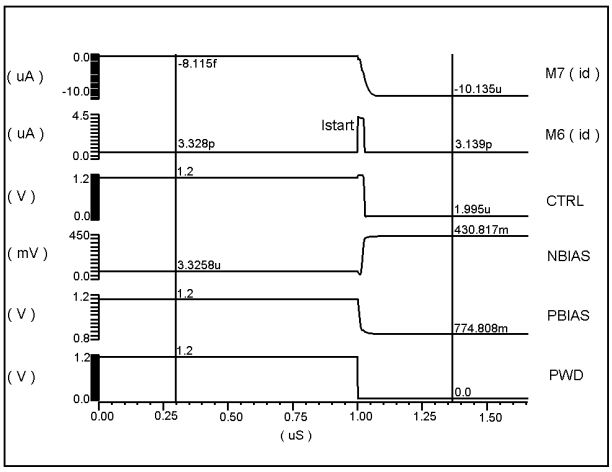

Figure 7. Simulation waveforms for the circuit in Figure 1

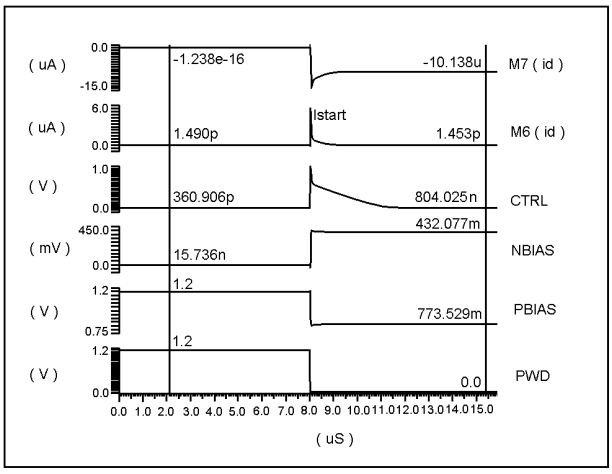

Figure 8. Simulation waveforms for the circuit in Figure 2

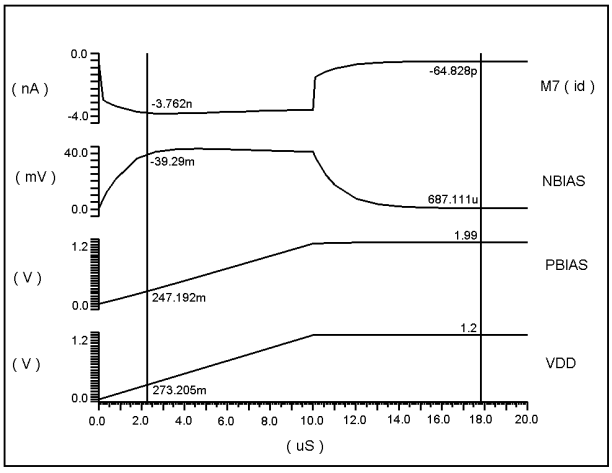

Figure 9. Simulation results of the current reference with VDD ramp up without startup circuit

Figure 9. shows the results of current reference with VDD ramp-up without a startup circuit. It is clear from the waveforms that the reference circuit does not start when VDD is ramping up.

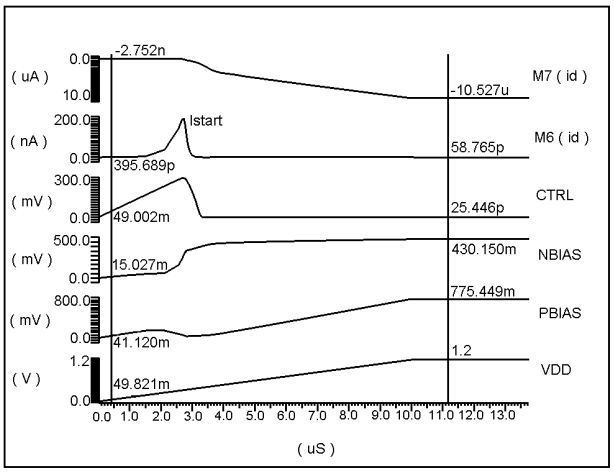

Figure 10. Simulation waveforms for the circuit in Figure 3

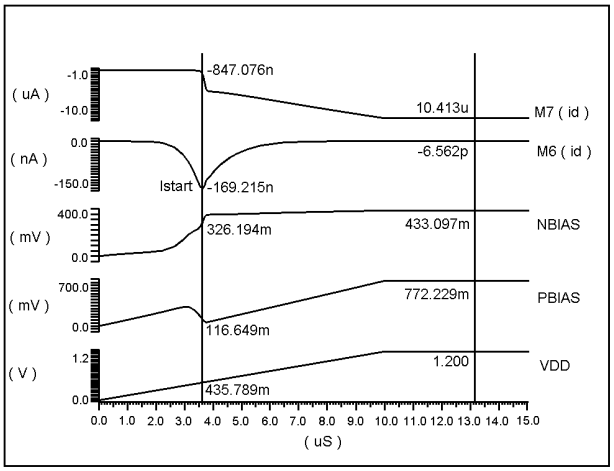

Figure 11. Simulation waveforms for the circuit in Figure 4

4. COMPARISION WITH CONVENTIONAL STARTUP CIRCUIT

The proposed startup circuits were compared with a conventional startup circuit as shown in Figure 12. The startup circuit has pmos M1 and nmos M0, M5 and M6. Cb represents the bypass capacitance that is used to reduce the effect of noise and to stabilize the bias voltage. Figure 13 shows the simulation results of the circuit. After the current reference settles at its required operating state, M0 goes on and a constant current starts flowing through M0 and M1. Thus, the conventional startup circuit continues to consume current even after the current reference circuit is started. The value of this consumed current depends upon the startup time required. For a low startup time, high current is required causing extra power consumption in the circuit. As is clear from Figure 13, for Cb=2pF and for 0.1us startup time for the current reference, the constant current which flows in M0 is 28.7uA, which is very high for low power circuits.

Figure 14 shows the simulation results of the circuit shown in Figure 1 with a capacitor Cb=2pF added between nodes VDD and PBIAS. It is clear from Figure 14 that current Istart becomes zero when the circuit settles at its required operating condition and thus consumes no dc current. This can also be concluded for the other proposed circuits as well.

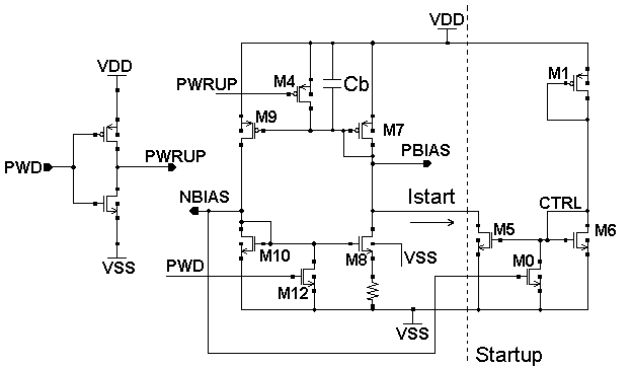

Figure 12. A conventional startup circuit

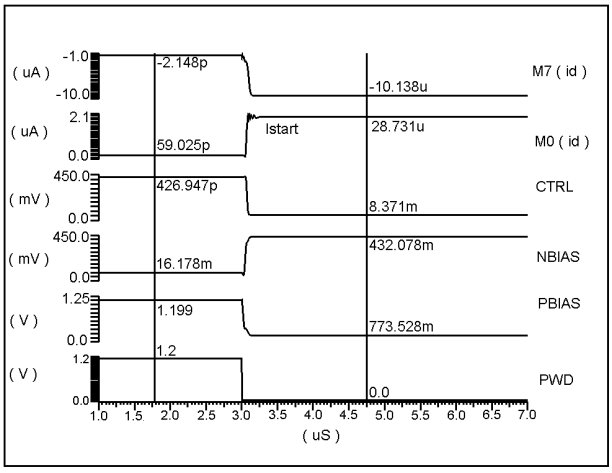

Figure 13. Simulation waveforms for the circuit in Figure 12

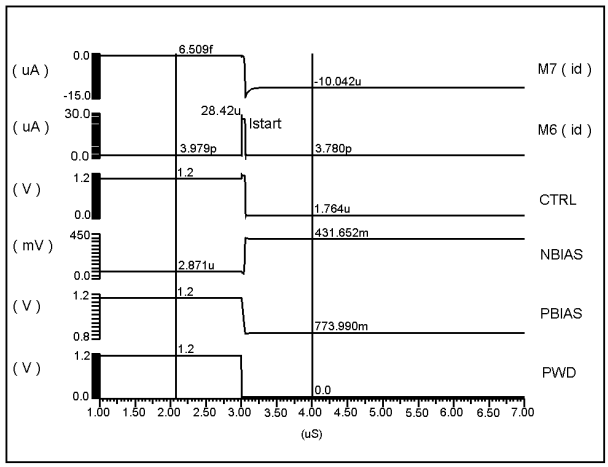

Figure 14. Simulation waveforms for the circuit in Figure 1 with 2pF capacitor between VDD and PBIAS

5. CONCLUSION

Low power startup circuits with zero steady state current have been proposed. Unlike conventional startup circuits, the proposed circuits are completely turned OFF once the Voltage/Current reference is started. Since the proposed circuits consume no steady state current in the normal operation of the reference circuits, a very low startup time is achieved with low power consumption. The circuits are generic in nature and can be used with any kind of voltage or current reference circuits that need startup circuit.

6. REFERENCES

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