Strained-Si Devices and Circuits for Low-Power Applications

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ABSTRACT
Static and dynamic power for strained-Si device is analyzed and compared with conventional bulk-Si technology. Optimum device design points are suggested with controlling physical/structural device parameters. Strained-Si CMOS circuits are studied, showing substantially-reduced power consumptions due to unique advantageous features of strained-Si device. The trade-offs for power and performance in strained-Si devices/circuits are discussed. Further, analysis and low-power design points are applied and extended to strained Si on SOI substrate (SSOI) CMOS technology.

Categories and Subject Descriptors
B.7.1 [**Hardware**]: Integrated Circuits–*Types and Design Style*

General Terms
Design, Theory, Verification

Keywords
Strained-Si MOSFET, SOI, SiGe, Mobility, Band offset

1. INTRODUCTION
Because of higher carrier mobility with preservation of conventional CMOS device structure and geometry, strained-Si (SS) MOSFETs are recently of much interest for high-performance circuit applications [1], [2]. The higher mobility stems from lattice mismatch between the Si channel and the relaxed SiGe layers, which reduces the conductivity effective mass and the intervalley scattering [1], [3]. Due to the speed advantage, SS devices could be applied to low-power circuit by lowering supply voltage, one of the most effective ways for low-power circuit design. Other important physical property for SS device is heterostructural band offset, which significantly reduces threshold voltage V_t [1] and must be accurately accounted for.

In this paper, we discuss low-power SS device/circuit applicability, analysis, and design points. Low-V_t bulk-Si device is compared with SS device with equal V_t (off-state current I_{off}). Typical CMOS circuits with SS device are analyzed. Power dependencies upon key SS device factors are discussed, and strained Si on SOI substrate (SSOI) device/circuit is addressed for low-power applications to attain the additional power savings with SS devices.

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2. STRAINED-SI DEVICE FEATURES
The CMOS device/circuit performance and power are mainly determined by the on-state current I_{on} and off-state current I_{off}, which could be physically written as

$$I_{on} = WC_{G(eff)}(V_{DD} - V_t)v_S \quad (1)$$

where W is the MOSFET width, $C_{G(eff)}$ ($< \varepsilon_{ox}/t_{ox}$ where ε_{ox} and t_{ox} are the gate-oxide permittivity and thickness, respectively) is the effective gate capacitance, and v_S is the average carrier (diffusion) velocity near the source [4], [5], and

$$I_{off} = I_O 10^{-(V_{t(low)} - \Delta V_{t(DIBL)})/S} \quad (2)$$

where I_O is the drain current when the gate-to-source voltage V_{GS} is equal to V_t, $V_{t(low)}$ is the threshold voltage at low V_{DS}, $\Delta V_{t(DIBL)}$ is V_t reduction due to the drain-induced barrier lowering (DIBL), and S is the subthreshold swing [6]. From (1) and (2), we can know that V_t, S, and DIBL are the key device factors for I_{on} (or performance) and I_{off} (or standby leakage power). We describe physical closed-form expressions for these three factors in SS device with only process-related parameters. Note that higher carrier mobility in SS device enhances v_S in (1), thereby increasing I_{on}.

The V_t for the strained-Si nMOSFET is written from classical theory:

$$V_t = \Phi_{MS} + \psi_s - Q_d/C_{ox} \quad (3)$$

for negligible oxide charge and fast surface states where Φ_{MS} is the gate-body work-function difference, ψ_s is the (pinned) surface potential (at the strong inversion), Q_d is the depletion charge density, and C_{ox} is the gate-oxide capacitance [6]. In SS device, Φ_{MS} and ψ_s are lower due to the band offset, and the band gap of SS device could be described as

$$E_{g(SS)} \cong E_{g(Si_{1-x}Ge_x)} \cong E_{g(Si)} - (E_{g(Si)} - E_{g(Ge)})x \quad (4)$$

from the linear interpolation where $E_{g(Si)}$ and $E_{g(Ge)}$ are the band gaps in Si and Ge, respectively, and x is the Ge content in the relaxed $Si_{1-x}Ge_x$ layer of SS device: $0 \le x \le 1$. For 20% Ge-implanted (x = 0.2) scaled SS nMOSFET, V_t could be ~200 mV lower [3], which increases I_{off} by more than two orders of magnitude for typical S = 70-100 mV. Note that V_t for strained-Si on SOI (SSOI) would be comparable at low V_{DS} but much lower at high V_{DS} due to the floating-body effect [1].

The subthreshold swing (S) for the strained-Si (SS) device is written as

$$S \cong (60mV)\left(1 + \frac{\varepsilon_{Si_{1-x}Ge_x}}{\varepsilon_{ox}} \cdot \frac{t_{ox}}{t_d}\right) \quad (5)$$

where ε_{ox} and $\varepsilon_{Si_{1-x}Ge_x}$ are the permittivities of the gate oxide and relaxed $Si_{1-x}Ge_x$ layer of SS device, respectively, and t_d is the depletion width in SS device. Although t_d could be derived by solving one-dimensional Poisson's equation with the boundary conditions [7], it can be intuitively described as

$$t_d \cong \sqrt{2\varepsilon_{Si_{1-x}Ge_x}\psi_s/(qN_{Si_{1-x}Ge_x})} \quad (6)$$

from the depletion approximation where $N_{Si_{1-x}Ge_x}$ is the body-doping density in the relaxed $Si_{1-x}Ge_x$ layer. Note that the dielectric constant of the strained-Si layer could not be too much different from that of the SiGe layer in the full relaxation. For 20% Ge content, SS device could have ~7.5% higher dielectric constant based on the linear interpolation:

$$\varepsilon_{Si_{1-x}Ge_x} \cong \varepsilon_{Si} + (\varepsilon_{Ge} - \varepsilon_{Si})x \quad (7)$$

where ε_{Si} and ε_{Ge} are the permittivities of Si and Ge, respectively. However, t_d of SS device is not too much different from that of bulk-Si device due to the lower ψ_s in (6), which tends to compensate for the higher dielectric constant. For scaled t_{ox} ($<< t_d$), S could be almost the same for Si and SS MOSFETs.

The DIBL model is derived by solving the two-dimensional Laplace's equation with Gauss's law and physical approximations [8]. For bulk-SS device, the DIBL could be expressed as

$$DIBL \cong \frac{3t_d t_{ox} V_{DS}}{L_{eff}^2\left(1 + \frac{\varepsilon_{Si_{1-x}Ge_x}}{\varepsilon_{ox}} \cdot \frac{t_{ox}}{t_d}\right)} \quad (8)$$

where t_d is the depletion width described in (6) and L_{eff} is the effective channel length. From (8), DIBL could be different between Si and SS devices. However, DIBL-induced V_t shift, $\Delta V_{t(DIBL)}$ could not be too much different based on (5) and (8) since $\Delta V_{t(DIBL)}$ = DIBL*(S/60).

3. STRAINED-SI CMOS INVERTER

To study the strained-Si (SS) device advantage of CMOS logic circuit, 9-stage CMOS inverter ring oscillators are simulated via physics/process-based UFPDB model [9]. The model parameters are calibrated against the fabricated 70 nm devices where the same process condition is used for bulk-Si (control) and bulk-SS devices [3]. Since V_t is lower in the SS devices, both bulk-Si and SS devices are designed for equal V_t = 0.2 V at V_{DS} = 1.2 V to yield a fair performance comparison, by adjusting the channel-doping density (N_{ch}). For V_{DD} = 1.2 V, I_{on} is increased by ~15% in the SS nMOSFET and by ~5% in the SS pMOSFET. The I_{on} improvement for the SS pFET is less primarily due to the device design and process integration constraints [1], [2].

Fig. 1 compares predicted normalized delays versus V_{DD} for (fan-out of 1) unloaded 9-stage inverter ring oscillator with bulk-Si (control) and bulk-SS devices. The bulk-SS inverter is significantly faster. For equal delay, V_{DD} could be reduced by ~85 mV for the SS CMOS, which would decrease the static (DC) and dynamic (AC) power consumptions. Fig. 2 shows DC and AC power consumptions versus delay of the ring

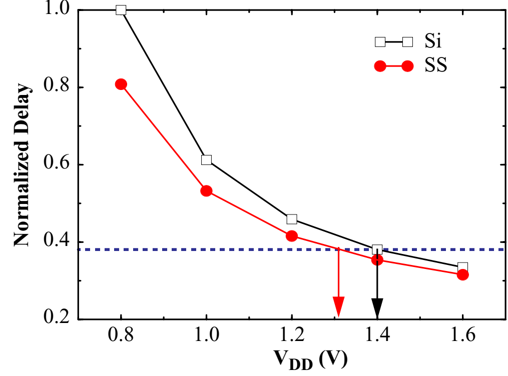


Figure 1. Predicted normalized delays per stage of (fan-out of 1) unloaded 9-stage inverter ring oscillator for bulk-Si and bulk-SS devices.

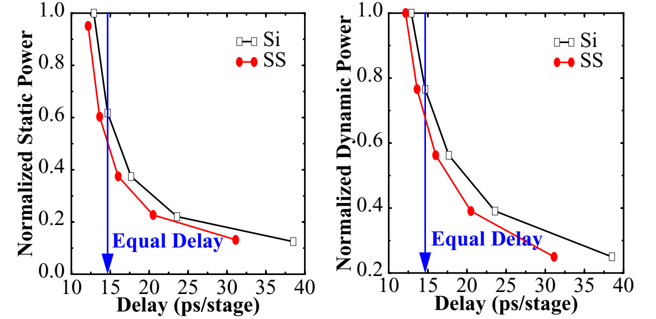


Figure 2. Predicted normalized normalized static (DC) and dynamic (AC) power consumptions of the unloaded ring oscillator for bulk-Si and bulk-SS devices in equal delay.

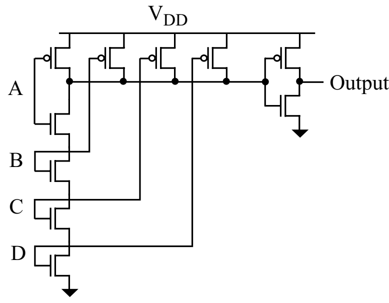
oscillator for the bulk-Si (control) and bulk-SS devices. For equal (fixed) delay ≅ 15 ps, DC power is ~20% lower in the SS device than the bulk-Si counterpart. Note that for equal V_{DD}, DC power is comparable since V_t (or I_{off}) is made equal. The lower V_{DD} would yield less DIBL in (8), thereby reducing I_{off} in (2) and DC power. For the equal delay, AC power ($\propto V_{DD}^2$) is ~10% lower in the SS device than the bulk-Si counterpart due to lower V_{DD}. Notice that optimum $W_{p(SS)}/W_{n(SS)}$ would be higher than $W_{p(Si)}/W_{n(Si)}$ due to lower $I_{on(pFET)}$ enhancement. Higher Ge content for SS pMOSFET would improve CMOS noise margin, offering better performance and less power consumption for the fixed performance as well.

4. STRAINED-SI CMOS CIRCUITS

We now analyze the more complex static CMOS circuits, self-resetting CMOS circuits, and latches.

4.1 Static 4-Way NAND

Fig. 3 shows the schematics of a static 4-way static NAND, followed by an output buffer, and depicts dynamic power consumption over one switching cycle versus frequency and static power consumptions for the five cases: (A, B, C, D) = (1, 1, 1, 1), (1, 1, 1, 0), (1, 1, 0, 0), (1, 0, 0, 0), (0, 0, 0, 0) during



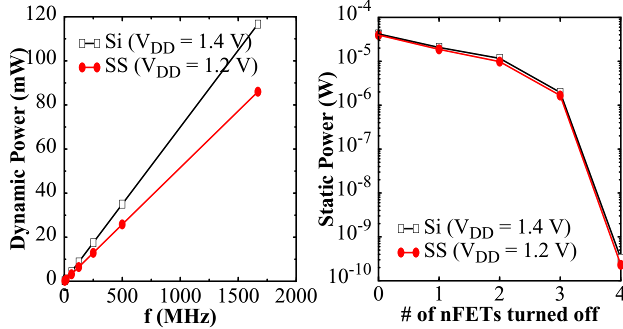
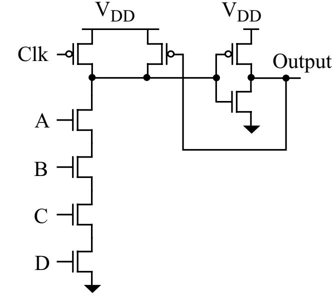


Figure 3. Static 4-way NAND circuit with bulk-Si and bulk-SS devices: dynamic power versus frequency and static power for (A, B, C, D) = (1, 1, 1, 1), (1, 1, 1, 0), (1, 1, 0, 0), (1, 0, 0, 0), (0, 0, 0, 0).



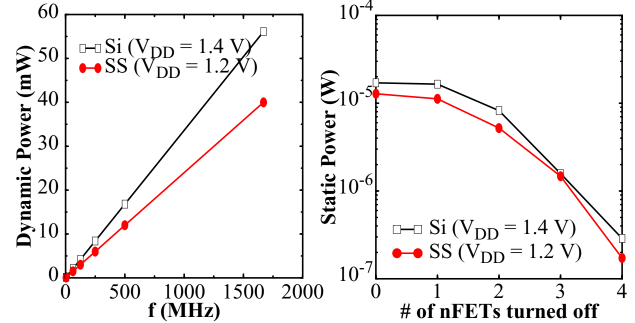


Figure 4. Dynamic self-resetting CMOS (SRCMOS) 4-way NAND circuit with bulk-Si and bulk-SS devices: dynamic power versus frequency and static power for (A, B, C, D) = (1, 1, 1, 1), (1, 1, 1, 0), (1, 1, 0, 0), (1, 0, 0, 0), (0, 0, 0, 0).

Clk = 1 for bulk-Si CMOS at V_{DD} = 1.4 V and SS CMOS at V_{DD} = 1.2 V. The static power is estimated in steady state of the circuits. For the equal delay in the critical path: (A, B, C, D) = (1, 1, 1, 1), V_{DD} for the SS devices can be reduced by ~0.2 V, which is much larger than the case for the inverter (85 mV). The more significant reduction in V_{DD} for NAND is due to the fact that the mobility enhancement in SS nFET significantly reduces the "ON" resistance of the stack devices, thus resulting in more significant performance improvement. The dynamic power is substantially reduced for SS CMOS. For the clock frequency range shown, dynamic power is reduced by ~26% for the static SS CMOS circuit. Static power consumptions are lower in SS CMOS circuit than the Si counterpart by ~5-30% for the five cases shown in Fig. 3. If four nFETs in NAND are turned off, the static power saving with SS is ~30%.

4.2 Self-Resetting CMOS 4-way NAND

Fig. 4 shows the schematics, dynamic power, and static power of a dynamic self-resetting CMOS (SRCMOS) 4-way NAND circuit with bulk-Si CMOS at V_{DD} = 1.4 V and SS CMOS at V_{DD} = 1.2V. For equal delay in the critical path: (A, B, C, D) = (1, 1, 1, 1), V_{DD} for the SS devices can be reduced by ~0.2 V, which is the same as static NAND circuit. The dynamic power is substantially reduced for SS CMOS. For the clock frequency range shown, the dynamic power is reduced by ~28% for the SS circuit. Static power consumptions for the cases shown in Fig. 4 are lower in SS CMOS circuit than the Si counterpart by ~25-40%. With all four nFETs in NAND turned off, the static power saving with SS is ~40%.

4.3 Latch

Fig. 5 shows the schematics of a clock-gated L1-L2 latch, and depicts the corresponding waveforms and dynamic power versus frequency for bulk-SS device compared with that for the bulk-Si one. The V_{DD} for SS latch is also ~0.2 V lower than that for bulk-Si one for equal delay. The dynamic power is substantially reduced for SS CMOS. For the clock frequency range shown, the dynamic power is reduced by ~27%, which is comparable to the static and dynamic SRCMOS 4-way NAND circuits. In the latch, static power is much smaller than dynamic power, and is ~45% lower for the SS case at A = 1, B = 1, and Clk = 1.

5. STRAINED SI ON SOI (SSOI)

SSOI CMOS has recently emerged for future high-performance applications with the benefits of both strained-Si and SOI devices [1], [2]. The areal junction capacitance (C_J) is significantly reduced in SSOI, resulting in higher speed and lower power. The simulation predicts SSOI CMOS inverter would offer ~10% faster speed and ~10% lower dynamic power over bulk-SS counterpart. However, due to the lower band gap in (4), SSOI could have different floating-body effect compared with SOI since all the generation and recombination currents are different [1], therefore hysteric V_t variation (or history effect) would be different for SSOI circuits. Furthermore, SSOI could have more severe self-heating effects than SOI due to the lower thermal conductivity in SiGe layer. Fig. 6 compares predicted delay versus power-delay product over one switching cycle for (fan-out of 1) unloaded 9-stage CMOS inverter ring oscillator for bulk-Si, bulk-SS, and SSOI

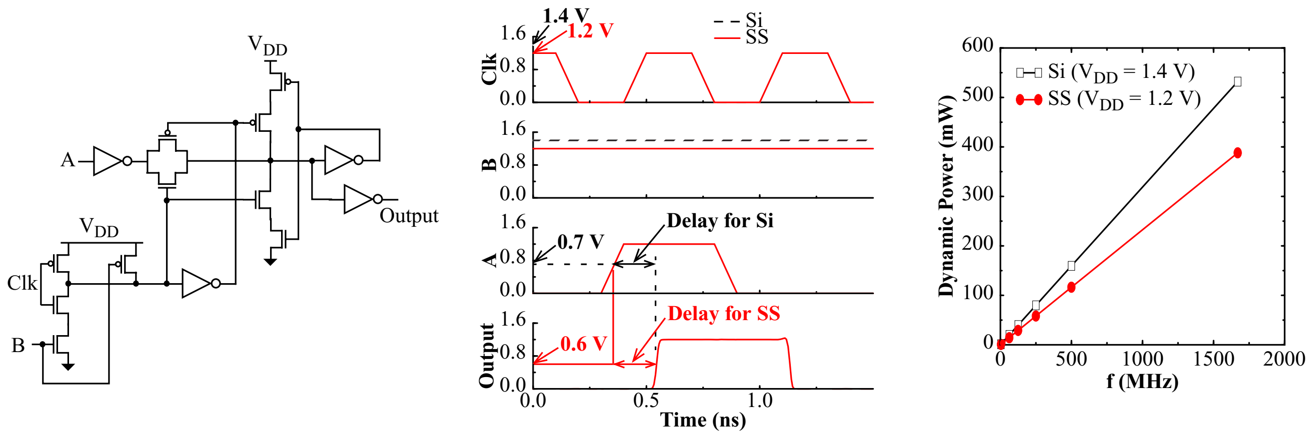


Figure 5. Clock-gated L1-L2 latch with bulk-Si and bulk-SS devices. The waveforms for equal delay cases and dynamic power versus frequency are shown.

devices. The V_t's for the three devices are the same at low V_{DS}. The energy dissipation is the lowest for SSOI CMOS. For equal V_{DD} = 1.4 V, SSOI CMOS exhibits ~7% lower energy dissipation than the bulk-Si counterpart. For equal delay around 15 ps, SSOI CMOS energy dissipation is ~44% lower than bulk-Si case and ~33% lower than bulk-SS case.

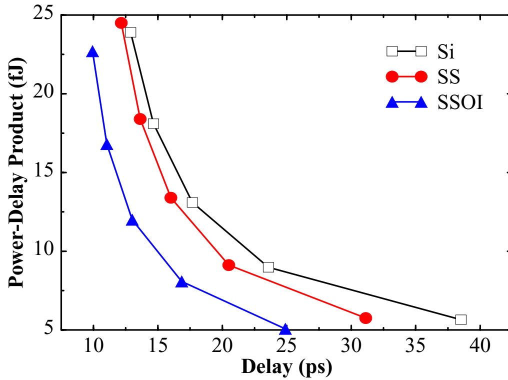


Figure 6. Predicted delay versus power-delay product for (fan-out of 1) unloaded inverter ring oscillator for bulk-Si, bulk-SS, and SSOI devices.

6. CONCLUSIONS

The performance and power for strained-Si MOSFET are analyzed and compared with conventional bulk-Si technology, from physical device characteristics to circuit applications. Based on theoretical studies and hardware-calibrated models, SS CMOS would offer lower static and dynamic power consumptions. Furthermore, SSOI, building SS channel with SOI structure, achieves higher performance and lower power.

7. ACKNOWLEDGMENTS

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