Effectiveness and Scaling Trends of Leakage Control Techniques for Sub-130nm CMOS Technologies

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Abstract

This paper compares the effectiveness of different leakage control techniques in deep submicron (DSM) bulk CMOS technologies. Simulations show that the 3-5x increase in I_{OFF}/μm per generation is offsetting the savings in switching energy obtained from technology scaling. We compare both the transistor I_{OFF} reduction and I_{ON} degradation due to each technique for the 130nm-70nm technologies. Our results indicate that the effectiveness of leakage control techniques and the associated energy vs. delay tradeoffs depend on the ratio of switching to leakage energies for a given technology. We use our findings to design a 70nm low power word line driver scheme for a 256 entry, 64-bit register file (RF). As a result, the leakage (total) energy of the word line drivers is reduced by 3x(2.5x) and for the RF by up to 35%(25%) respectively.

Categories and Subject Descriptors

C.4 [Performance of Systems]--*modeling techniques,* **B.7.1 [Integrated Circuits]:** Types and Design Styles—*advanced technologies, VLSI (very large scale integration)*

General Terms

Performance, Design, and Theory

Keywords

DSM leakage control and scaling trends, high performance RF design, non-minimum L_e, RBB.

1. Introduction

The need to achieve improved performance for high-end microprocessors, portable and wireless devices has resulted in aggressive technology scaling over the past two decades. As this trend continues into the future, it is expected that both the device geometry and transistor threshold voltage (V_{TH}) will be further scaled. This will lead to degraded short channel effects (*SCE*) and increased transistor OFF-state (I_{OFF}) current. Figure 1 shows the plots for I_{ON}/I_{OFF} ratio, and threshold voltages (V_{TH}) for low and high V_{TH} n-MOS transistors for the 130nm, 100nm and 70nm technologies [1]. The transistor I_{OFF}/μm is increasing by 3-5x per generation resulting in the degradation of the I_{ON}/I_{OFF} ratio with technology scaling. This will result in excessive leakage currents for the 70nm generation and offset the reduction in switching energy obtained from scaling. In addition, aggravated leakage current is causing thermal hot spots and thermal run away problems during burn-in and adversely affecting long-term reliability of high-end microprocessors [2-4, 6, 18]. Several different leakage control techniques have been proposed in the past [4-11] reducing transistor OFF-state current.

In this paper, we consider four of the most effective techniques:

- Reducing supply voltage (V_{CC}) [2, 6, 11]
- Non-minimum channel length (L_e) transistors [7]
- Stack effect [10, 14]
- Reverse body bias (RBB) [8, 9]

and compare their effectiveness in reducing leakage current for the 130nm-70nm technologies. In addition, we compare the degradation in I_{ON} associated with each of these leakage control techniques. This enables us to choose the most efficient technique offering maximum leakage current savings with minimum degradation in transistor saturation current (I_{ON}) and circuit performance.

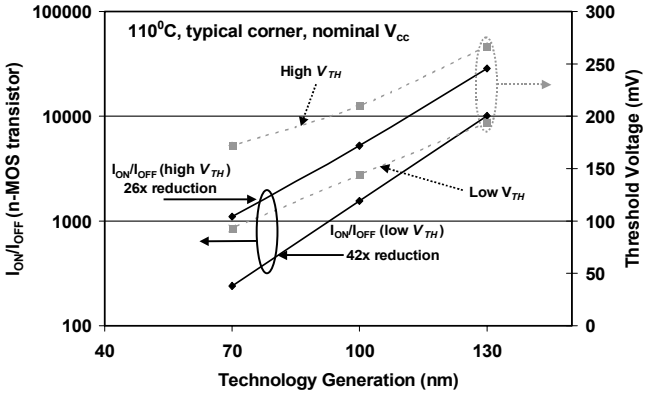

Figure 1: I_{ON}/I_{OFF} and V_{TH} scaling for sub-130nm generations

Register files (RF) are performance critical building blocks of high-end microprocessors requiring single cycle read/write latency [12, 13, 21]. In this paper, we design low power word-line (WL) drivers using the above mentioned leakage control techniques for a 256-entry 64-bit high-performance RF. We discuss the energy vs. delay tradeoffs associated with each WL driver implementation. Supply voltage reduction allows switching and leakage energy savings and is most effective in reducing total energy for the 130nm generation. However, for the subsequent technologies, leakage energy dominates the total energy. In addition, our simulations indicate that

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RBB and non-minimum L_e techniques reduce transistor I_{OFF} with minimum I_{ON} degradation. Consequently, RBB and non-minimum L_e techniques become more efficient leakage control techniques for high performance digital circuits in the sub-130nm regime.

Rest of the paper is organized as follows: Section 2 discusses various leakage control techniques and models their impact on transistor I_{OFF}. In Section 3, we present data showing the degradation in transistor I_{ON} caused by the leakage control techniques. In Section 4, implementation of the leakage control techniques for a 256-entry 64-bit RF is described. Section 5 discusses some implementation overheads and Section 6 summarizes our conclusions and discusses future work.

2. Leakage Control Techniques

In this section, we discuss the leakage control mechanism of the four above-mentioned techniques and present simulation results showing the reductions in I_{OFF} for the 130nm generation. The transistor I_{OFF} comprises of several different components [10, 17] of which, the weak inversion and drain-induced barrier lowering (*DIBL*) currents are the most important. These two dominant leakage current components can be modeled using Eq. 1 [10, 14-16] as shown below:

$$I_{OFF} = Ae^{\left(\frac{V_{GS}-V_{TH0}-\gamma V_{SB}+\eta V_{DS}}{nv_T}\right)}.\left(1-e^{\frac{-V_{DS}}{v_T}}\right) \quad (1)$$

where, $A = \mu_0 C_{ox} W/L_{eff}\, v_T^2 e^{1.8}$, μ_0 is the zero bias carrier mobility, C_{ox} is the gate-oxide capacitance, L_{eff} is the transistor effective channel length, W is the transistor width, η is the *DIBL* coefficient, γ is the linearized body effect coefficient, n is the transistor sub-threshold swing coefficient and v_T is the thermal voltage given by kT/q (~33mV at 110^{0}C). In addition, V_{TH0}, V_{GS}, V_{SB} and V_{DS} denote the transistor zero-bias threshold voltage, gate-source, source-body, drain-source voltages respectively. We determined the worst-case transistor leakage by simulating the device OFF-state current at 110^{0}C for $V_{GS} = 0V$ and $V_{DS} = V_{DD}$ as shown in Figure 2(a-d).

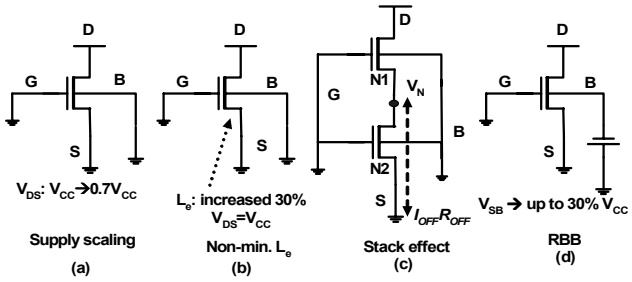

Figure 2: Leakage control techniques: simulation setup

In this study, we present data for the n-MOS transistor only. Results for the p-MOS transistor show similar trend and hence are not shown. Based on the leakage current expression in Eq. 1 and simulation setup shown in Figure 2, it is possible to establish closed form approximate expressions modeling [16, 19] the reduction in leakage current for each of the techniques. We use the term $\Delta I_{OFF}/I_{OFF}$ to quantify the leakage current reduction, where:

$$\frac{\Delta I_{OFF}}{I_{OFF}} = \frac{I_{OFF} - I_{OFF}^{final}}{I_{OFF}} = 1 - \frac{I_{OFF}^{final}}{I_{OFF}} \quad (2)$$

and, I_{OFF} and I_{OFF}^{final} represent the transistor OFF-state current without and with leakage control, respectively. In order to simplify the modeling using Eq. 1, we assume $e^{\frac{-V_{DS}}{v_T}} \approx 0$. This approximation is justified since in this study, the ratio of $V_{DS}/v_T \geq 20$. Thus, the simplified transistor OFF-state current is given by:

$$I_{OFF} \approx Ae^{\left(\frac{V_{GS}-V_{TH0}-\gamma V_{SB}+\eta V_{DS}}{nv_T}\right)} \quad (3)$$

Supply voltage reduction lowers the transistor drain-source voltage consequently reducing the *DIBL* current (Figure 2(a)). In addition, since $V_{SB} = 0V$, the corresponding term in Eq. 3 is equal to zero. Thus, the reduction in leakage current obtained by lowering of the supply voltage is given by:

$$\left.\frac{\Delta I_{OFF}}{I_{OFF}}\right|^{V_{CC}} = 1 - e^{-\frac{\eta \Delta V_{DS}}{nv_T}} \quad (4)$$

Non-minimum channel length transistors (Figure 2(b)) reduce the I_{OFF} [7] by increasing the zero-bias threshold voltage (V_{TH0}). The impact of transistor channel length on V_{TH0} is shown in Figure 3.

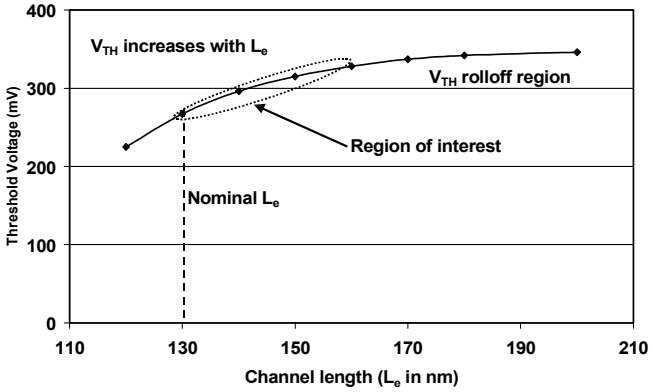

Figure 3: V_{TH} vs. channel length for 130nm n-MOS transistor

In the region of interest (Figure 3), the threshold voltage increases almost linearly for small increases in the drawn channel length (L_e). As a result, the increase in the transistor zero bias threshold voltage

can be approximated using $\Delta V_{TH0} = V_{TH0}\left(\frac{\Delta L_e}{L_e}\right)$. In addition, the channel mobility remains approximately constant due to velocity saturation in *DSM* transistors. Therefore, the reduction in leakage current using non-minimum channel length transistors can be modeled as:

$$\left.\frac{\Delta I_{OFF}}{I_{OFF}}\right|^{L_e} = 1 - \frac{1}{1 + \frac{\Delta L_{eff}}{L_{eff}}} e^{\frac{-\Delta V_{TH\,0}}{nv_T}} \quad (5)$$

where, ΔL_{eff} is the change in effective channel length (L_{eff}) while all other terms have their usual meanings.

Similarly, the reduction in leakage current using stack effect can be explained with the help of Figure 2(c). The intermediate node voltage *(V_N)* reaches a steady state DC value for the two stack n-MOS pull down when both transistors are OFF. This value is within an order of magnitude of the thermal voltage (v_T) and can be calculated using the generalized equations derived in [14]. Simulations in 130nm CMOS technology for our specific circuit indicate that V_N reaches a steady state value of 95mV. This results from the $I_{OFF}R_{OFF}$ voltage drop across the bottom transistor *(N2)*. As a result, a negative V_{GS} gate drive voltage appears across the top n-MOS transistor *(N1)* of the stack. Furthermore, there is a reduction in V_{DS} (*DIBL* current suppression) and appearance of negative V_{BS} (RBB) across the top transistor *(N1)* because of stack effect. Thus, the leakage current reduction using stack effect is:

$$\left.\frac{\Delta I_{OFF}}{I_{OFF}}\right|^{stack} = 1 - e^{\frac{-I_{OFF}R_{OFF}(1+\gamma+\eta)}{nv_T}} \quad (6)$$

Finally, the leakage current can be suppressed by reverse body biasing (RBB) the transistor (Figure 2(d)). The body of the n-MOS transistor is connected to a negative voltage with respect to the source terminal. The reduction in leakage current is proportional to the extent of the applied reverse bias voltage (V_{SB}). However, recent research indicates [8, 9] that beyond a certain optimal RBB voltage the transistor OFF-state current starts to increase due to increased gate induced drain lowering *(GIDL)* leakage as shown in Figure 4.

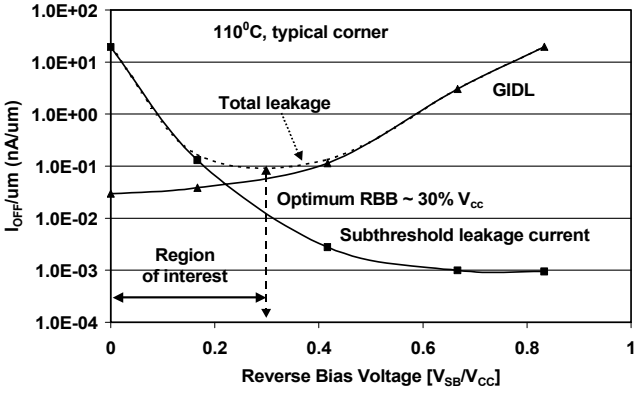

Figure 4: Optimum RBB voltage for 130nm technology

For the range of RBB voltages in the region of interest, Eq. (3) can be used to model the leakage current reduction as follows:

$$\left.\frac{\Delta I_{OFF}}{I_{OFF}}\right|^{RBB} = 1 - e^{\frac{-\gamma V_{SB}}{nv_T}} \quad (7)$$

The reduction in n-MOS transistor worst-case I_{OFF} was modeled for each leakage control technique using Eqs. (4-7). Table 1 demonstrates, that the theoretical models track the simulation results for all the four above-mentioned techniques. However, the models consistently under estimate the reductions in leakage current. This is because the simplified equations do not account for all the leakage current components and associated reductions when using leakage control techniques. These results indicate that stack effect reduces leakage current by up to 12x while using non-minimum L_e (L_e increased 30%) reduces leakage by 9.3x. On the other hand, supply voltage reduction (V_{CC} reduced by 30%) or RBB equal to 30% of V_{CC} reduces leakage by 2.2x-2.3x.

Table 1: Leakage current reductions for 130nm technology

Technique	Simulation Results	Theoretical Model
Supply Voltage (30% V_{CC} reduction)	2.2x	1.9x
Non minimum L_e (L_e+30%)	9.3x	8.7x
Stack Effect	12.0x	11.5x
RBB (30% reverse bias)	2.3x	2.1x

3. Performance Impact and Scaling Trends

An efficient leakage control technique is one that allows large reduction in I_{OFF} with minimum I_{ON} degradation. This helps minimize the adverse performance impact of the leakage control techniques when used in high-end digital circuits. We quantify the I_{OFF} vs. I_{ON} tradeoffs for each technique in Figures 5 (a) and 5(b) for the 130nm and 70nm generations.

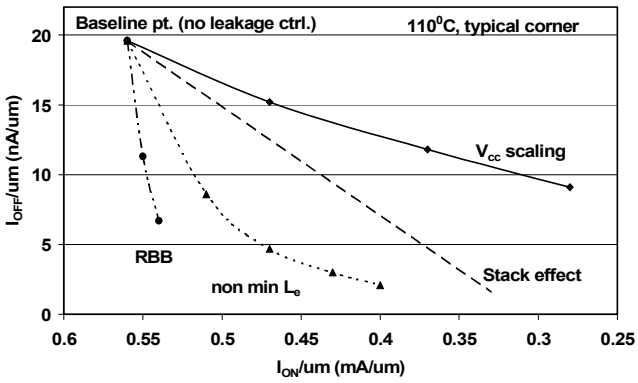

Figure 5(a): I_{OFF} vs. I_{ON} plots for 130nm technology

The data for the 100nm generation shows similar trend, and is therefore not presented. These figures indicate that both RBB and non-minimum L_e techniques result in lesser degradation of transistor I_{ON} than supply V_{CC} reduction or stack effect. Consequently, both RBB and non-minimum L_e techniques have steeper gradients in the I_{OFF}-I_{ON} plane making them more efficient in reducing leakage current for the 130nm-70nm generations. The extent to which I_{OFF} can be reduced using RBB is however limited by the optimal reverse bias voltage as discussed in Section 2.

In addition to examining the performance trade-offs, we study the scalability of these techniques for the sub-130nm generations. For this purpose, we compare the degradation of the normalized I_{OFF}/I_{ON} ratio as shown below:

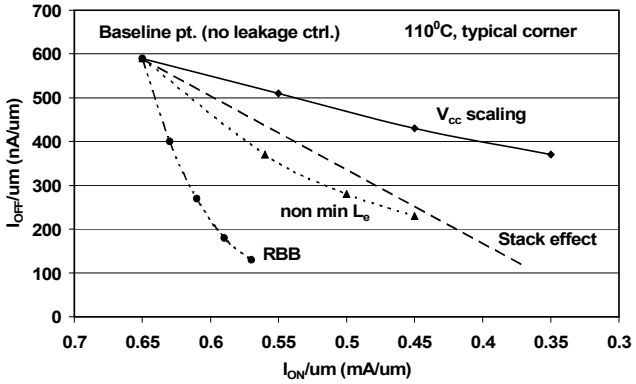

Figure 5(b): I_{OFF} vs. I_{ON} plots for 70nm technology

$$\xi = \left(\frac{\partial I_{OFF}}{\partial I_{ON}}\right) \Big/ \left(\frac{I_{OFF}}{I_{ON}}\right) \tag{8}$$

Table 2 shows the value of ξ and scaling trends for each of the leakage control techniques. It should be noted that a technique with higher value of ξ is more efficient in reducing leakage current.

Table 2. Normalized I_{OFF}/I_{ON} degradation: scaling trends

$\xi = \left(\frac{\partial I_{OFF}}{\partial I_{ON}}\right) \Big/ \left(\frac{I_{OFF}}{I_{ON}}\right)$	130nm	100nm	70nm
Supply Voltage (30% V_{CC} reduction)	1.1	1.0	0.8
Non minimum L_e (L_e+30%)	3.1	3.1	2.8
Stack Effect	2.2	2.1	1.9
RBB (30% reverse bias)	20.0	9.0	7.5

Our results indicate that RBB followed by non-minimum L_e have the highest ξ values. On the other hand, the degradation in I_{ON} resulting from techniques like supply voltage reduction and stack effect (2 series transistors) make their respective ξ values lower. In fact, the reduction in I_{ON} more than offsets the savings in leakage current when supply voltage is reduced by 30% for the 70nm generation.

4. Low Power Word Line Driver for RFs

Wide bit-width register files (RF) are performance-critical components of microprocessor integer/FPU execution cores and demand single cycle read/write latency. In this section, we use the leakage control techniques discussed in the previous sections to implement low power word line (WL) drivers for a 2-read, 1-write ported 256-entry 64-bit high performance RF whose organization is shown in Figure 6. Each of the 256 RF entries is uniquely selected using an 8:256 decoder scheme that generates the read and write select (RS/WS) signals. In order to read/write from an entry, only one WL driver signal/port switches high (active) while the rest of the 255 drivers are inactive and are leaking. The read port WL drivers are on the RF critical path and are hence upsized to drive the 32 local bit-cells on each side of this partitioned RF. This results in increased leakage for the WL drivers of the 255 deselected entries.

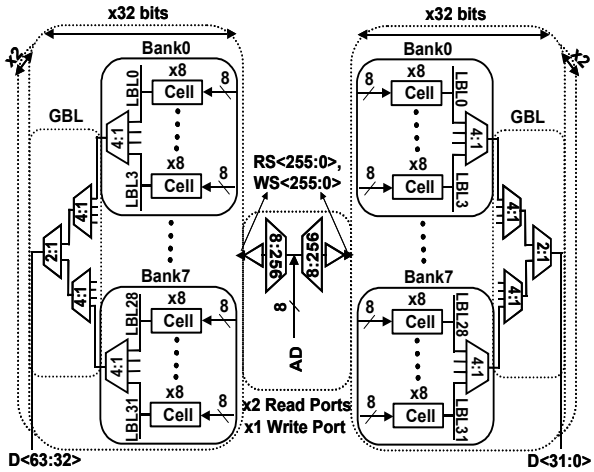

Figure 6: 2R-1W ported 256 entry-64 bit RF organization

Figure 7 shows the contribution of the WL drivers to the RF total energy as a function of technology scaling. In addition, we show the breakup of the WL driver total energy in terms of switching and leakage energy. The normalized WL driver energy contribution increases from 18% (130nm) to 27% (70nm) of RF total energy with scaling. The WL driver switching energy reduces by about 50% per generation due to capacitance and voltage scaling as indicated in Figure 7.

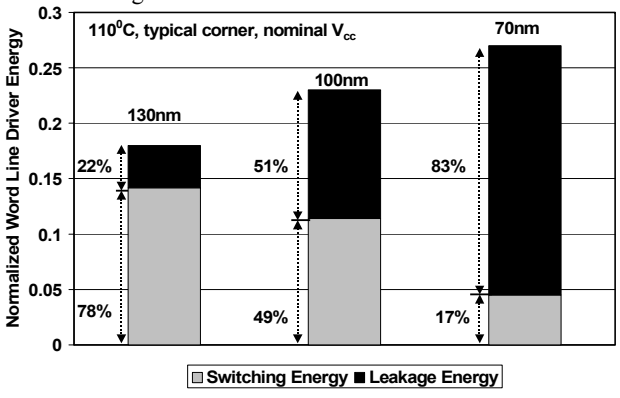

Figure 7: Word line driver energy breakup and scaling trends

The WL driver leakage energy however, increases from 22% (130nm) to 83% (70nm) of the total energy due to 3-5x increase in $I_{OFF}/\mu m$ per generation. This provides the basis for our investigation into efficient leakage control techniques for the RF word line drivers. Figure 8 shows the layout of the WL drivers and the local bit-line (*LBL*) interconnects of the 256 entry 64 bit RF for the 130nm generation.

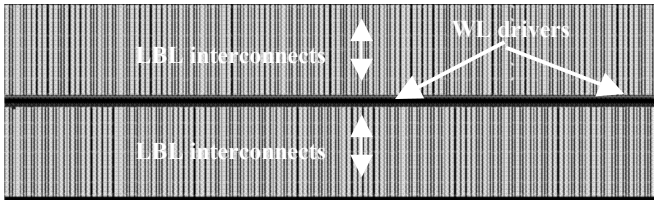

Figure 8: WL driver layout for 256-entry, 64-bit 130nm RF

Figures 9(a) and 9(b) show the WL driver total energy (switching + leakage) vs. delay tradeoffs for each of the leakage control techniques for the 130nm and 70nm generations respectively.

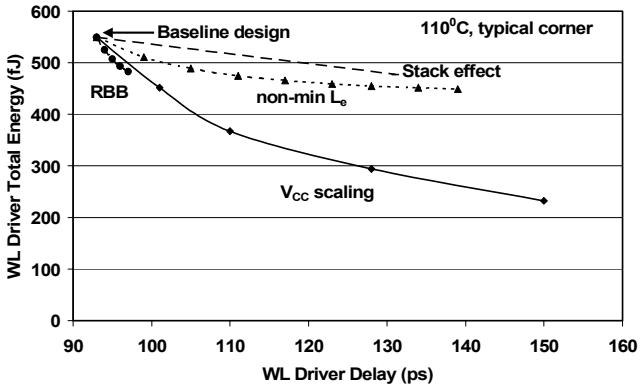

Figure 9(a): Total energy vs. delay for 130nm WL drivers

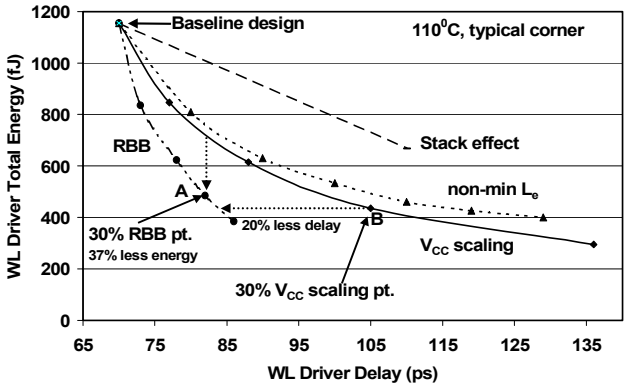

Figure 9(b): Total energy vs. delay for 70nm WL drivers

Switching energy dominates the WL driver total energy (switching energy α V_{cc}^2) for the 130nm generation. Thus, a 30% supply voltage reduction allows a 2.4x reduction in total energy and a 3.6x reduction in leakage energy. The reduction in leakage energy using RBB is however limited by the optimal reverse body bias voltage discussed earlier. In addition, RBB does not have significant impact on switching energy. Consequently, 30% RBB allows a 12% reduction in total energy while reducing leakage energy by 1.9x for the 130nm technology (Figure 9(a)).

However, as the technology is scaled to 70nm, leakage energy becomes 83% of WL driver total energy and RBB becomes more effective than supply scaling as indicated in Figure 9(b). Thus, a 30% RBB allows 3x(2.5x) reduction in leakage (total) energy compared to the baseline design (design with no leakage control). We compare the RBB and V_{cc} scaling curves at 2 points (A and B) in the total energy vs. delay plane. Point A corresponds to the 30% RBB case and allows 37% savings in total energy compared to V_{cc} scaling at the same delay. On the other hand, point B corresponds to the case with 30% V_{cc} scaling and indicates that RBB allows 20% improved performance for the same total energy. It should be noted that the energy vs. delay tradeoffs for the different techniques is dependent on the switching and leakage energy breakup of the total energy and the V_{CC}/V_{TH} ratio for a given technology.

Figure 10 shows the leakage energy, total energy and delay tradeoffs for the 70nm, 2 read-1 write ported 256 entry 64-bit RF using the different low power word line drivers. The leakage (total) energy reduction for the RF is between 30-35% (13-25%) while the worst-case RF read delay increases by 4-21%. Our results indicate that RBB followed by usage of non-minimum L_e transistors offer better energy savings with less delay penalties for the 70nm RF design and are more efficient than techniques involving reduced supply voltage or stack effect.

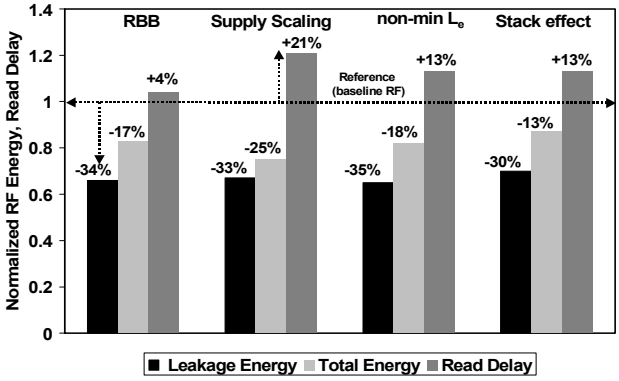

Figure 10: Normalized leakage, total energy, delay: 70nm RF

5. Implementation Issues

In addition to performance degradation, the above-mentioned leakage control techniques have certain implementation overheads. For example, the selective usage of supply voltage reduction for the word line drivers might require a dual-V_{cc} design to mitigate excessive performance penalty [20]. This requires the generation and routing of a second power supply within the RF. Similarly, the usage of RBB requires the generation and routing of extra power supply to the body and well terminals of n- and p-MOS transistors. In addition, it will require the usage of a triple well bulk CMOS process [5] increasing the overall implementation cost. The stack effect and non-minimum L_e techniques do not require any additional power supply. However, stack effect reduces the effective transistor I_{ON} and results in excessive performance degradation. Furthermore, the additional stack transistor has to be upsized thereby increasing the overall switching energy and area penalty. On the other hand,

usage of non-minimum L_e would require precise process control over the transistor channel length.

6. Conclusions and Future Work

In this paper, we have compared four different leakage control techniques and discussed their effectiveness in reducing leakage and total energy for the 130nm-70nm technologies. We demonstrated that RBB followed by non-minimum L_e are the most efficient leakage control techniques in the sub-130nm regime. However, the effectiveness of each of these techniques in reducing leakage and total energy depends on the ratio of switching/leakage energy and V_{CC}/V_{TH} for a given technology. Based on the above results we designed a low power word line driver for a 2 read, 1 write ported, 256 entry 64 bit RF which achieved 3x(2.5x) reduction in leakage (total) energy for the 70nm generation.

In this paper, we modeled the impact of leakage control techniques on the sub-threshold current. However, it is expected that the gate leakage will become a significant component of the total transistor leakage current in the sub-100nm regime. Both stack effect and non-minimum L_e techniques result in the increase of the overall transistor active area. In addition, RBB results in an increase of the effective gate-body voltage. Thus, a more detailed model needs to account for the impact of leakage control techniques on gate leakage for DSM technologies. Studying the reductions in total leakage energy afforded by various leakage control techniques in the context of high performance digital logic blocks remains the topic of our future research.

7. Acknowledgements

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