Understanding and Minimizing Ground Bounce During Mode Transition of Power Gating Structures

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ABSTRACT

We introduce and analyze the ground bounce due to power mode transition in power gating structures. To reduce the ground bounce, we propose novel power gating structures in which sleep transistors are turned on in a non-uniform stepwise manner. Our power gating structures reduce the magnitude of peak current and voltage glitches in the power distribution network as well as the minimum time required to stabilize power and ground. Experimental simulation results with PowerSpice fixtured in a package model demonstrate the effectiveness of the proposed power gate switching noise reduction techniques.

Categories and Subject Descriptors

B.7.1 [**Integrated Circuits**]: Types and Design Styles—*advanced technologies, microprocessor and microcomputers*

General Terms

Reliability Design

Keywords

clock gating, power gating, wake-up latency, inductive noise, ground bounce, system-on-a-chip (SOC) design.

1. INTRODUCTION

If the magnitude of a voltage surge/droop due to ground bounce is greater than the noise margin of a circuit, the circuit may erroneously latch the wrong value or switch at the wrong time. Traditionally, ground bounce has been a phenomenon associated with input/output buffers and internal circuitry [1, 2, 3]. Recently, this inductive noise problem has also been associated with clock gating in [4, 5].

Until now, however, ground bounce originating from the power-mode transition of a power gating structure was not seriously considered, even though it affects the reliability of a system-on-a-chip (SOC) employing multiple power gating domains to control leakage power. As shown in Figure 1, this noise source may induce ground bounce in neighboring circuits which are executing normal operations.

In this paper, we introduce and analyze ground bounce induced by an instantaneous power-mode transition of a sleep transistor in power gating structures. To reduce ground bounce, we propose novel power gating structures in which sleep transistors are turned on in a non-uniform stepwise manner. Such power gating structures reduce the magnitude of voltage fluctuations in the power distribution network as well as the time required to stabilize them. Stepwise switching of the sleep transistors is implemented either by dynamically controlling the gate-to-source voltage, V_{GS}, of a sleep transistor or by turning on only a portion of the sleep transistor at one time. The stepwise switching consists of a relaxation stage follow by a complete turn-on stage. During the relaxation stage, the gate voltage of the sleep transistor is charged to only a small portion of the rail voltage or only a small portion of the sleep transistor gate is switched full-rail. This stage allows the V_{DS} of the sleep transistor to reduce significantly with only a small peak current. During the complete turn-on stage, V_{GS} is charged up to VDD or the remaining portion of the sleep transistor is switched on, respectively.

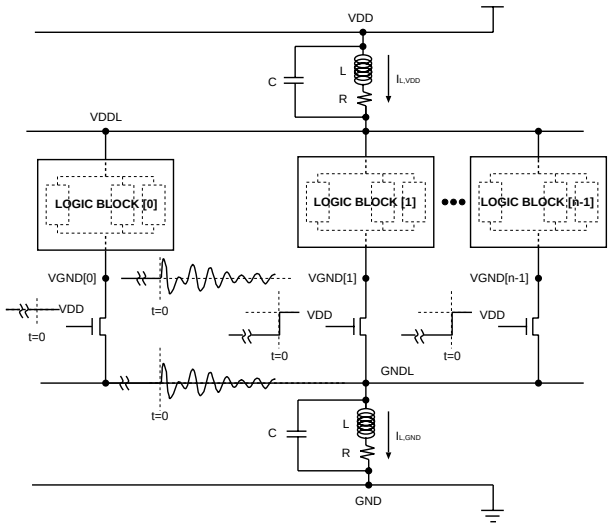

Figure 1: Ground bounce in a system-on-a-chip employing multiple power gating structures to control leakage power.

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2. UNDERSTANDING GROUND BOUNCE

In this section, ground bounce due to switching of the sleep transistor in a power gating structure is introduced and analyzed.

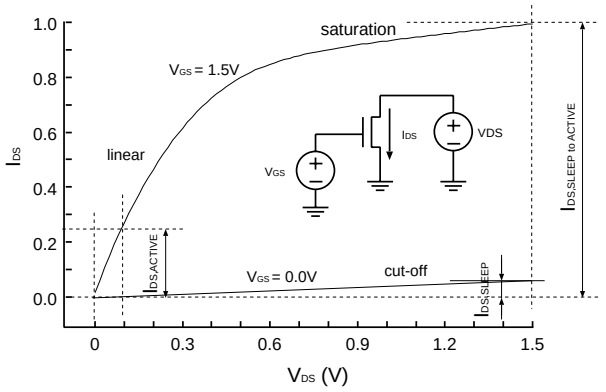

Figure 2: I-V characteristics.

In active mode, the sleep transistor of the power gating structure operates in its linear region of Figure 2. The sleep transistor may be modeled by a resistor R_{active}. This generates a small voltage drop V_{VGND} equal to $I_{\text{active}} \times R_{\text{active}}$, where I_{active} is the total current demand of the logic block operating in active mode. The voltage drop reduces the the gate's drive capability from VDD to VDD-V_{VGND} and and increases the threshold voltage of NMOS pull-down devices due to the body effect. Both effects degrade the speed of the circuit. The size of the sleep transistor should not be too small.

In standby mode, the sleep transistor operates in the cut-off region of Figure 2 and may be modeled by an open switch. During this mode, the leakage current is limited by the sleep transistor, which is reduced by a high threshold and a proportionally smaller width. By turning off the sleep transistor during the sleep period, all internal capacitive loads connected to the VGND node through NMOS pull-down devices are charged up to a steady state value near VDD.

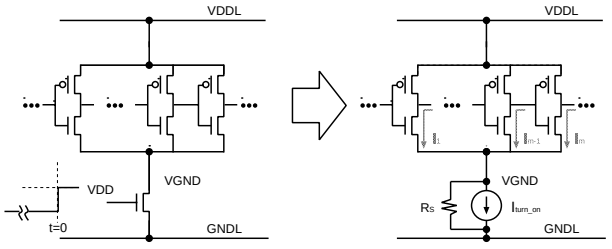

Figure 3: Sleep transistor operates as current source.

If the sleep transistor is turned on in step manner, all of charge trapped in the internal capacitive nodes and the VGND node discharges rapidly through the switched NMOS pull-down paths of logic blocks and sleep transistor. Initially, as shown in Figure 3, the sleep transistor operates in the saturation region and may be modeled by a current source.

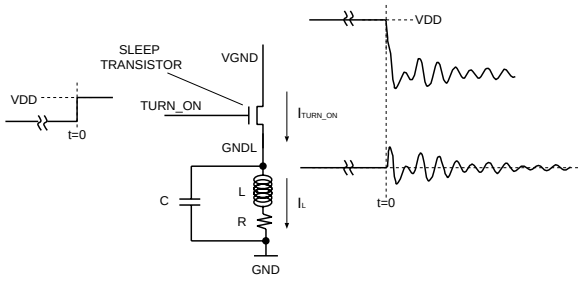

Figure 4: Switching noise within a on-chip ground rail.

The amount of instantaneous current that can flow through the sleep transistor at this moment is much larger than the active mode current, I_{active}. As shown in Figure 4, the current surge creates inductively induced voltage fluctuations in the power distribution network.

3. NOVEL POWER GATING STRUCTURES

In this section, we propose novel power gating structures in which V_{GS} or the effective size of the sleep transistor increases dynamically in a non-uniform stepwise manner.

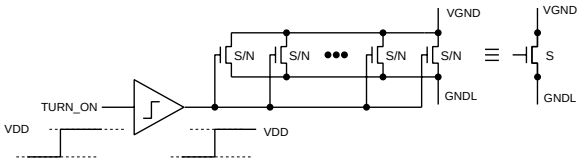

Figure 5: A sleep transistor or a set of sleep transistors used in a conventional power gating structure.

Figure 5 shows a previously published power gating structure in which the sleep transistor is implemented with a single transistor or a set of transistors [6, 7, 8]. A sleep transistor implemented by a set of individual transistors wired in parallel is effectively a single transistor because the transistors share both VGND node and GNDL rail and are turned on simultaneously. During the mode transition of these conventional power gating structures, the large instantaneous current flow through the sleep transistor causes large voltage fluctuations in the on-chip power distribution network.

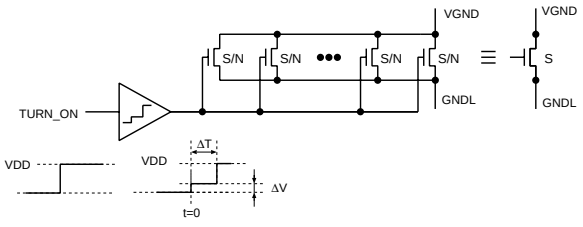

Figure 6: A sleep transistor or a set of sleep transistors whose V_{GS} increases in a non-uniform stepwise manner.

To solve this problem, we propose two different techniques to minimize the instantaneous current flow through the sleep transistor. The first is by dynamically controlling V_{GS} and hence V_{DS}, as shown in Figure 6. During the relaxation

stage, the sleep transistor is weakly turned on with $V_{GS} = V_X$ ($0 < V_X <$ VDD), until its V_{DS} is significantly reduced. During the complete turn-on stage, the sleep transistor is completely turned on with V_{GS} = VDD. When the V_{DS} of the sleep transistor is small enough, the instantaneous current is less sensitive to variation in the V_{GS} of the sleep transistor, thus allowing increasing V_{GS} of the sleep transistor in a non-uniform stepwise manner without increasing instantaneous peak current.

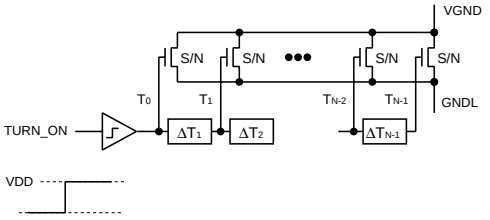

Figure 7: A portion of sleep transistor that is switched on increases in non-uniform stepwise manner.

The second is dynamically resizing the effective size of the sleep transistor, as shown in Figure 7. Specifically, only a small portion of the sleep transistor is turned on with V_{GS} equal to VDD until its V_{DS} is significantly reduced. Then, the remaining portion of the sleep transistor is completely turned on with its V_{GS} at VDD. When the V_{DS} is small enough, the instantaneous current is less dependent on the percentage of the sleep transistor that is turned on. This observation encourages increasing the portion of the sleep transistor that is turned on in a non-uniform stepwise manner.

4. SIMULATION RESULTS

To demonstrate the benefit of these novel power gating structures, we have designed three different arithmetic and logic units (ALUs) in 0.13 μm CMOS technology. These ALUs were simulated with PowerSpice fixtured in a DIP-40 package model where $R1$, $L1$, and $C1$ are 0.217 Ω, 8.18nH, and 5.32pF, respectively. All ALUs have the same functional units, including a multiplier, add and subtract unit, shifter and saturation unit, comparator, logic unit, and data-retention latches and operate at 500MHz at 1.5V. The power gating structure of each ALU has the same size of sleep transistor, sized at approximately 3.0% of the total PMOS and NMOS transistor width of the functional units in the ALU. Each ALU uses a unique power gating structure, however.

Figure 8 shows a block diagram of a 16-bit ALU with a conventional power gating structure in which the sleep transistor consists of a set of transistors turned on by a static CMOS buffer. Even though the sleep transistor is composed of a set of transistors, these transistors share TURN_ON node, VGND node, and GNDL rail. Figure 8 also shows the parameters defined to characterize the impact of inductive noise caused by the power-mode transition. $V_{MIN/VDDL}$ and $V_{MAX/VDDL}$ are, respectively, the lowest and highest voltage levels of the bounce on the VDDL rail. $V_{MIN/GNDL}$ and $V_{MAX/GNDL}$ are, respectively, the lowest and highest voltage levels of the bounce on the GNDL rail. T_S is the minimum time required for both the VDDL and GNDL rails to be stabilized within ± 5% of nominal and defines the minimum delay before the ALU operates at its specified performance. The measurement of T_S is started at the falling edge of TURN_ON signal of each power gating structure.

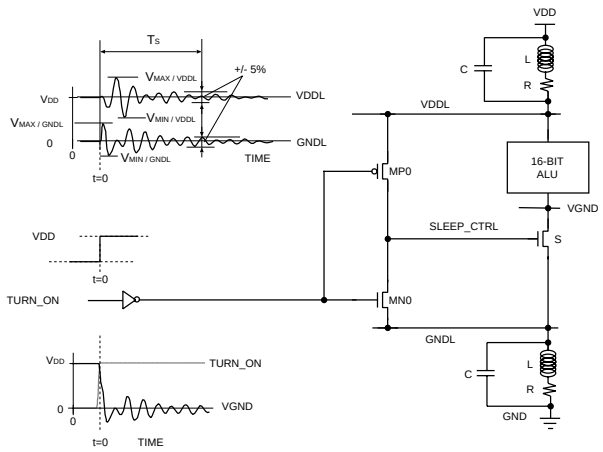

Figure 8: Block diagram of 16-bit ALU with a conventional power gating structure whose sleep transistors are turned on by a static CMOS buffer.

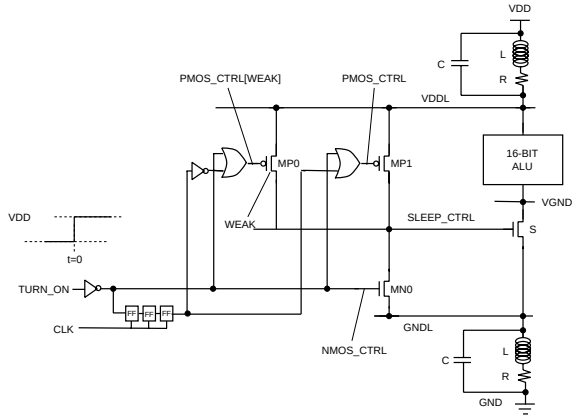

Figure 9: Block diagram of 16-bit ALU with one of novel power gating structures whose sleep transistor is turned on by a non-uniform stepwise voltage generation circuit.

Figure 9 shows a block diagram of a 16-bit ALU with one of novel power gating structures in which the sleep transistor is turned on by a stepwise voltage generation circuit. As TURN_ON becomes high, the relaxation stage is initiated. The weak transistor MP0 is turned on for 3 clock cycles and V_{GS} of the sleep transistor slowly increases with RC delay. When the V_{DS} is discharged significantly, the complete turn-on state is initiated. The strong transistor MP1 is turned on and V_{GS} is completely charged up to VDD.

Figure 10 shows a block diagram of the 16-bit ALU with another novel power gate structure including a 3-bit shift register to control turn-on of the sleep transistor. As TURN_ON becomes high, $\frac{1}{23}$ of total sleep transistor size is turned on with V_{GS} = VDD. Then, the percentages of sleep transistor turned on with V_{GS} = VDD increases every cycle, until the sleep transistor is completely turned on.

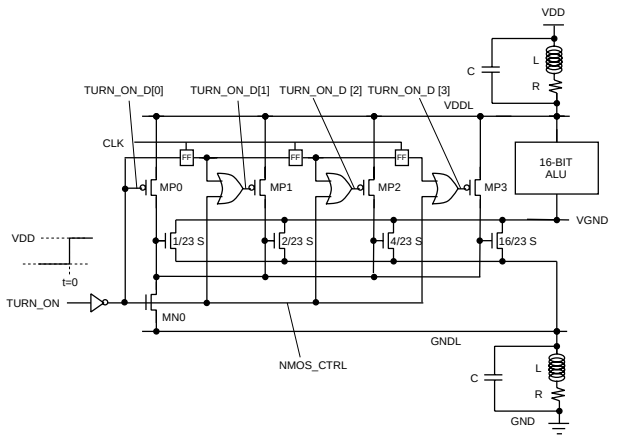

Figure 10: Block diagram of a 16-bit ALU with another novel power gating structure in which sleep transistors are sequentially turned on in a non-uniform manner.

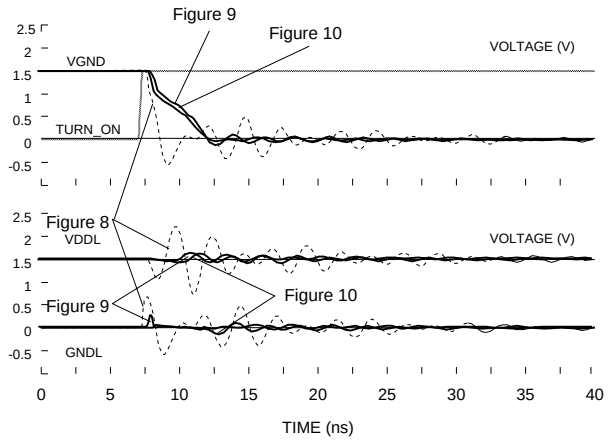

Figure 11: PowerSpice simulation results for novel power gating structures of Figure 9 and Figure 10, compared to a conventional one of Figure 8

Figure 11 shows the voltage waveforms of the VGND node and sleep transistor TURN_ON signal, and the voltage fluctuation waveforms of VDDL and GNDL rails of the ALUs with novel power gating structures of Figure 9 and Figure 10, compared to the ALU with a conventional power gating structure of Figure 8.

	Figure 8:Figure 9	Figure 8:Figure 10
$I_{MAX/R1}$	86.18%	80.06%
$I_{MIN/R1}$	76.07%	87.15%
$V_{MAX/VDDL}$	83.61%	83.89%
$V_{MIN/VDDL}$	87.94%	89.04%
$V_{MAX/GNDL}$	84.79%	60.96%
$V_{MIN/GNDL}$	77.16%	88.40%
T_S	68.20%	81.16%

Table 1: Relative inductive noise reduction.

The simulation results are summarized in Table 1, in terms of the parameters defined to characterize the ground bounce induced by the mode transition of power gating structure. The simulation results show that the ALUs with proposed power gating structures have smaller peak current and voltage glitches at the on-chip power distribution network and faster power supply and ground rail stabilization times.

5. CONCLUSIONS

This paper investigates the ground bounce caused by large discharge current through a sleep transistor during the mode transition of the power gating structure. Two novel power gating structures are proposed to reduce the magnitude of voltage glitches in the power distribution network as well as the time required for the network to stabilize.

In PowerSpice simulation of a 16-bit arithmetic and logic unit (ALU) with a DIP-40 package model, the maximum magnitude of voltage glitches on the VDDL and GNDL rails of the ALUs with our power gating structures are reduced by up to 89.04% and 88.40%, respectively, compared to the ALU with a conventional gating structure. At the same time, the time required for VDDL and GNDL rails to stabilize is reduced by up to 81.16%.

6. REFERENCES

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