TUTORIAL 3

RECENT ADVANCES IN FORMAL VERIFICATION

Speakers:

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Background: Recent progress in model checking techniques has allowed formal verification to be applied to larger and more complex design blocks. This tutorial will examine some of the recent methods that have led to a remarkable expansion in the capacity of formal verification tools. The tutorial will be divided into three parts. The first section will discuss iterative abstraction methods. One key to verifying assertions in larger designs is to be able to automatically determine which parts of a design are relevant to a given property. In the past few years, a number of new techniques have been developed for this purpose. This has made it possible in many cases to verify assertions on designs blocks with thousands of registers. The second portion will cover the role of Boolean SAT solvers in model checking. Many recent model checking approaches make use of Boolean satisfiability solvers. We will look at how SAT solvers work, why and in what cases they can be applied effectively to large problems, and how they can be exploited in model checking. The final section will cover predicate abstraction. This approach has made it possible to apply model checking to verify properties of relatively large pieces of software, such as device drivers in the Windows and Linux kernels.

The tutorial is intended for designers and CAD engineers interested in next generation formal verification methods. Basic background of VLSI and CAD is useful though not needed.