Mixed Signal DFT: A Concise Overview

Bozena Kaminska, Comet Microsystems
Karim Arabi, PMC-Sierra

Abstract

Practical mixed-signal DFT solutions are presented with an emphasis on performance, cost, and test coverage. Special consideration is given to the possible DFT techniques for Phase-Locked Loops (PLLs) with associated implications on test coverage, performance, cost, and time to market. An introduction to practical DFT techniques for data converters (A/D and D/A) follow. An overview of IEEE P1149.4 analog test bus standard concludes the embedded tutorial.

1. Introduction

The demand for system-on-a-chip (SoC) devices has stretched tools' capabilities beyond their practical limits to keep pace with design productivity. As a result new tools and development flows are needed that will be able to handle the greater design challenges. The verification and test are the areas in which the limits of today's tools are making SoC design harder, longer, and less efficient

There is a trend of increasing use of Design-For-Test (DFT) methodologies that focus on testing the structure of a design rather than its macro functionality. DFT with the purpose of testing the structure of the device is called Structural DFT. This trend is being driven by several factors. The traditional driving forces for use of DFT have been, and remain, observability into the design for diagnostics and system check out and achieving acceptable fault coverage levels, typically between 95% and 98%, in a predictable time frame. With the advent of SoC methodologies, DFT is being used to provide test portability for reusable Intellectual-Property (IP) blocks or cores. Additionally, DFT tools have advanced to permit a more comprehensive device test that, in some cases, has been proven to eliminate the need for traditional functional test. As a consequence of these advances, DFT methods are seen as an enabling technology to break the cost trend. This reduced cost trend will cause a shift in the market acceptance of these non-traditional methods over traditional methods.

On the contrary, mixed-signal DFT is mainly focused on facilitating functional testing of the circuit under test. This trend may change if the structural DFT techniques prove to be aggressively more cost effective. This paper focuses on current mixed-signal DFT techniques practiced in industry. In particular, the detailed overview of test techniques for PLL and its jitter is provided. Currently, oscillation-based approaches seem to be among the most popular mixed-signal DFT techniques in practical implementations. Since the original introduction of the oscillation methodology [2 to 6], many researchers successfully explored better implementations and expanded applications [16]. The popularity of oscillation based DFT techniques results from the following main characteristics:

- Applicable to various functional modules: analog, mixed signal, digital, and MEMS devices
- Signal generator is not required
- Immune to noise
- Deliver very good fault coverage for parametric, hard and functional errors
- Easy to implement with little cost

2. PLL Testing

PLL testing has gained significant interest recently due to the widespread integration of PLLs in mixed-signal communications and data processing devices. Mixed-signal devices embedding PLLs are normally sensitive to input jitter (time distortion) and level distortion. For example, to guarantee proper data reception in any network the transmitter and receiver must meet a certain budget of jitter.

Before discussing how to measure jitter, it is important to distinguish what jitter means for two application areas: non-communication applications,

Permission to make digital or hard copies of all or part of this work for personal or classroom use is granted without fee provided that copies are not made or distributed for profit or commercial advantage and that copies bear this notice and the full citation on the first page. To copy otherwise, to republish, to post on servers or to redistribute to lists, requires prior specific permission and/or a fee.
ICCAD'03, November 11-13, 2003, San Jose, California, USA.
Copyright 2003 ACM 1-58113-762-1/03/0011 ...$5.00.

for example processors, and serial-communication applications. In the first case jitter is defined as the variation of the clock period and is referred to as period jitter or cycle-to-cycle jitter. The measure of the phase variation between the PLL's input and output clocks is known as a long term or tracking jitter. In serial data communication, on the other hand, jitter is defined as the short-term variation of a digital signal's significant instants—for example, rising edges with respects to their ideal position in time. Such a jitter is known as accumulative jitter and is described as a phase modulation of a clock signal. Jitter sources can come from power supply noise, thermal noise from the PLL components and limited bandwidth of the transmitting media. There are some applications where the absolute jitter is important, for example in clock synthesis circuits; there is a need for a use of a jitter-free or low jitter reference signal. The difference between the position of corresponding edges of the signal of interest and the reference signal indicates the jitter.

Table 1: *A comparison of the four different ways to measure jitter*

	ATE Testers	Real-Time Sampling Oscilloscope	Dedicated Instrumentation	BIST/DFT
Performance	Limited accuracy, resolution, and throughput	Very high accuracy resolution, and throughput	High accuracy, resolution, moderate throughput.	High accuracy, resolution, and throughput.
Additional Hardware	None or Dedicated Instrumentation	High-speed digitizer system per channel	Digital jitter measurement system per ATE.	Modular, flexibility with different levels of integration.
Additional Software	Minimal	Significant signal processing and application-specific code	Insignificant signal processing and application specific code	Insignificant signal processing and application specific code
Application:	>30psec jitter in CMOS ICs. Production test	1-5 psec jitter on a few critical signals/clocks. Precise characterization of communications channels, optical fiber clocks, prediction of bit error rate.	: > 1 psec jitter. Clock jitter, serial data communications, carrier jitter in integrated RF subsystems	1 or more psec jitter in ICs. Clock , data jitter, serial data communication, measurements in a noisy environment

3.1 Review of Jitter Measurement Techniques

From user perspective there are three established ways of making jitter measurements: using ATE equipment, a real-time sampling oscilloscope or a dedicated jitter measurement instrument. Because jitter is becoming such an important factor in overall system performance, it is worthwhile to examine the pros and cons of using each of these techniques. A fourth technique based on built-in self-test (BIST) or just DFT has recently emerged.

Spectrum Analyzer Measurement

An analog spectrum analyzer can be used to measure the jitter of a signal in the frequency domain in terms of phase noise. For this measurement the jitter is modeled as phase modulation. For example a sine wave signal is represented as a perfect sine wave with amplitude and phase modulation. With a spectrum analyzer one can measure the power of the signal as a frequency with wide dynamic range, however one cannot distinguish between the amplitude and phase modulation components. A common

assumption made when using a spectrum analyzer to measure jitter is that the amplitude modulation component of the signal is negligible. This assumption may be valid for signal internal to a pure digital system where undistorted square waves or pulse are the norm. This assumption is typically not true for a serial communication or data channel. Isolating the noise from the actual signal frequency components and translating that into jitter is non-trivial.

Real-time Time Interval Analyzer Measurements

This technique measures the time interval between a reference voltage crossing of the transmitted signal. There is no need for an abstract model of the signal when using this technique because the time intervals are measured directly. The real-time interval analyzer gives complete knowledge of the nature of the jitter and the components of the jitter. With this measurement technique the position and time of every edge is measured, thus allowing statistical space and frequency-based models of the signal, as well as absolute peak-to-peak measurements. The clear advantages of this technique are the facts that there are no skipped edges and measurement acquisition time is limited only by the signal itself. In practice, instrumentation that has the necessary acquisition rate and resolution to test gigabit data rates does not exist.

Repetitive Start/Stop Measurements

This is a common technique that gives high resolution and accuracy using a direct time measurement. Time measurements are normally made by starting a counter on the first occurrence of an edge, and stopping the counter on the next edge. Enhancements to this technique include skipping multiple edges for cumulative measurements, comparing two different signals, and time interpolation for achieving resolution greater than the counter clock period. Retriggering of time interval measurement normally requires a significant dead time, particularly when time interpolation is used. After collecting many of these time interval measurements, post processing is applied to extract statistical parameters and jitter components. This technique has been used to good effect in ATE equipment to measure jitter of low frequency clock (<100MHz) or in some bench top instrument implementations such as Wevecrest that include special software features for jitter component characterization.

ATE-Based

Using automatic tester equipment, a signal may be repeatedly acquired at slightly different time settings for the capture clock. The distribution of signal timing can be determined from the average number of successful acquisitions at each clock setting. Although using ATE equipment lowers the cost for those designers that have test equipment, it does take some time to make multiple acquisitions of a given transition. What is more of a concern is that the accuracy and resolution are limited by the tester resolution, accuracy, and jitter. One plus is that the processing load imposed on the tester's computer is minimal.

Real-time Digital Sampling Oscilloscope

When using a real-time digital sampling oscilloscope to measure jitter, a signal is acquired by the oscilloscope's over-sampling clock and transitions through a fixed voltage threshold that is determined by filtering and interpolation. The variation of the transitions with respect to a fixed clock is interpreted with special jitter software. Advanced real-time oscilloscopes are typically used to measure 1-5 ps jitter on a few critical signals/clocks for precise signal characterization in communications channels, optical fiber clocks, and predicting the bit error rate. Making jitter measurements with an oscilloscope requires a high-speed digitizer on each of the instrument's channels, along with a high-speed memory system and possibly DSP hardware. The oscilloscope's system has the potential for very high throughput and accuracy because the signal is being continuously observed and the threshold transitions can be interpolated to very high precision, in part because of the oscilloscope's multi-bit acquisition.

The drawbacks of this approach is that the processing load can be quite high and increases with the channel count, so it may become impractical to realize a tolerable throughput when there are multiple channels involved. Moreover, the power dissipation in practical systems is on the

order of 15 watts per channel, so large channel counts may become problematical for this reason too. Also with most oscilloscopes, when the full complement of channels are in use, the sampling acquisition is no longer continuous, so the probability of capturing infrequent jitter faults drops off quickly.

Dedicated Jitter Instrumentation

Dedicated jitter instrument hardware is used to measure jitter directly and report the result as a number. A dedicated jitter measurement instrument is used, offloading the measurement burden from the ATE or oscilloscope. However, since jitter measurements are now made independent of general-purpose equipment, the overall test time is increased to accommodate these special measurements. Moreover, a method must be provided to switch the measurement system to the required channels. There are two main providers of these instrumentation: Wavecrest and Guidetech. Guidetech's hardware is based on time-interval-analyzer (TIA) technology, whereas Wavecrest's hardware is based on counter-timer technology. TIAs create precise timesteps of trigger events, and within limits (Guidetech's limit is 2 million triggers/sec) can measure the timing of every trigger event. At higher frequencies, however, TIAs can make precise measurements only on some fraction of all of the cycles received. Counter-based, on the other hand, make timing measurements by "stretching" cycles, for example by ramping an analog integrator rapidly until a trigger event is detected and then ramping the integrator slowly back down to zero so that a relatively low-speed counter can measure the ramp-down time. This technique is allegedly slower than that used in TIAs, and, in the case of the Wavecrest boxes, limits the maximum frequency of signals that can be completely sampled (sampled in every cycle) to about 30,000 waveforms/sec.

BIST and DFT

All the methods discussed above rely on external measurement equipment to examine jitter. In contrast, new BIST/DFT approaches can be used for SoC/ICs that exhibit jitter as low as 1-5 ps. Applications can include clock and data jitter, differential jitter, serial data communications, and measurements in a noisy environment

3.2 DFT/ BIST for PLL Testing

The PLL test circuit, DFT/BIST, which follows the oscillation methodology, is based on the Vernier principle transposed to the time domain. Due to a very high measurement resolution, it is practical to measure the frequency and the jitter of PLL circuits. As Vernier caliper allows for a precise measurement of a linear distance between two points, the same principle applied in a time space allows for a precise measurement of time interval between two events. Instead of two linear scales having a very small difference in linear step, two oscillators with a very small difference in oscillation frequency are used for PLL test circuit. The measurement resolution is that of time difference between the periods of two oscillators. These oscillators have two essential characteristics:

1) When triggered, the oscillation will start virtually instantaneously and with a fixed phase relationship to the external trigger pulse.
2) When oscillating, the stability of the frequency is preserved.

The system uses phase-startable oscillators called start and stop oscillators. The stop oscillator has a slightly shorter period of oscillation than the start oscillator such that once started, they will reach coincidence after some number of cycles later dependent on measured time interval. If the reference (start) oscillator period is T_0 then the stop oscillator has period equal to $T_1=T_0 - \Delta T$ where ΔT is a difference between periods of both oscillators. A time interval T used to trigger the start and stop oscillators can be derived using the following equation:

$$T = N_1 T_0 - N_2 T_1 = N_1(T_0 - T_1) = n\Delta T$$

Where N_1 is the number of start oscillator pulses to coincidence and N_2 is the number of stop oscillator pulses to coincidence. If the time interval T is much smaller than the start and stop oscillation period, we can assume that $n=T_1 \approx T_2$. Another important assumption is that the delta between start and stop oscillator periods is much smaller than the time interval T.

A practical limitation on the interpolation factor *n* is imposed by the inherent noise and there is little advantage to be gained by having an interpolation factor capable of giving resolutions substantially better than this. Recent implementations give around 10 ps of single shot resolution.

The high single shot resolution allows the collection of meaningful statistical information. Important characteristics concerning time intervals like max., min., standard deviation values are collected in addition to the mean value. With low speed data collection, full histogram-building information is obtained. In many time interval measurement situations these statistical properties are of prime importance. For example, in PLL jitter testing the standard deviation gives an excellent indication of jitter.

In all practical implementations, the test circuit contains two matched phase-startable oscillators. A coincidence detector detects the coincidence. The test circuit consists of two main parts: the functional circuit and the result processing circuit and/or software. The functional circuit is equivalent to about 2000 to 2500 gates, depending on the implementation. For result processing different techniques can be adopted depending on the application requirements. It can be a hardware implemented DSP technique (such as histogram building; used by Fluence) or custom software module [17]. The result processing is, in general, very fast, and can easily be executed in real time. The dedicated algorithms for fast performance computation include: RMS and peak-to-peak jitter, instantaneous period, frequency, phase jitter, delay, and similar characteristics.

Besides its impressive jitter measurement capability, there are a multitude of benefits that flow from this DFT approach to PLL measurement. First, the dedicated test circuit based on DFT approach requires only minor tester capabilities, which in turn lowers test cost development and equipment requirements. The test circuit can be placed directly on a low cost tester [17] or can follow the integrated implementation. In the case of fully integrated version, time dependent process variations incurred during the fabrication of the SoC/IC can have an impact on the jitter of the oscillators used in the test circuitry. What should be noted is that the oscillator itself can inject jitter depending on process variations. Basically, there are two types of jitter that can occur in these particular situations. The first is the correlated jitter where the two oscillation frequencies vary in time but always the same amount. This jitter will only impact the absolute value of the frequencies but the difference will remain constant. The second type of jitter is the non-correlated one and it impacts the difference between the two frequencies. The latest has the greatest impact on the DFT approach to measuring jitter and should be analyzed and minimized.

With a MonteCarlo simulation, it is only possible to quantify the impact of the static variations—those variations that do not change with time. Injecting time dependent variation involves an indirect use of the simulation where the variation are generated externally and injected in the simulation as noise sources.

Other DFT/BIST techniques for PLL testing are reported in [7,8,9]. Each of them has, however, an important technical limitation and as a result a limited applicability.

4. A/D and D/A Testing

Among frequently used mixed-signal circuits, data converters are typical mixed-signal devices that bridge the gap between analog and digital world. They determine the overall precision and speed performances of the system and therefore dedicated test techniques should not affect their specifications. For instance, it is difficult to test the analog and the digital portions of data converters separately using structural test methods and conclude that the whole device specifications are fully respected. Therefore, it is necessary to test data converters as an entity using at least some functional specifications. There is also a strict requirement in terms of precision related to hardware used to test data converters. Most of efforts in on-chip testing data converters are devoted to ADC converters. In [13] and [14], conventional test techniques have been applied to the ADC under test using a micro-controller available on the same chip. Oscillation-test strategy is a promising technique to test mixed-signal circuits and is very practical for designing effective BIST circuits [6].

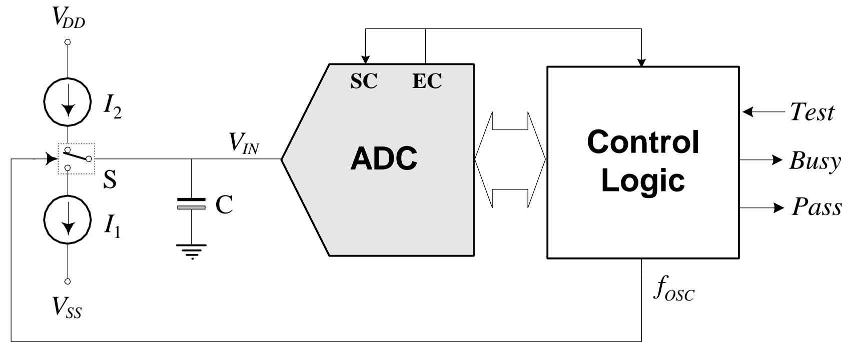

Figure 1: Oscillation-test method used to apply BIST to ADCs.

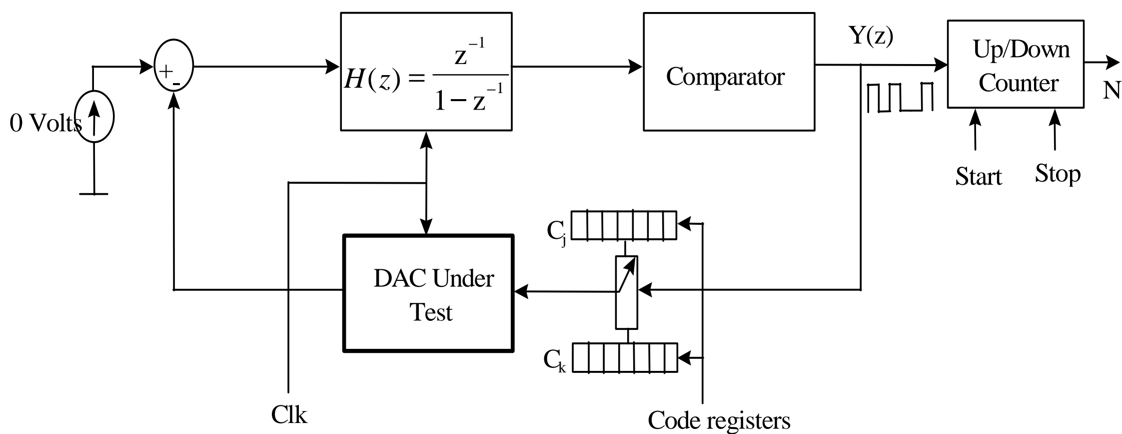

Figure 2: Oscillation-test used to apply BIST to embedded DACs.

Based on oscillation-test method, in [6] the ADC under test is put into an oscillator and the system oscillates between two pre-established codes by the aid of some small additional circuits in the feedback loop. Functional specifications such as offset, DNL, INL, and gain error are then evaluated by measuring the oscillation frequency of the circuit under test. This technique has the advantage of delivering a digital signature that can be analyzed on-chip or by a conventional digital tester. Testing ADC-DAC pairs has been addressed in [15]. Such techniques use the DAC to apply analog stimuli to the ADC under test and use the ADC to convert DAC under test signatures to digital. Three problems have to be considered for these techniques. First, it is limited to applications where one can find a ADC-DAC pair on the same IC. Second, the ADC (or DAC) used to test the DAC (or ADC) should have at least 2-bits of resolution more than the DAC (or ADC) under test. The third problem is fault masking in which a fault in DAC (or ADC) compensates another fault in ADC (or DAC). Therefore, it is very important to be able to test DAC or ADC individually without using another data converter. The only BIST approach for solitary DACs has been proposed in [18] that verifies all static specifications using some additional analog circuitry and a control logic. The accuracy of the analog circuitry limits the test precision and authors propose an auto-calibration scheme to overcome this limitation.

The main difficulty when dealing with BIST for DAC is the analog nature of its output signal that requires to design high resolution but still area efficient analog signature analyzers. Oscillation-test strategy [6,16] deals with this problem by establishing a closed-loop oscillation including the circuit under test in which one does not have

to apply analog input stimuli and the test output is a pure digital signal.

Figure 1 and 2 show the implementation of oscillation-test method to apply BIST to embedded data converters. Other relevant references include [11 to 15].

5. Analog Test Bus Standard

The significant advancement in mixed signal DFT area is the IEEE P1149.4 bus standard. It is a new IEEE standard that aims at providing a complete solution for testing analog and digital I/O pins and the interconnection between mixed-signal ICs. The secondary objective is to provide access to internal cores based on the Test Access Bus concept. It includes IEEE 1149.1 boundary scan Test Access Port (TAP) controller and therefore provides a support infrastructure for BIST and test set-up. Figure 3 shows the IEEE P1149.4 architecture that includes the following elements:

- Test Access Port (TAP) comprising a set of four dedicated test pins: Test Data In (TDI), Test Data Out (TDO), Test Mode Select (TMS), Test Clock (TCLK), and one optional test pin: Test Reset (TRSTn).
- Analog Test Access Port (ATAP) comprising two dedicated pins: Analog Test Stimulus (AT1) and Analog Test Output (AT2), and two optional pins: Inverse AT1 (AT1n) and Inverse AT2 (AT2n) for differential signals.
- Test Bus Interface Circuit (TBIC).
- An Analog Boundary Module (ABM) on each analog I/O.
- A Digital Boundary module (DBM) on each digital I/O.
- A standard TAP Controller and its associated registers.
-

6. Conclusions

This embedded tutorial presents a concise overview of practical mixed-signal DFT techniques with the emphasis on PLL and jitter testing. The practical aspects of A/D and D/A converter testing using DFT approaches have also been reported followed by the IEEE analog test bus standard highlights. Popular analog and mixed-signal DFT techniques are designed based on functional testing of the circuit under test. Mixed-signal DFT remains an ad-hoc solution practiced by analog designers until an automated way of synthesizing analog blocks gain popularity in semiconductor industry. Mixed-signal BIST is being used as an integral part of design process for high-accuracy or high-resolution analog circuits. Therefore, it is only a matter of awareness and education to enable current mixed-signal designers to apply mixed-signal BIST to their next design.

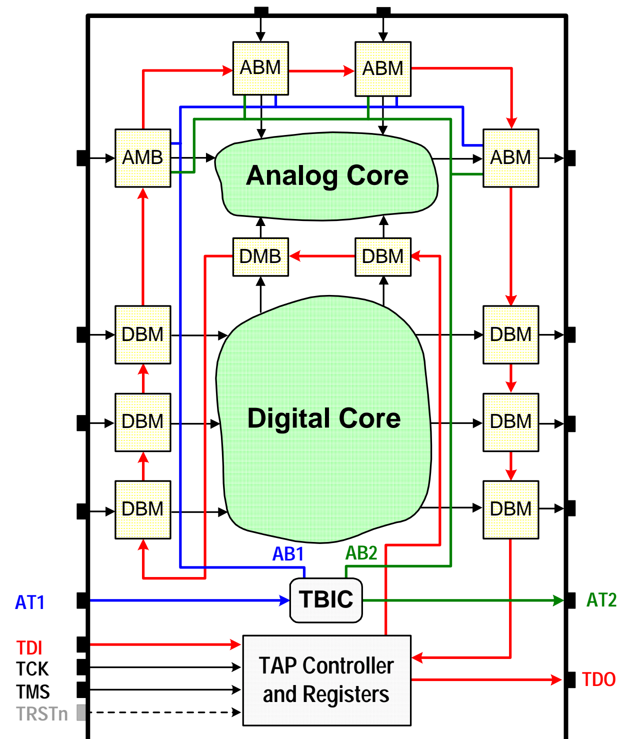

Figure 3: IEEE 1149.4 architecture.

References:

[1] Roberts, G., “Metrics, Techniques and Recent Developments in Mixed Signal Testing”, ICCAD, Nov. 1996.

[2] K. Arabi and B. Kaminska, “Oscillation – Based Test Method for Testing an at Least

Partially Analog Circuit", ***US Patent 6,005,407***, December 1999.

[3] K. Arabi and B. Kaminska, "Design for Testability of Embedded Integrated Operational Amplifiers", ***IEEE Journal of Solid-State Circuits***, April 1998, vol.33, no.4, pp.573-581

[4] K. Arabi and B. Kaminska, "Oscillation Test Method for Low Cost Testing of Active Analog Filters", ***IEEE Trans. on Instrumentation and Measurement***, Vol 48, Number 4, August 1999, pp 798-806

[5] K. Arabi, HS, H., Dufaza, C., Kaminska, B., "Digital Oscillation Test Method for Delay and Structural Testing of Digital Circuits", ***IEEE ITC***, October 1998, pp. 91-100.

[6] K. Arabi, and Kaminska, B., «Oscillation Buit-In Self-Test Scheme for Functional and Structural Testing of Analog and Mixed-Signal Integrated Circuits», ***IEEE ITC***, November1997,pp.786-795.

[7] Sunter, S. and Roy, A., "BIST for PLL SIN digital Applications", IEEE International Test Conference, Sept. 1999, pp.532-540.

[8] Kim, S., and Soma, M., "An Efficient Defect Oriented BIST for High-Speed PLL", IEEE VLSI Test Symposium, Montreal 2000, pp.231-236.

[9] Veillette, B. and Roberts. G., "On-Chip Measurement of the jitter transfer function of PLL", IEEE International Test Conference, 1997, pp. 776-785.

[10] C. Browing, "Testing A/D Converter on Microprocessors," Proc. IEEE ITC, 1985, pp. 818-824.

[11] R. Bobba et al. "Fast Embedded A/D Converter Testing Using the Microcontrollers' Ressources," Proc. IEEE ITC, 1990, pp. 598-604.

[12] E. Teraoca et al. "A Built-In Self Test for ADC and DAC in a Single Chip Speech Codec," Proc. IEEE ITC, pp. 791-796.

[13] R. Norworthy, R. Schreier and G.C. Temes, "Delta-Sigma Data Converters: Theory, Design, and Simulation," IEEE press, 1997.

[14] P.M Aziz, H.V. Sorensen and J. Van Der Spiegel, "An Overview of Sigma-Delta Converters," IEEE Signal Processing Magazine, January 1996, pp. 61-84.

[15] J. G. Kenney and L.R. Carley, "Design of Multibit Noise-Shaping Data Converters," Journal of Analog Integrated Circuits and Signal Processing, vol. 3, May 1993, pp. 259-272.

[16] D.Vazquez,G.Huertas,g.Leger,A.Rueda,J.L .Huertas,"On-Chip Evaluation of Oscillation-Based test", Analog IC and Signal Proc., Kluwer Pub.,Vol 33, 2002

[17] B.Kaminska, E.Sokolowska,"Floating Infrastructure IP", IMSTW2003,pp221-226

[18] K. Arabi, B. Kaminska and J. Rzeszut, "BIST for D/A and A/D Converters," IEEE Design & Test of Computers, 1996, pp. 40-49.