POWER-OPTIMAL SIMULTANEOUS BUFFER INSERTION/SIZING AND WIRE SIZING

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ABSTRACT

This paper studies the problems of minimizing power dissipation of an interconnect wire by simultaneously considering buffer insertion/sizing and wire sizing (BISWS). We consider two cases, namely minimizing power dissipation with optimal delay constraints, and minimizing power dissipation with a given delay penalty. We derive closed form optimal solutions for both cases. These closed form solutions can be used to efficiently estimate the power dissipation in the early stages of the VLSI designs. We observe that the power dissipation can be much different even with the same optimal delay.

1. INTRODUCTION

With the development of deep submicron (DSM) very large scale integrated (VLSI) designs, the interconnect delay becomes the dominant factor in the performance of these IC designs. In order to reduce the interconnect delay, many methods have been proposed such as parallel regeneration, driver and sink sizing, buffer insertion, wire sizing and simultaneously buffer insertion/sizing and wire sizing [1], [2], [3], [6], [7], [12], [14]. Some tutorials can be found in [6], [10], [11]. Since the interconnect delay is quadratically proportional to its wire length, buffer insertion is one of the most effective methods to decrease global interconnect delay. After buffer insertion, the long wires are broken into a lot of short wire segments and the optimal delay of a buffered wire is linear in its length [1]. With the technology scaling, it is expected that more and more buffers should be inserted for high-performance VLSI designs (about 800,000 for 50nm technology estimated in [9]). The introduction of such a large number of buffers will increase the power consumption which exacerbates the power dissipation issue because of the technology scaling. A lot of references address the power dissipation issue during the buffer insertion. Lillis el al [15] presented optimal polynomial algorithms to minimize dynamic power dissipation while satisfying given timing

constraints for the wire sizing/buffer insertion problems. Turgis et al [16] discussed the buffer insertion limits and the application to the buffer design to satisfy minimum power delay product constraint. Zhou and Liu [19] considered the problem of minimizing the circuit area and power dissipation subject to delay constraints by buffer sizing. Nalamalpu and Burleson [17], and Adler and Friedman [18] also addressed the issue of optimizing buffer insertion and power dissipation. Banerjee and Mehrotra [4] discussed the power-optimal buffer insertion for global interconnects in Nanometer designs. They developed a methodology to compute the repeater size and interconnect length that minimizes the total interconnect power dissipation for a given delay penalty for a uniform long line. However, these discussions for the power dissipation in the buffer insertion either ignore the leakage power [15], [16], [19], [18], or ignore both the leakage and short-circuit power [17], [18], [19], or only consider the buffer sizing for a uniform line ignoring the wire sizing [4], [16], [17], [18], [19]. Furthermore most of these discussions were algorithmic, and did not provide closed form solutions. Chu and Wong [6] derived elegant closed form solutions to minimize the interconnect delay for simultaneous buffer insertion/sizing and wire sizing. They obtained closed form solutions for three versions. The first version is wire sizing (WS) without buffer insertion. The second version uses fixed number of buffers (version BISWS/m), and the third version uses the optimal number of buffers (version BISWS). They mathematically proved some frequently used optimal results such as the use of equal-length wire segments is optimal. But they did not analyze the power dissipation during the simultaneous buffer insertion/sizing and wire sizing. We notice that when the optimal delay for BISWS (BISWS/m) is achieved, the optimal solution is not unique. However, the power dissipation corresponding to different solutions which achieve the same optimal delay can be much different. We simulate the power dissipation corresponding to different optimal delay solutions given by [6] using SPICE3 for a wire with length=$4000\mu m$, ten wire segments, and one buffer (version BISWS/1). The driver and load are 50 times minimum device. The result is shown in Figure 1, from which we can see the maximum power dissipation is more than 3 times of its minimum with the same optimal delay. Since power dissipation becomes a serious issue in the DSM VLSI design, it is very important to minimize the power dissipation while satisfying delay constraints.

In this paper, we study the problem of minimizing power dissipation of an interconnect wire by simultaneously considering buffer insertion/sizing and wiring sizing (BISWS). We consider two cases, namely minimizing power dissipation with optimal de-
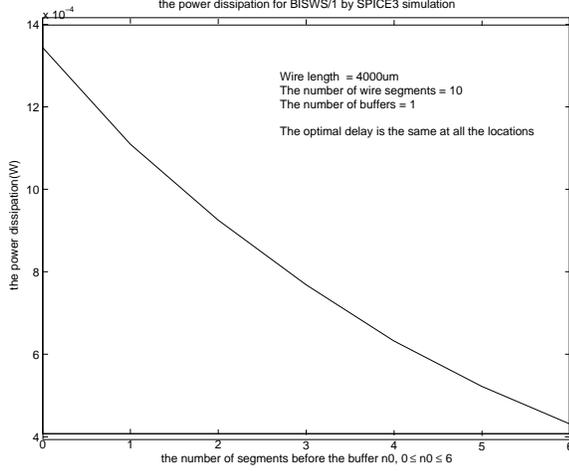
Figure 1: Power dissipation variation with optimal delay simulated by SPICE3 with $0.18\mu m$ technology

lay constraints, and minimizing power dissipation with a given delay penalty. Our main contributions are as follows, (1) we derive closed form optimal solutions to the problem of minimizing power dissipation while satisfying delay-optimal constraints for BISWS and BISWS/m. These closed form solutions can be used to efficiently estimate the power dissipation in the early stages of the VLSI designs. (2) we derive closed form optimal solutions to the problem of minimizing power dissipation without delay-optimal constraints but with delay penalty for BISWS and BISWS/m. This is very important in the sense that it is believed that the total power dissipation is excessive for the delay-optimal buffer insertion [4]. Our solutions provide efficient methods for the power-delay trade off.

The rest of the paper is organized as follows. In section 2, we give the preliminaries for BISWS (BISWS/m) and power dissipation. In section 3, we discuss the power dissipation minimization problems for BISWS (BISWS/m) with optimum delay. In section 4, we consider the power dissipation minimization problems for BISWS (BISWS/m) with delay penalty. Section 5 is the experimental results. Section 6 gives conclusion.

2. PRELIMINARIES

In this paper, we use the following notations of parameters, some of which are used in [6] or [4].

R_D: driver resistance
C_L: load capacitance
r_0: unit square wire resistance
c_0: unit area wire capacitance
r_e: effective output resistance of a minimum device
c_g: gate capacitance of a minimum device
c_d: drain capacitance of a minimum device
V_{DD}: power supply voltage
f: clock frequency
$I_{off_n}(I_{off_p})$: leakage current per unit NMOS (PMOS) transistor width
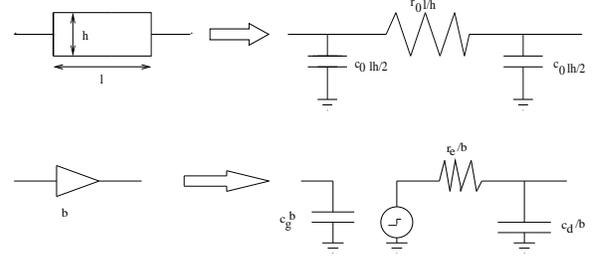$W_{n_{min}}(W_{p_{min}})$: width of the NMOS (PMOS) transistor in minimum sized inverter

Figure 2: Wire and Buffer model

We model a wire segment as a π-type RC circuit and a buffer as switch-level RC circuit as shown in Figure 2. Elmore delay model [13] is used to calculate the delay of a circuit.

2.1. Simultaneous Buffer Insertion/Sizing and Wire Sizing Problem

The simultaneous Buffer Insertion/Sizing and Wire Sizing problem (BISWS) [6] is defined as follows: given wire length L, the driver resistance R_D, the load capacitance C_L, and the total number of segments n to be used, minimize the delay D from source to sink over the number of used buffers m, the number of segments n_j ($0 \le j \le m$) between the jth buffer and the $(j+1)$th buffer (with n_0 being the number of wire segments between the source and the first buffer and n_m being the number of segments between the last buffer and sink), the length l_i and the width h_i ($1 \le i \le n$) of ith segment, and the size of jth buffer b_j ($0 \le j \le m$), with constraints $n_0 + n_1 + \cdots + n_m = n$ and $l_1 + l_2 + \cdots + l_n = L$. For BISWS, Chu and Wong obtain closed form optimal solutions (THEOREM 3 in [6]). By their results, when

$\quad m = the\ better\ one\ of\ \lfloor \hat{m} \rfloor\ and\ \lceil \hat{m} \rceil,$
where

$$\hat{m} = \left(ln \frac{r_e c_g}{R_D C_L \hat{\beta}} \left(1 + \frac{S\hat{\beta}}{2} - \sqrt{S\hat{\beta} + \left(\frac{S\hat{\beta}}{2}\right)^2} \right) \right) / ln\hat{\beta},$$
$$and\ \ (\frac{1}{e\hat{\beta}})^{1/\hat{\beta}} = e^{c_d/c_g},$$

$$(2.1)$$

$n_j = $ an arbitrary nonnegative integer, for $0 \le j \le m$,
$\quad\quad$ such that $n_0 + n_1 + \cdots + n_m = n$,
$b_j = \frac{r_e}{R_D} \frac{\alpha^{s_j}}{\beta^j}, for\ 1 \le j \le m$,
$l_i = \frac{L}{n}$,
$h_i = \sqrt{\frac{r_0 C_L}{c_0 R_D} \frac{\beta^m}{\alpha^{n-1}}} \frac{\alpha^{i-1}}{\beta^j}, for\ 1 \le i \le n$,
$\quad\quad$ with j being the index such that $s_j + 1 \le i \le s_{j+1}$,
$S = \frac{r_0 c_0 L^2}{r_e c_g n^2}$,
$\beta = \frac{(1-\alpha)^2}{S\alpha}$,

$$(2.2)$$

where

$$s_i = n_0 + n_1 + \cdots + n_{i-1}, \quad\quad (2.3)$$

and α is the unique root between 0 and 1 of

$$g(\alpha) = \sqrt{\frac{r_e c_g}{R_D C_L}} S^{(m+1)/2} \alpha^{(n+m+1)/2} - (1-\alpha)^{m+1} = 0,$$

$$(2.4)$$

the optimum delay D_{opt} is given by

$$D_{opt} = mr_e c_d + \frac{r_0 c_0 L^2}{2n^2} \frac{n + 2(m+1)\alpha - n\alpha^2}{(1-\alpha)^2}. \quad (2.5)$$

The problem of simultaneous Buffer Insertion/Sizing and Wire Sizing problem with m buffers (BISWS/m) is the same as BISWS except m is a given input. The solutions for BISWS/m are in the same forms as (2.2)-(2.5) except the value of m is given by input. In the following we simplify the expression of h_1 for the latter use.

Finding h_1 from (2.2), then substituting β and S in (2.2) into the expression of newly obtained h_1, we have

$$h_1 = \sqrt{\frac{r_0 C_L}{c_0 R_D} \frac{(1-\alpha)^{2m}}{\alpha^{n+m-1} S^m}}. \qquad (2.6)$$

From (2.4), we have,

$$\alpha^{n+m-1} S^m = \frac{R_D C_L (1-\alpha)^{2m+2}}{r_e c_g \alpha^2 S} = \frac{n^2 R_D C_L (1-\alpha)^{2m+2}}{r_0 c_0 L^2 \alpha^2} \qquad (2.7)$$

substitute (2.7) into (2.6),

$$h_1 = \frac{\alpha r_0 L}{n R_D (1-\alpha)}. \qquad (2.8)$$

2.2. Power Dissipation

The power dissipation of a buffer consists of switching power, leakage power and short-circuit power [5]. With the technology scaling, the leakage power and short-circuit power occupy a large percentage of total power dissipation. The total power dissipation is computed using the similar formulae in [4]. For detail, please see the reference.

3. OPTIMAL POWER DISSIPATION WITH OPTIMUM DELAY FOR BISWS (BISWS/M)

It is noticed that the optimal delay solution (2.1)-(2.5) for BISWS has no further restriction over the parameters $n_j (0 \leq j \leq m)$ except $n_0 + n_1 + \cdots + n_m = n$. However the different assignments of n_j may affect the total power dissipation. As power dissipation becomes a serious issue in DSM IC designs, it is important to maintain power dissipation minimum while satisfying delay requirements. In the next, the power-optimal problems over $n_0, n_1, \cdots n_m$, satisfying the delay-optimal constraint for simultaneous buffer insertion/sizing and wire sizing problems are considered. We formulate the power-optimal BISWS/m (BISWS) with optimum delay problem named POBISWSOD/m (POBISWSOD) as follows.

Power-optimal Simultaneous Buffer Insertion/Sizing and Wire Sizing with m buffers satisfying Optimum Delay constraint problem (POBISWSOD/m): Given a BISWS/m problem, the objective is to minimize the total power dissipation over $n_j (0 \leq j \leq m)$ satisfying (2.2)-(2.5).

Power-optimal Simultaneous Buffer Insertion/Sizing and Wire Sizing with Optimum Delay problem (POBISWSOD): Given a BISWS problem, the objective is to minimize the total power dissipation over $n_j (0 \leq j \leq m)$ satisfying (2.1)-(2.5).

3.1. POBISWSOD/m Problem

For a given BISWS/m problem, we first find its optimal solutions by (2.2)-(2.5), then compute the total power dissipation. The total power dissipation is the sum of switching power (P_{switch}), short-circuit power (P_{short}) and leakage power ($P_{leakage}$), i.e.

$$P_{total} = P_{switch} + P_{short} + P_{leakage}.$$

In the following, we compute P_{switch}, P_{short}, and $P_{leakage}$ using the similar basic formulae in [5, 4].

3.1.1. Switching Power

The switching power is computed as following,

$$
\begin{aligned}
P_{switch} = \quad & V_{DD}^2 f \delta [c_0 (l_1 h_1 + l_2 h_2 + \cdots + l_{s_1} h_{s_1}) + c_g b_1 \\
& + c_d b_1 + c_0 (l_{s_1+1} h_{s_1+1} + \cdots + l_{s_2} h_{s_2}) + c_g b_2 \\
& + \cdots \cdots \\
& + c_d b_m + c_0 (l_{s_m+1} h_{s_m+1} + \cdots + l_{s_{m+1}} h_{s_{m+1}}) \\
& + C_L]
\end{aligned}
\qquad (3.1)
$$

where δ is the switching factor, which is the fraction of buffers on a chip that are switched during an average clock cycle. δ can be 0.15 [5].

Substituting the parameters $l_i, h_i (1 \leq i \leq n)$ and $b_j (1 \leq j \leq m)$ of (2.2) and h_1 of (2.8) into (3.1), we have,

$$
\begin{aligned}
P_{switch} = \quad & \frac{V_{DD}^2 f \delta r_0 c_0 \alpha L^2}{n^2 R_D (1-\alpha)^2} [(\frac{\alpha^{s_1}}{\beta} + \frac{\alpha^{s_2}}{\beta^2} + \cdots + \frac{\alpha^{s_m}}{\beta^m}) \\
& - (\alpha^{s_1} + \frac{\alpha^{s_2}}{\beta} + \cdots + \frac{\alpha^{s_m}}{\beta^{m-1}})] \\
& + \frac{V_{DD}^2 f \delta r_e}{R_D} (c_g + c_d)(\frac{\alpha^{s_1}}{\beta} + \frac{\alpha^{s_2}}{\beta^2} + \cdots + \frac{\alpha^{s_m}}{\beta^m}) \\
& + \frac{V_{DD}^2 f \delta r_0 c_0 \alpha L^2}{n^2 R_D (1-\alpha)^2} - \frac{V_{DD}^2 f \delta r_0 c_0 \alpha L^2}{n^2 R_D (1-\alpha)^2} \frac{\alpha^n}{\beta^m} + V_{DD}^2 f \delta C_L.
\end{aligned}
\qquad (3.2)
$$

From (2.7) and the expression of β of (2.2), we obtain

$$\frac{\alpha^n}{\beta^m} = \frac{\alpha^{n+m} S^m}{(1-\alpha)^{2m}} = \frac{n^2 R_D C_L (1-\alpha)^2}{r_0 c_0 \alpha L^2} \qquad (3.3)$$

Substitute (3.3) into (3.2),

$$P_{switch} = k_1 (\frac{\alpha^{s_1}}{\beta} + \frac{\alpha^{s_2}}{\beta^2} + \cdots + \frac{\alpha^{s_m}}{\beta^m}) + k_2, \qquad (3.4)$$

where

$$
\begin{aligned}
k_1 &= \frac{V_{DD}^2 f \delta r_0 c_0 \alpha L^2 (1-\beta)}{n^2 R_D (1-\alpha)^2} + \frac{V_{DD}^2 f \delta r_e (c_g + c_d)}{R_D}, \\
k_2 &= \frac{V_{DD}^2 f \delta r_0 c_0 \alpha L^2}{n^2 R_D (1-\alpha)^2}.
\end{aligned}
\qquad (3.5)
$$

3.1.2. Leakage Power

Assume that $I_{off_n} = I_{off_p}$ and $W_{p_{min}} = 2 W_{n_{min}}$ as in [4]. The leakage power is given by,

$$
\begin{aligned}
P_{leakage} &= \frac{3}{2} V_{DD} I_{off_n} W_{n_{min}} (b_1 + b_2 + \cdots + b_m) \\
&= \frac{3 V_{DD} I_{off_n} W_{n_{min}} r_e}{2 R_D} (\frac{\alpha^{s_1}}{\beta} + \frac{\alpha^{s_2}}{\beta^2} + \cdots + \frac{\alpha^{s_m}}{\beta^m}).
\end{aligned}
\qquad (3.6)
$$

3.1.3. Short-circuit Power

Under the same assumption as in [4] that the input waveform is a single time-constant exponential and $V_{t_n} = V_{t_p} = V_{DD}/4$, where V_{t_n} and V_{t_p} are the threshold voltages. The short-circuit power is given by,

$$
\begin{aligned}
P_{short\_circuit} = \quad & \delta V_{DD} W_{n_{min}} I_{short\_circuit} f ln3 \\
& (b_1 \tau_0 + \cdots + b_m \tau_{m-1}),
\end{aligned}
\qquad (3.7)
$$

where $\tau_i (0 \leq i \leq m-1)$ is the delay between the ith buffer and $(i+1)$th buffer (with τ_0 being the delay between the source and the first buffer). By Elmore delay [13] and Theorem 1 of [6],

$$
\begin{aligned}
\tau_0 &= A n_0 + B_0 \\
\tau_i &= A n_i + B_1, \quad 1 \leq i \leq m,
\end{aligned}
\qquad (3.8)
$$

where

$$A = \frac{r_0 c_0 L^2 (1+\alpha)}{2 n^2 (1-\alpha)}, \quad B_0 = \frac{\alpha r_0 c_0 L^2}{n^2 (1-\alpha)^2}, \quad B_1 = r_e c_d + B_0. \qquad (3.9)$$

Substitute $b_j(1 \leq j \leq m)$ of (2.2) and $\tau_i(0 \leq i \leq m - 1)$ of (3.8) into (3.7),

$$P_{short\_circuit} = \frac{r_e\delta V_{DD}W_{n_{min}}I_{short\_circuit}fln3}{R_D}[\frac{\alpha^{s1}}{\beta}(An_0 + B_0) + \frac{\alpha^{s2}}{\beta^2}(An_1 + B_1) + \cdots + \frac{\alpha^{sm}}{\beta^m}(An_{m-1} + B_1)]. \quad (3.10)$$

Combining (3.4), (3.6) and (3.10), we get,

$$P_{total} = k_3\frac{\alpha^{s1}}{\beta} + k_4(\frac{\alpha^{s2}}{\beta^2} + \cdots + \frac{\alpha^{sm}}{\beta^m}) + k_5(\frac{\alpha^{s1}}{\beta}n_0 + \cdots + \frac{\alpha^{sm}}{\beta^m}n_{m-1}) + k_2, \quad (3.11)$$

where

$$\begin{aligned} k_3 &= k_1 + \frac{3V_{DD}I_{off_n}W_{n_{min}}r_e}{2R_D} \\ &+ \frac{r_e\delta V_{DD}W_{n_{min}}I_{short\_circuit}fln3}{R_D}B_0, \\ k_4 &= k_1 + \frac{3V_{DD}I_{off_n}W_{n_{min}}r_e}{2R_D} \\ &+ \frac{r_e\delta V_{DD}W_{n_{min}}I_{short\_circuit}fln3}{R_D}B_1, \\ k_5 &= \frac{r_e\delta V_{DD}W_{n_{min}}I_{short\_circuit}fln3}{R_D}A. \end{aligned} \quad (3.12)$$

By setting $\frac{\partial P_{total}}{\partial n_i} = 0$ $(0 \leq i \leq m - 1)$, we have

$$n_{m-2} = \frac{1}{\beta ln\alpha}\alpha^{\frac{-k_4-k_3 ln\alpha}{k_4 ln\alpha}} - \frac{k_4 + k_3 ln\alpha}{k_4 ln\alpha}. \quad (3.13)$$

After some simplification from $\frac{\partial P_{total}}{\partial n_i} = 0$ $(0 \leq i \leq m - 1)$, the following recursive relationships are obtained,

$$\begin{aligned} n_0 &= \frac{1}{\beta ln\alpha}\alpha^{n_1} - \frac{k_5 + k_3 ln\alpha}{k_5 ln\alpha}, \\ n_i &= \frac{1}{\beta ln\alpha}\alpha^{n_{i+1}} - \frac{k_5 + k_4 ln\alpha}{k_5 ln\alpha}, \ 1 \leq i \leq m - 2, \\ n_{m-1} &= \frac{-k_5 - k_4 ln\alpha}{k_5 ln\alpha}. \end{aligned} \quad (3.14)$$

Note that (3.14) is the only critical point (at which all the partial derivatives are 0) of function P_{total} and it is a peak point. In the practice, k_5 is much smaller than k_4. As α and β are both between 0 and 1 [6], the values of expressions of $n_i(0 \leq i \leq m - 1)$ of (3.14) are negative. However n_i is the number of wire segments between two buffers, it should be nonnegative integers between 0 and n. This means the maximum and minimum of P_{total} can only be achieved at the boundary points. It is easily seen that if $k_5 << k_4$, all the partial derivatives of P_{total} are negative in the feasible region of $n_i(0 \leq i \leq n)$. Hence P_{total} decreases as any specific $n_i(0 \leq i \leq m - 1)$ increases. Let $p(n_0, n_1, \cdots, n_{m-1}) = P_{total}$. The following theorem is obtained,

Theorem 1. If $0 \leq n_i < \bar{n}_i \leq n$, and $n_j(0 \leq j \leq m - 1, j \neq i)$ is fixed, then

$$\begin{aligned} p(n_0, \cdots, n_i, \cdots, n_{m-1}) &> p(n_0, \cdots, \bar{n}_i, \cdots, n_{m-1}), \\ for \ 0 &\leq i \leq m - 1. \end{aligned} \quad (3.15)$$

The following theorem can be derived under the assumption that $k_4 >> k_5$.

Theorem 2

$$\begin{aligned} p(n_0, \cdots, n_i, \cdots, n_j, \cdots, n_{m-1}) &> \\ p(n_0, \cdots, n_i + 1, \cdots, n_j - 1, \cdots, n_{m-1}), \\ for \ 0 \leq i &\leq j \leq m - 1. \end{aligned} \quad (3.16)$$

Proof. From the expression of $p(n_0, \cdots, n_i, \cdots, n_j, \cdots, n_{m-1})$,

and noticing (2.3), we have

$$\begin{aligned} &p(n_0, \cdots, n_i, \cdots, n_j, \cdots, n_{m-1}) - \\ &\quad p(n_0, \cdots, n_i + 1, \cdots, n_j - 1, \cdots, n_{m-1}) \\ &= k_4(1 - \alpha)(\frac{\alpha^{s_{i+1}}}{\beta^{i+1}} + \frac{\alpha^{s_{i+2}}}{\beta^{i+2}} + \cdots + \frac{\alpha^{s_j}}{\beta^j}) \\ &+ k_5(1 - \alpha)(n_{i+1}\frac{\alpha^{s_{i+2}}}{\beta^{i+2}} + \cdots + n_{j-1}\frac{\alpha^{s_j}}{\beta^j}) + k_5\frac{\alpha^{s_{j+1}}}{\beta^{j+1}} \\ &+ [k_5 n_i(1 - \alpha) + k_4 - (k_4 + k_5)\alpha]\frac{\alpha^{s_{i+1}}}{\beta^{i+1}}. \end{aligned} \quad (3.17)$$

Since $0 < \alpha < 1$ and $k_4 >> k_5 > 0$, $k_5 n_i(1 - \alpha) + k_4 - (k_4 + k_5)\alpha \geq 0$, and all other terms in (3.17) are nonnegative. We have proved Theorem 2.

Combining Theorem 1 and Theorem 2, we have

Theorem 3. Given a simultaneous buffer insertion/sizing and wire sizing with m buffers (BISWS/m) problem, suppose its optimal delay is achieved, i.e. (2.2)-(2.5) are satisfied, the maximum and minimum power dissipation are at $(n_0, n_1, \cdots, n_{m-1}) = (0, 0, \cdots, n)$ and $(n_0, n_1, \cdots, n_{m-1}) = (n, 0, \cdots, 0)$, respectively, where n is the total number of wire segments.

Theorem 3 tells us that when all the buffers are taped just before the load the power dissipation is optimal with the optimum delay for BISWS/m. This is because of the special property of BISWS. The wire size and buffer size are simultaneously changed when the buffer position is changed. Our SPICE simulations in section 5 also confirm this conclusion.

Remark

We need to point out that Theorem 3 provides us the optimal solution from the theoretical aspect. In practice, there may have some constraints such as the lower bounds for wire width of each segment. But we always can find the optimal solution by Theorem 1 and 2.

3.2. POBISWSOD Problem

For a given BISWS problem, we first find its optimal solutions by (2.1)-(2.5). After the value of m is fixed, the POBISWSOD problem becomes POBISWSOD/m problem which can be solved by the method of last part.

4. OPTIMAL POWER DISSIPATION WITH DELAY PENALTY FOR BISWS

As we mentioned before, to achieve the optimum delay, a large number of buffers need to be inserted with the technology scaling. It is believed that the total power dissipation of the optimum buffer insertion scheme can be excessive [4]. It is very important to study the optimum power dissipation with delay penalty during the buffer insertion. [4] addressed this problem for a uniform long line. In the next we consider the problems of optimizing total power dissipation under given delay penalty for BISWS.

Power-optimal Simultaneous Buffer Insertion/Sizing and Wire Sizing with Delay Penalty problem (POBISWSDP): Given a BISWS problem, and a delay penalty $\rho(\rho > 1)$, the objective is to minimize the total power dissipation satisfying that its delay is ρD_{opt}, where D_{opt} is the BISWS optimum delay given by (2.5).

To solve POBISWSDP, we first solve the BISWS problem to find out the optimum delay D_{opt} of (2.5), then

$$D = \rho D_{opt}. \quad (4.1)$$

From (2.4), we get

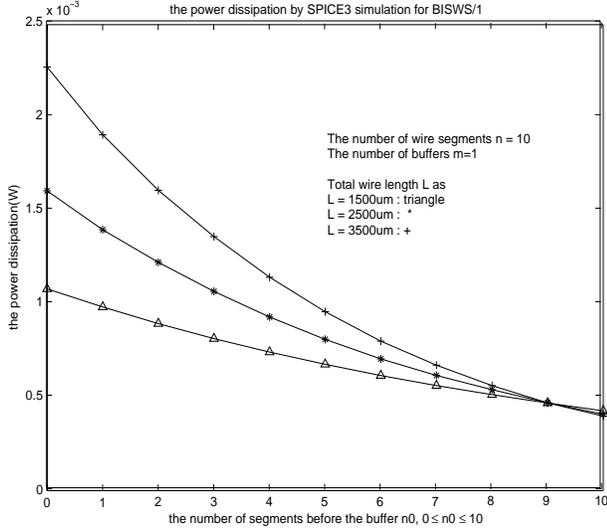$$\frac{r_e c_g}{R_D C_L}\alpha^n = \beta^{(m+1)}. \quad (4.2)$$

the power dissipation by SPICE3 simulation for BISWS/1

The number of wire segments n = 10
The number of buffers m=1

Total wire length L as
L = 1500um : triangle
L = 2500um : *
L = 3500um : +

the power dissipation by SPICE3 simulation for BISWS/2

The wire length L = 2500um
The number of wire segments n = 10
The number of buffers m = 2

n0=0
n0=1
n0=2
n0=3

Figure 3: Power dissipation for different wire length with optimal delay simulated by SPICE3 with $0.18\mu m$ technology

Figure 4: Power dissipation for BISWS with optimal delay simulated by SPICE3 with $0.18\mu m$ technology. The minimum power is at $(n_0, n_1, n_2) = (10, 0, 0)$ labeled with '*'

Hence

$$m = \frac{1}{ln\beta}(ln\frac{r_e c_g}{R_D C_L} + nln\alpha) - 1. \qquad (4.3)$$

Substituting m of (4.3) into (2.5), after simplification we have

$$(rec_d + \frac{2\alpha}{(1-\alpha)^2})\frac{ln(r_e c_g)-ln(R_D C_L)}{2ln(1-\alpha)-ln(S\alpha)}$$
$$+ \frac{r_0 c_0 L^2}{2n^2}\frac{n(1-\alpha^2)+2\alpha}{(1-\alpha)^2} - \frac{2\alpha}{(1-\alpha)^2} = D + r_e c_d, \qquad (4.4)$$

where S is given in (2.2). We can obtain α by numerically solving equation (4.4) using Newton-Raphson iterative method. Then substitute the value of α into (4.3), the value of m is obtained.

Once m and α are fixed, the POBISWSDP problem becomes POBISWSOD/m which can be solved by using the method of last section.

Similarly, we can solve the problem of Power-optimal Simultaneous Buffer Insertion/Sizing and Wire Sizing with m buffers with Delay Penalty problem (POBISWSDP/m).

5. EXPERIMENTAL RESULTS

In order to verify our theoretical results, SPICE simulation is carried out in this section. We use SPICE3 with the $0.18\mu m$ technology for all the simulations. The value of the circuit parameters is from [4], which is based on ITRS [21] and FASTCAP [20] as shown at Table 1. The source driver and load we used are 100X of minimum device in the following simulations.

5.1. Simulation of POBISWSOD(POBISWSOD/m) problems

For the first simulation, we take $m = 1$, $n = 10$, and the total wire length $L = 1500\mu m$, $2500\mu m$, and $3500\mu m$, respectively. The simulation result for power dissipation is shown in Figure 3, from which, we can see that the minimum power dissipation is achieved at the point $(n_0, n_1) = (10, 0)$, and the maximum achieved at the point $(n_0, n_1) = (0, 10)$. The maximum power dissipation can be 6 times of the minimum, and there is no much difference for the minimum power dissipation for different wire lengths while the
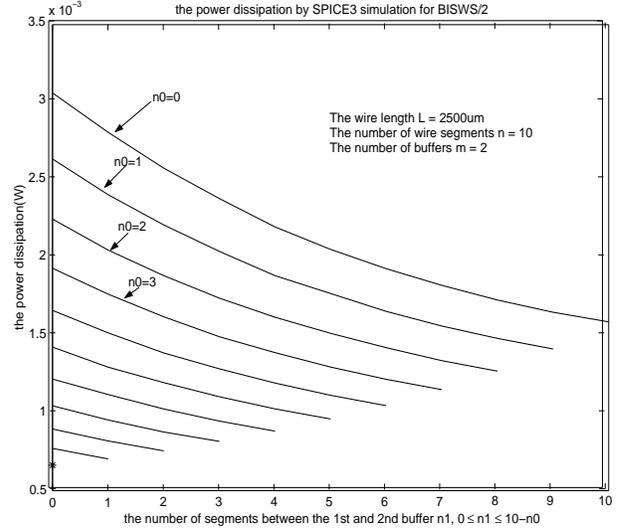
Table 2: Power Dissipation for a wire with length $15000\mu m$, 10 segments

m	delay (ns)	max power (mW)	min power (mW)
1	0.817	20.701	1.712
2	0.767	65.248	2.421

maximum power dissipation changes significantly. This indicates optimizing the power dissipation for BISWS is very necessary.

The second simulation is for a wire with length $L = 2500\mu m$, 10 segments and 2 buffers. When the number of wire segments between the source and the first buffer $n_0 = 0, 1, \cdots, 10$, the power dissipation curves over the number of wire segments between the first buffer and the second buffer n_1 are shown in Figure 4. This also verified our results of Theorem 1 and Theorem 2.

5.2. Simulation of POBISWSDP

We simulate a wire with length $15000\mu m$, 10 segments. The number of buffers is $m = 2$ when the optimal delay is achieved. If the delay penalty is $\rho = 1.06$, $m = 1$ is the optimal solution by solving the POBISWSDP problem of section 4 and the minimum power dissipation can be saved as much as 25%. The result is shown at table 2.

5.3. Comparison with uniform buffer insertion

In order to show the advantages of the simultaneous buffer insertion/sizing and wire sizing, we compare it with the traditional uniform buffer insertion (UBI) in which all the wire segments are with the same width. We simulate a wire with one buffer, ten segments for BISWS. For uniform buffer insertion the wire width is set to be the average width of all the segments in BISWS. The same buffer size is used for both UBI and BISWS. Table 3 shows the simulation results for wire length $L = 1000\mu m, 2500\mu m, 5000\mu m$.

Table 1: Parameters for 0.18μ m technology from [4] which is based on ITRS ([21]) and FASTCAP([20])

$r_0(\Omega/\square)$	$c_0(\mu F/m^2)$	$r_e(k\Omega)$	c_g(fF)	c_d(fF)	V_{DD} (V)	$I_{off_n}(\mu A/\mu m)$	f(GHz)	$W_{min}(\mu m)$
0.0419	232.9	8	1.9	4.8	1.8	0.2	1.2	0.18

Table 3: SPICE3 simulation for the comparison between the traditional uniform buffer insertion and BISWS for a wire with length L=$1000\mu m$, $2500\mu m$ and $5000\mu m$ and the number of segments is 10 for BISWS.

wire length(μm)	type	buffer size (X of min device)	delay (ns)	power (mW)
1000	UBI	71.30	0.0977	0.540
	BISWS	71.30	0.0954	0.439
2500	UBI	49.47	0.1568	0.621
	BISWS	49.47	0.1432	0.409
5000	UBI	32.18	0.3160	0.986
	BISWS	32.18	0.2409	0.598

From table 3, we can see the BISWS is better than UBI in terms of delay and power dissipation.

6. CONCLUSION

We have analyzed the optimal power dissipation problems for simultaneous buffer insertion/sizing and wire sizing with delay constraints. The closed form solutions to minimize total power dissipation with optimal delay or with delay penalty are derived for BISWS. These closed form solutions can be used to efficiently estimate the power dissipation in the early stages of the VLSI designs. We observe that the power dissipation can be much different even with the same optimal delay. SPICE simulations verify our theoretical results. The simulation results also show that the simultaneous buffer insertion/sizing and wiring sizing is better than traditional uniformed buffer insertion in terms of optimal delay and optimal power dissipation.

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