Systematic Design for Power Minimization of Pipelined Analog-to-Digital Converters

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ABSTRACT
In this paper a general method to design a pipelined ADC with minimum power consumption is presented. By expressing the total power consumption and the total input-referred noise of the converter as functions of the capacitor values and the resolutions of the converter stages, an optimization algorithm is employed to calculate the optimum values of these parameters, which lead to minimum power consumption while a specific noise requirement is satisfied. To determine the bias current values of operational amplifiers an optimal choice for settling and slewing time parameters is proposed. A practical design example is presented to show the effectiveness of the proposed methodology.

1. INTRODUCTION
Pipelining is one of the best approaches for low-power implementation of high-speed high-resolution analog-to-digital converters. Design approaches to reduce the power consumption of pipelined ADCs are therefore of great importance to realize medium-to-high-resolution high-speed A/D converters with the least possible power consumption. It has been illustrated that employing optimum non-identical values for the capacitors and the resolutions of the stages effectively reduces the power consumption [1-5]. In [1] it has been concluded that to minimize the power consumption of a pipelined ADC, the resolution of all the stages can be chosen equal to 1.5 just in converters with resolutions of less than 10 bits. In [2] a systematic design methodology has been presented where resolutions higher than 1.5 has been proposed for the front-end stages of the high-resolution converters but the capacitor values of the stages are not optimized and a predefined noise distribution is assumed. In [3] the effects of the capacitor scaling, parallelism, and non-identical resolutions per stages on the pipelined ADC power consumption are investigated separately. In the latest reported automatic design tool for pipelined ADCs [4] the converter is optimized to minimize the power consumption and area using geometric programming. However, the latter algorithm is applied to a converter with identical resolution per stages. To our knowledge, it appears that neither of the proposed approaches is as general yet simple and effective as the approach employed in our work [5].

In this paper with no specific constraint, arbitrary capacitor scaling as well as non-identical resolution per each stage is utilized in the design of the converter. First, a closed-form equation for the bias current value of a single-pole operational transconductance amplifier (OTA) is derived employing an innovative dynamic allocation of the small- and large-signal settling time parameters. Then the total static power dissipation and also the total input-referred noise of the pipelined ADC are calculated. A design methodology is presented to minimize the power consumption with a defined noise budget. The input parameters of the optimization CAD tool and related considerations as well as the advantages of this methodology are addressed. Finally a design example illustrating the effectiveness of the proposed methodology is presented.

2. MINIMUM-CURRENT OTA DESIGN
In a switched-capacitor circuit, the outputs of the operational transconductance amplifiers have to settle to within a very small fraction of their final values (e_{ss}), depending on the required accuracy of the OTA, in a definite interval called the settling time. The total settling time including the small-signal (t_{ss}) and the large-signal (t_{ls}) settling times should be less than half of the clock period, i.e.

$$t_S = t_{ss} + t_{ls} = T_{clk}/2 - t_{other} \quad (1)$$

where t_{other} is the rest of the half-period for non-overlapping of two clock pulses. While t_{ls} is due to the limited slew rate, t_{ss} depends on the finite bandwidth of the OTA.

For a single-pole or a two-pole op-amp where the second pole is sufficiently larger than the unity-gain bandwidth, the small- and large-signal settling times are related to the op-amp characteristics as

$$t_{ls} = \frac{V_{FS}}{SR} \quad \text{and} \quad t_{ss} = n.\tau = n.\frac{1}{2\pi f_{-3dB}} = n.\frac{1}{2\pi.\beta.f_u} \quad (2,3)$$

where V_{FS} is the full-scale signal range, f_{-3dB} the -3-dB bandwidth, β the feedback factor, f_u the unity-gain bandwidth of the OTA and n the number of the time constants to be spent to achieve a desired accuracy, equal to $ln(1/e_{ss})$. For a single-stage fully-differential telescopic- or folded-cascode op-amp the required value for the current of the input devices can be expressed by [6]:

$$I_i = \frac{V_{FS}.C_{load}}{t_{ls}} \quad \text{and} \quad I_i = n.\frac{V_{eff,i}.C_{load}}{2\beta.t_{ss}} \quad (4,5)$$

where SR is the op-amp slew rate, I_i is the current of the input transistors, and C_{load} is the load capacitor at each output node. With the equation expressed above, V_{FS} is the single-ended voltage swing, half of the differential full-scale voltage. V_{effi} is chosen as the smallest effective voltage that keeps the input transistors in the strong inversion region and satisfies the other op-amp specifications such as gain. If t_{ss} and t_{ls} are predefined statically, e.g. one third of the total settling time is reserved for slewing[7], then I_i should be chosen as the maximum value of the above two, probably leading to some power being wasted. However, if the two settling contributions are determined dynamically such that the two above terms for the current are equal, some power can be saved. This will lead to the optimum value for the total bias current of the OTA to be calculated from

$$I_{OTA,opt} \propto 2I_{i,opt} = 2\frac{V_{FS}.C_{load}}{t_S}.\left(1+\frac{\ln(e_{ss}^{-1}).V_{eff,i}}{2\beta.V_{FS}}\right) \quad (6)$$

where $t_{ls}+t_{ss}=t_S$ (the total settling time). This equation shows the dependency of the optimized current of a single-pole OTA on the load capacitor, the settling time and accuracy, the full-scale voltage

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and the feedback factor of the operational amplifier. It has been realistically assumed that the current value of all the non-input branches including the bias circuit or the gain-boosting amplifiers [8] or the folded branch in a folded-cascode structure is proportional to the bias current of the input devices. A proportional closed-form formula can also be extracted if two-stage Miller-compensated OTAs are used assuming that the compensation capacitors are chosen equal to the load capacitors and the current values in the second stages of the amplifier are proportional to the currents of the input stages. Such an assumption will be true when either the second stage currents are high enough to satisfy the slewing requirements of the output nodes, or class-A/AB amplifiers are used as the output stages [9]. The current values obtained with this relation are always smaller than what obtained by the conventional methods.

3. TOTAL CURRENT AND NOISE POWER

For a high-resolution converter, where the capacitor values are determined by the required signal-to-noise ratio (SNR), if the total current consumption as well as the total input-referred noise of the converter is expressed versus the resolutions and the capacitor values of the stages, one can simply determine the optimum values of those parameters in order to minimize the current consumption while a specified noise constraint is met. This is what performed in our systematic design methodology. In order to express the total current of the ADC OTAs versus the ADC parameters, the load capacitor seen by each OTA should be calculated. Fig. 1 shows one possible implementation of an *m*-effective-bit residue amplifier in a pipelined ADC. For the OTA used in the residue stage of Fig. 1, the total capacitive load in the amplifying phase can be obtained from [5]

$$C_{load_j} = C_{F_j}\left(2^{m_{j+1}}s_j + \left(\frac{2^{m_j}+\gamma_j-1}{2^{m_j}+\gamma_j}\right)\right) + C_{out_j} + (2^{1+m_{j+1}}-2)C_{cu} \quad (7)$$

where C_F is the feedback capacitor, C_{out} is the output parasitic capacitance of the OTA, and C_{cu} is the input capacitance of a single comparator. In this equation, m_j, s_j and γ_j represent the effective resolution, the scaling factor (i.e. C_{Fj+1}/C_{Fj}) and the ratio of C_{op} to C_F (where C_{op} is the input parasitic capacitance of the OTA) of the *j*th stage, respectively. It has been assumed that one redundant bit has been employed in each stage. We have modeled the additional effect of C_{out} as an excess factor of ε. In this switched-capacitor amplifier, the feedback factor of the OTA in the amplification phase can be written as

$$\beta = \frac{C_F}{C_S + C_F + C_{op}} = \frac{1}{2^m + \gamma} \quad (8)$$

Therefore the total current consumption of the amplifiers and the comparators of the *n*-stage pipelined converter, using (6) for single-stage amplifiers can be obtained from [5]

$$I_{total} = \sum_{j=1}^{n}(2^{1+m_j}-2).I_{cu} + K.\frac{2V_{FS}}{t_S}\sum_{j=1}^{n-n^*}\left\{1 - \frac{\ln(e_{ss_j}).V_{eff}(2^{m_j}+\gamma_j)}{2V_{FS}}\right.$$
$$\left.\cdot\left[C_{F_j}\left(2^{m_{j+1}}s_j + \left(\frac{2^{m_j}+\gamma_j-1}{2^{m_j}+\gamma_j}\right)\right)(1+\varepsilon_j) + (2^{1+m_{j+1}}-2)C_{cu}\right]\right\}$$
$$+ n^* I_{OTA^*} \quad (9)$$

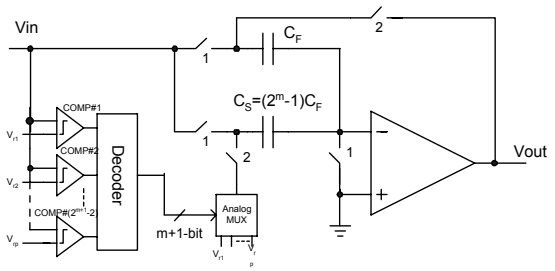


Figure 1. The schematic of the residue stage

where n^* is the number of similar back-end stages in which the capacitor scaling has been stopped, reminding the fact that the scaling stops as soon as the capacitors are determined by the minimum required capacitor matching or when the output capacitance of the amplifiers is dominant [4]. $I_{OTA}{}^*$ is the current consumption of the back-end OTAs. In this equation, *K* is the modification factor added to include the excess current consumption of the bias circuits, the common-mode feedback circuits and other branches of the OTAs with proportional current values. In the above equation it has been assumed that the comparators used in different stages are all similar. The problem can be easily generalized to a case where different comparators are used for different stages. Another important consideration is the sample-and-hold (S/H) stage. The current consumption of this stage can be calculated in a similar fashion with a resolution of *m* equal to zero. Just the feedback factor of the OTA in the S/H amplifier should be corrected due to the architecture utilized. For a flip-around architecture, for instance, the feedback factor is obtained from (8) with m=0 (which would have a value less than unity).

In order to calculate the input-referred noise of the converter, the input-referred noise power of each stage is primarily calculated and then referred to the input of the ADC. The input-referred thermal noise of a switched-capacitor amplifier has two main sources, the on-resistance of the switches and the operational amplifiers. It has been shown that the total input-referred noise power of the *n*-stage pipelined ADC is obtained from [5]

$$\overline{v}_{ni,t}^2 = kT\sum_{j=1}^{n}\frac{\left(\frac{4}{3}\frac{F}{C_{load,j}} + \frac{2}{C_{F,j}}\right)\left(2^{-m,j} + \gamma_j 2^{-2m,j}\right)}{2^{2\sum_{i=1}^{j-1}m_i}} \quad (10)$$

In our CAD tool, making use of the relation derived for the load capacitor of the *j*th stage, the above equation is simply expressed versus the capacitors and the resolutions of stages when the OTA configuration and therefore an estimation for the OTA excess noise factor, *F*, is known.

4. DESIGN METHODOLOGY

Using MATLAB, a simple optimization tool has been developed that employs the proposed closed-form formulas of total current and input-referred noise of the ADC. The optimization problem is defined as follows.

Find the optimum values of the capacitors and the resolutions of different stages, in order to minimize the total power consumption of the ADC, while the total input-referred noise requirement is satisfied.

The main parameters of the sub-blocks of the converter including the capacitor values and the resolutions of different stages are *simultaneously* optimized while no limiting assumption is imposed.

The employed optimization algorithm is a simple search engine, which can be replaced by more complex optimization procedures such as genetic algorithm. The optimization tool is very fast and accurate since the employed equations include all the non-ideal effects. For the rms value of the required input-referred thermal noise voltage one choice, employed here, is half of the quantization noise voltage calculated from

$$\sqrt{\overline{v}_{ni_q}^2} = \frac{V_{LSB}}{\sqrt{12}} = \frac{2V_{ref}}{2^N\sqrt{12}} \qquad (11)$$

This choice will lead to 1dB degradation in the value of SNR of the ideal ADC. Note that the signal-to-noise ratio is obtained from

$$SNR = 10\log_{10}\left(\frac{V_{ref}^2/2}{\overline{v}_{ni_q}^2 + \overline{v}_{ni_{th}}^2}\right) \qquad (12)$$

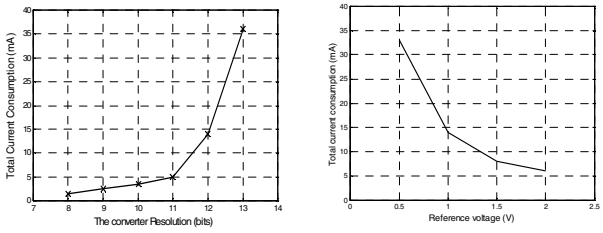
where V_{ref}, the reference voltage, is equal to the single-ended full-scale voltage swing. By using bit redundancy the maximum comparator offset in an *m*-effective bit stage is permitted to be less than $V_{ref}/2^{m+1}$. Since the comparator offset must always meet the above relation, after choosing a specific architecture for the comparators, depending on the maximum offset voltage, the maximum allowed resolution of the residue stages is determined.

The input parameters for the CAD tool are addressed in section (5) with a design example. The optimization tool determines the optimum values for all capacitors, C_F's, and the stage resolutions and also the optimum values for the bias currents of the stages. The input transistors are then optimally sized using the optimum values for the currents and the overdrive voltages (V_{eff}). It should be mentioned that some of the input parameters such as the parameters of the comparators and if permitted the reference voltage can be even optimally chosen using the methodology presented here. Since the values of γ, ε and F were just the initial estimations, a few iterations accompanied with circuit simulations are required to modify the optimized values of the parameters. Design examples have confirmed the effectiveness of this methodology in low-power design of pipelined ADCs [5]. A practical design example will be presented in the following section as well.

For ADCs with resolutions of not larger than 10, the optimization CAD tool suggests a resolution of 1 effective bit (i.e. 1.5 bits) for all stages. This is exactly the same as what proposed by Lewis [1] nevertheless the capacitor values are optimized here.

The developed tool can be used not only to optimize an ADC but also to calculate the power consumption of arbitrary design cases with specific values for the resolutions, the capacitor values, the full-scale voltages, the comparator power dissipations or the OTA noise excess factors. For example, the designer can easily decide to choose between the maximum allowed number of bits of 5 with power hungry low-offset comparators and the maximum bits of 2 or 3 with low-power dynamic comparators.

Using the developed CAD tool the dependency of the total current consumption of the ADC on the overall resolution and also the full-scale voltage swing can be conveniently investigated. Fig. 2-a shows the current consumption of a 50MSamples/s converter versus its resolution. It can be observed that by adding one bit to the overall resolution, the current consumption is increased with a higher rate in higher resolutions. This is mainly due to the fact that in low resolutions the capacitor values are mainly determined by the required matching rather than the *kT*/*C* noise. However at higher resolutions the thermal noise determines the capacitor values. When the resolution is increased by a single bit, the magnitude of the LSB voltage is halved and the thermal noise



(a) (b)

Figure 2. The optimized current consumption of the 50MS/s converter versus (a) its resolution for a full-scale voltage swing of 1V, (b) its full-scale voltage swing for a resolution of 12 bits.

power should become one fourth to save the SNR value. Thus the capacitor values are to become four times larger.

The dependency of the power dissipation on the full-scale voltage can be also investigated as shown in Fig. 2-b for a 12-bit 50MS/s example. It can be seen that if the full-scale voltage is halved, the current consumption is increased by a factor more than two. This behavior can be clearly predicted from the optimized value for the current consumption given by (6) keeping in mind the dependency of C_{load} on the full-scale voltage similar to what discussed for resolution. Therefore the *power* consumption of the ADC increases by scaling down the voltage. It should be finally mentioned that if the non-dominant poles of the employed OTAs are not high enough to be neglected in the frequency response, it can be shown that the proposed formulas have just *overestimated* the parameters of small-signal settling time and the contribution of the OTAs in the total input-referred thermal noise and the methodology is still true [5].

5. DESIGN EXAMPLE

In order to illustrate the effectiveness of the proposed design methodology, a 3.3-V 12-bit 40MS/s ADC is presented here as a design example. The input parameters of the developed tool including N (the resolution of the converter equal to 12 in this design), V_{ref} (equal to 1V here), C_{min} (the minimum required value to satisfy a specified matching behavior dependent on the fabrication process, equal to 100fF in our design), C_{cu} and I_{cu} (the input capacitance and the current dissipation of a single comparator equal to 30fF and 100μA respectively with our comparators), m_{max} (the maximum permitted value for the resolution of a residue stage determined due to the maximum offset of the comparator, equal to 3 here), γ (the vector of γ_i's initially equal to [0.5 …0.5]), ε(the vector of ε_i's initially assumed equal to[0.8 0.6 0.5 … 0.5]), F (the excess noise factor dependent on the OTA architecture, equal to 2 for the telescopic-cascode structure of our design), and V_{eff} (the minimum value for the overdrive voltage of the input devices, equal to 150mV here) are initially determined for the optimization CAD tool. The optimization tool has determined the optimum values for the capacitors, C_F's, and the stage resolutions and also the optimum values for the currents of the stages as listed in Table.1. The input transistors are then optimally sized using the optimum values for the currents and the overdrive voltages (V_{eff}). One redundant bit is employed in all stages in order to be able to use low-power dynamic comparators with large offset voltages.

Table 1. Optimized specifications of the residue stages

Stage #	$m_{effective}$	C_F	Stage Current
1st Stage	3	0.45pF	7mA
2nd Stage	2	0.25pF	2.5mA
3rd-7th Stage	1	0.1pF	1.5mA

The third stage and the following stages are all realized using well-known 1.5-bit residue amplifiers. The back-end ADC is only a 2-bit flash converter. The final 12 bits are extracted form 19 output bits employing a digital error correction circuit.

A dedicated sample-and-hold amplifier (SHA) at the front-end of the converter consumes a considerable amount of the total power of the converter since its noise power is referred to the input with no attenuation and therefore large capacitors (calculated equal to 9.6pF in our design by the CAD tool) are required to satisfy the *kT/C* noise constraint. In order to be able to eliminate this power-hungry SHA it should be insured that the input signal would vary less than $V_{ref}/8$ (the maximum interval between comparators' decision levels of the front-end 3-bit stage) in the time interval between the sampling instance of the first residue stage and the comparison time of the comparators. For a sampling rate of 40MS/s and a Nyquist-frequency input the maximum acceptable time difference is about 1.5ns, which can be conveniently satisfied with careful layout design.

The utilized OTA structure employed in all stages (of course with optimized values of bias currents and device sizes) including the bias and the common-mode feedback circuits is shown in Fig. 3.

The ADC is simulated with HSpice using BSIM3v3.1 model parameters of a 0.25-µm 2P3M CMOS process in all process and temperature corners (from -40°C to +85°C). Full-scale DC test of the ADC confirms its 12-bit resolution. Fig. 4-a shows the simulated worst-case total (including the static and dynamic) current consumption of the ADC excluding the current of the reference buffers and clock drivers when a full-scale DC signal is applied as the input. It shows that the worst-case average power consumption of the ADC is 56mW. Fig. 4-b shows the dynamic performance of the converter where a full-scale input Nyquist-frequency sinewave is sampled with frequency f_s=40MHz. The signal-to-noise-and-distortion ratio including the thermal noise of the circuit is 69dB. The value of the spurious-free dynamic rang (SFDR) is 75dB as well. The power consumption of this ADC shows more than 2X reduction in power consumption compared to recently-reported 12-bit ADCs [10-13].

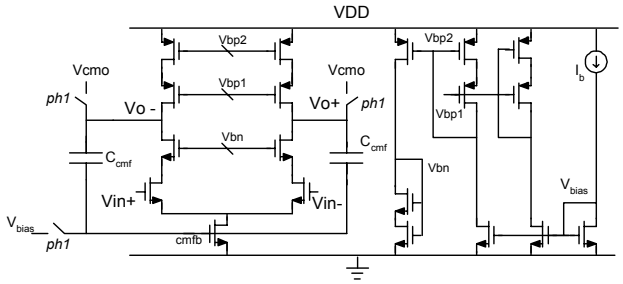
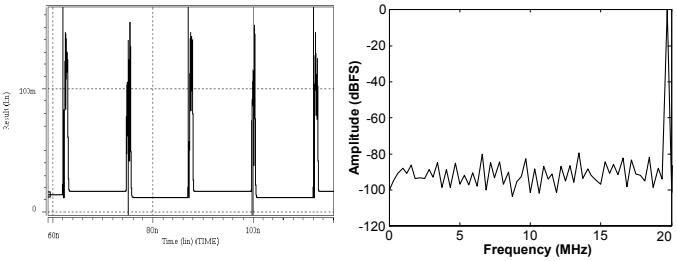


Figure 3. Structure of the OTAs including the bias and CMFB circuits

6. CONCLUSIONS

In this paper a novel systematic design methodology has been presented, which suggests the optimum values for the resolutions and the capacitors of all the stages in a switched-capacitor pipelined ADC. In this methodology, a low-power design technique for single-stage OTAs has been utilized which optimizes the values of the small- and large-signal settling times. The values of the capacitors and the resolutions of the stages are optimally determined in order to minimize the total current consumption of the converter (expressed in a closed-form equation here) while the required noise constraint (expressed in a closed-form equation as well) is satisfied.



(a) (b)

Figure 4. (a) Simulated worst-case current consumption of the entire ADC with a full-scale input (b) An FFT plot of the output for f_s=40MHz and a Nyquist-frequency input.

The dependency of the optimized power consumption on the resolution and reference voltage of the ADC was investigated as well. Finally simulation results of a practical 3.3-V 12-bit 40MS/s 56-mW ADC were presented to confirm the effectiveness of the proposed methodology in reducing the power consumption.

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