Weibull Based Analytical Waveform Model

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ABSTRACT
Current CMOS technologies are characterized by interconnect lines with increased relative resistance w.r.t. driver output resistance. Designs generate signal waveshapes that are very difficult to model using a single parameter model such as the transition time. In this paper, we present a simple and robust two-parameter analytical expression for waveform modeling based on the Weibull cumulative distribution function. The Weibull model accurately captures the variety of waveshapes without introducing significant runtime overhead and produces results with less than 5% error. We also present a fast and simple algorithm to convert waveforms obtained by circuit simulation to the Weibull model. A methodology for characterizing gates for the new model is also presented. Simulation results for many single and multiple input gates show errors well below 5%. Our model can be used in a mixed environment where some signals may still be characterized by a single parameter.

1. INTRODUCTION
As deep sub-micron technology moves towards decreasing feature sizes, the impedance of the interconnect lines does not scale down by the same factor as the gate impedance [1]. As a result, the wave shapes of the signals normally propagated through a digital circuit are increasingly more complex. In this context, waveshape complexity is a subjective measure of how far from a classical saturated ramp the shape is.

While the signal shapes are not directly interesting from a verification perspective, they greatly influence at least two quantities important for design performance: gate delay and cross-coupling noise amplitude. The most widely used analysis tool to predict timing performance is the static timing analyzer [2]. Current methodologies for static timing analysis map the signal shapes that are propagated through a digital circuit to a single parameter. The parameter used is usually the transition time obtained from the time difference between two points on the waveform (for example, the 20% and 80% points).

This approach is used almost invariably in gate-level static timing analyzers where the gates are pre-characterized as a function of input transition time and output load. The implicit assumption is that all wave shapes reaching the input of a gate resemble the shapes used in gate characterization and can be accurately described by a single parameter. The gate delay model is used during static timing analysis to compute timing windows and path delays for the entire circuit.

The most commonly used one-parameter waveform model in literature is the saturated ramp; industrial applications use many variations of this model to enhance its accuracy. Generally, these variations try to smooth out the corners of the saturated ramp. However, none of the variations we are aware of can go significantly beyond the limitations of a one-parameter model. We will compare our results against both the saturated ramp model and one of the more obvious variations.

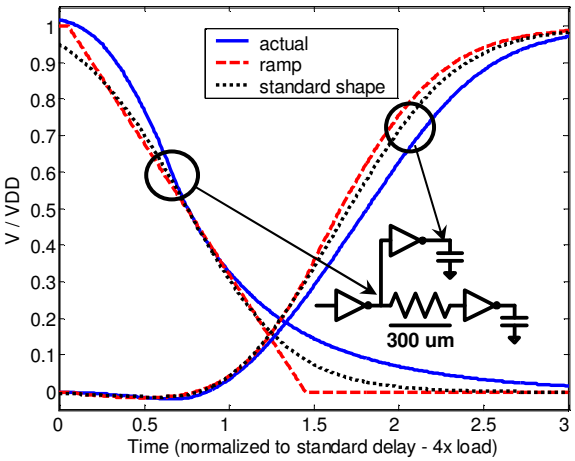

Figure 1 *RC* dominated waveform and its approximations

Figure 1 shows a sample waveform obtained through simulation of extracted post-layout netlist taken from the input of an inverter in an industrial 90nm technology. Its saturated ramp approximation is obtained by measuring the 20% to 80% time difference, extending it to a full saturated ramp and shifting the waveform to match the 50% point of the original. To obtain the standard shape approximation which is typically used during gate characterization, a saturated ramp with an average transition time was applied to a standard inverter. The capacitive load of the inverter was varied to obtain the desired 20% to 80% transition time at the output. The waveform at the output was shifted to match 50% point of the original waveform and was used as the standard shape approximation of the original waveform with same transition time.

Both the original waveform and its approximations were applied to the same inverter and the differences in outputs were measured. The delay and transition time errors produced by approximating the inverter input using a ramp were 14% and 19%, respectively, and those produced by approximating the inverter input using a standard shape were 9% and 11%, respectively. Moreover, the ramp model is not robust in the sense that its accuracy will depend highly on the threshold voltage of the receiver.

As shown by Figure 1, there are cases when a single parameter waveshape model cannot cover the variety of waveshapes seen in typical integrated circuits. Typically, using more parameters in the model increases accuracy in approximating the original signal. However, this increase in accuracy also comes with an increase in

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complexity of modeling and gate characterization, which depends exponentially on the number of parameters.

An accurate four parameter model for signal waveforms has been presented in [3] but it increases pre-characterization complexity by requiring a 4-dimensional table to store input information for gate instead of the one-dimensional table required for a ramp approximation. A 2-ramp model has been presented in [4] and it provides good accuracy for most of the signals. However, the model is hard to use because of its piecewise description and there is no clear deterministic method to determine when the model is applicable. More recently, [5] introduced a method to compute parameters for a waveform model based on a ramp followed by exponential for estimating delay variation due to crosstalk. However, the region where the ramp meets exponential can be very sensitive and can cause significant errors if the ramp and exponential do not fit naturally.

Thus, it is necessary to analyze the tradeoffs between various models for signal waveshapes and determine the requirements that an ideal model should satisfy. In our opinion, a good model should meet the following criteria:

- adequate coverage for waveshapes typically seen in circuits
- concurrent usage of both "old" and "new" model
- intuitive parameters
- simple gate characterization
- minimal storage space for gate characterization

We observed that the cumulative distribution functions (CDFs) of some statistical distributions could cover a variety of waveshapes using just two parameters [6]. Noting this appealing resemblance, we focused on modeling signal waveshapes analytically by using CDFs of probability distribution functions.

In this paper, we propose an analytical waveform model based on the CDF of the Weibull distribution function [6] and compare it with a ramp approximation of waveforms. We show that our model captures a variety of shapes with the introduction of just one parameter other than the transition time. The solution proposed here is easy to use in time domain and in frequency domain, thus making it convenient for circuit analysis. Moreover, results show that this smooth model introduces less noise in the circuit compared to a ramp approximation of the original signal, thus making timing analysis more accurate.

The Weibull distribution has been previously used to predict interconnect delay, [7]. The method used was moment matching for mean and standard deviation. With the mean and standard deviation roughly approximating the delay and transition time, respectively, [7] provides a good flow for linear circuit delay computation. Unfortunately, the wave shape proves to be quite independent from the delay especially when nonlinear gates are present. For example, changing the time reference for the signal to be matched will dramatically influence the shape of the resulting model given by [7] although the delay will continue to be very well approximated. Further details for this problem are given in section 3.2. Our conclusion is that none of the results from [7] can be used for waveform modeling, and a dedicated model focused on wave shape is required.

The rest of the paper is organized as follows. Theoretical background and the new model are presented in section 2. We present the fitting algorithm to obtain model parameters from original waveforms in section 3. A methodology for characterizing the gates with respect to three parameters (two describing the input waveform and one the output load) is given in section 4. Results for one-parameter modeling and the new two-parameter model are presented in section 5. The paper is concluded in section 6.

2. TWO-PARAMETER MODEL

This section presents a justification for the choice of two parameters for waveform modeling. Then we present two two-parameter probability distributions that can be used to approximate waveforms.

2.1 Moving from one parameter to two

We can define a waveform model as a time domain parameterized function

$$y = f(time, a_1, a_2 \ldots a_n) \tag{1}$$

Equation (1) defines a family of time domain signals, each member of this family being identified by its set of values ($a_1 \ldots a_n$). The parameters ($a_1 \ldots a_n$) can be thought of as *natural* if they show up in the minimal or canonical or most recognizable form of the function (1). For example, a and b are natural parameters for

$$y = a \cdot e^{-b \cdot t} \tag{2}$$

In the case of the saturated ramp model, there is a single parameter, t_{in}, and the function is shown in equation (3):

$$y(t, t_{in}) = \begin{cases} 0 & t < 0 \\ \dfrac{t}{t_{in}} & 0 \le t < t_{in} \\ 1 & t \ge t_{in} \end{cases} \tag{3}$$

The family of time domain signals (each distinguished by a specific t_{in}) is shown in Figure 2.

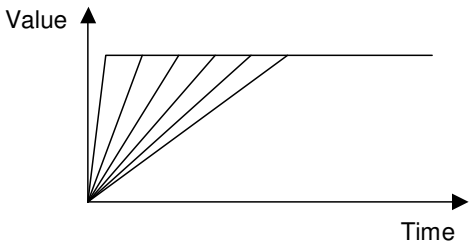

Figure 2 Saturated ramp family of curves

The current gate delay model [9] depends on two parameters, input transition time (the model for the waveform) and capacitive load (the model for the load):

$$\begin{aligned} delay &= f(t_{in}, C_L) \\ t_{out} &= g(t_{in}, C_L) \end{aligned} \tag{4}$$

To avoid increased complexity for the gate delay model, we first want to check the results we get by increasing the number of parameters for the waveform model just by one to, say, *p1* and *p2* instead of the transition time t_{in}:

$$delay = f(p1_{in}, p2_{in}, C_L)$$
$$p1_{out} = g(p1_{in}, p2_{in}, C_L) \quad (5)$$
$$p2_{out} = h(p1_{in}, p2_{in}, C_L)$$

It is possible (at least in a gate-level timing analyzer) to propagate the waveform parameters without ever needing to plot the waveforms (*p1* and *p2* at the output of a gate become the input for the next stage, then equation (5) is applied to propagate them further, and so on). These are the parameters the user learns about and therefore we will call them *user* parameters. It is not necessary that the *natural* and the *user* parameters be the same (although for the saturated ramp model they are). For example, equation (2) could be transformed so natural parameter a is mapped into the user parameter t_0:

$$y = e^{-b\cdot(t-t_0)} \quad where \quad t_0 = \ln(a)/b \quad (6)$$

In order to be more easily accepted by the design community, a waveform model should keep the transition time as a *user* parameter, regardless of the *natural* parameters of the model equation. This property makes it possible to mix-and-match old and new models easily, revert to previous methodologies and maintain the intuition that designers have formed for the single-parameter model.

To gain some intuition about the second *user* parameter one could easily plot a set of typical waveforms from a design and scale the time axis for each of them such that all have the same t_{in} (in our case the same 20% to 80% transition time). What we can observe from such a plot is the difference in "shape" between the waveforms. We would like to see some number associated with this "shape."

We define the parameter k as a shape factor that has some physical meaning attached to it. The shape factor k is associated with the shape of the waveform when its voltage value is between 20% and 80% of VDD. As a design decision, we force the value of k to be zero for a standard waveshape such as the output of an inverter loaded by four copies of itself. We could force the value of k to be negative for normal waveshapes such as the output of any CMOS gate and positive for strange waveshape such as complex *RC* responses (an example of this is presented in Figure 1).

2.2 CDF-based waveform models

As mentioned in the introduction, many of the waveshapes seen on circuits appear to resemble CDFs of probability distribution functions, such as the Gamma distribution and the Weibull distribution [6]. Gamma and Weibull distributions have been used before to compute interconnect delay [7] -[8].

Equations (7) and (8) show expressions for CDFs of the Gamma distribution and Weibull distribution respectively.

Gamma:

$$G(t,n,\lambda) = 1 - \frac{\Gamma(n,\lambda t)}{\Gamma(n)} \quad \forall t \geq 0$$
$$\Gamma(n) = \int_0^\infty y^{n-1}e^{-y}dy \quad and \quad \Gamma(n,\lambda t) = \int_{\lambda t}^\infty y^{n-1}e^{-y}dy \quad (7)$$

Weibull:

$$W(t,\alpha,\beta) = 1 - e^{-\left(\frac{t}{\beta}\right)^\alpha} \quad \forall t \geq 0 \quad (8)$$

These two distributions have the desired parameters, the time-scaling factor and the shape factor. For a Gamma CDF, parameters λ and n in equation (7) explicitly represent the time-scaling factor and the shape factor, respectively. For the Weibull distribution, the parameters β and α in equation (8) represent only approximately the time-scaling factor and the shape factor, respectively.

Although Gamma CDFs can resemble a variety of shapes, it is not well suited for analytical computations. The Gamma distribution requires evaluating complicated integrals. Even using lookup tables, mapping a PWL waveform to (λ, n) values requires a non-linear regression. Therefore, we will concentrate on the Weibull waveform model.

Figure 3 shows a representative sample of Weibull distributions for different values of α and β for the same 20% to 80% transition time. The figure shows that the Weibull distribution can be used to fit the wide range of complex non-linear waveshapes observed on high performance circuits. As α changes from 0.1 to 3.0, the shapes change from those similar to more complicated *RC* responses to standard shapes similar to the output of an inverter. If a ramp is used to model these complex waveforms, all of the waveforms will map on to the same ramp. This causes significant error in approximating the original waveforms.

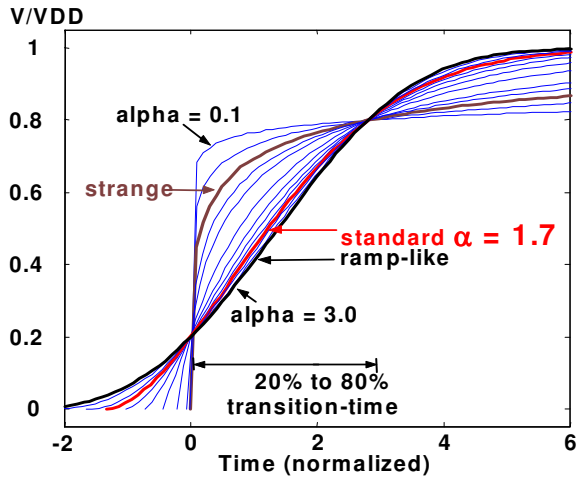

Figure 3 Examples of Weibull CDFs (Note: β computed from equation (11) using α and transition time)

2.3 *Natural* and *user* parameters for Weibull-based waveform models

To preserve the transition time as a user parameter and to align ourselves with the *natural/user* parameter approach we propose the transition time Δt and shape factor k as user parameters, to replace the Weibull natural parameters α and β. By imposing the shape factor k to be zero for a "standard" waveform, and defining the "standard" waveform as the output of an inverter loaded by

four identical inverters we come to the following relationship between k and α:

$$k = -(\alpha - \alpha_0) \quad (9)$$

α_0 is technology dependent and in our case we used a value of 1.7. The transition time t_{out} can be derived analytically from equation (8). Let $t_{20\%}$ and $t_{80\%}$ be the time points when the measured voltage values of (t,v) waveform reach 20% and 80% of VDD, respectively. Equation (10) shows their analytical expressions.

$$t_{20\%} = \beta \cdot (\log(1.25))^{1/\alpha} \quad and \quad t_{80\%} = \beta \cdot (\log(5))^{1/\alpha} \quad (10)$$

The transition time t_{out} is simply $t_{80\%}$-$t_{20\%}$ and is given by (11).

$$t_{out} = t_{80\%} - t_{20\%} = \beta \cdot \left((\log(5))^{1/\alpha} - (\log(1.25))^{1/\alpha} \right) \quad (11)$$

Moreover, the same equations (9) and (11) can be used to obtain (α, β) if the pair (k, t_{out}) is known. Thus, designers have the convenience to use the set of parameters (k, t_{out}) without any concern about the underlying waveform model used in timing analysis tools.

3. PARAMETER EXTRACTION

We describe how parameters (α, β) are obtained from a PWL waveform.

3.1 Parameter estimation

An important step in using any waveform model is the mapping of a signal given as a (time, value) vector pair to the model function (by computing the parameters best fitting the original). This procedure is applied during gate characterization for the output waveform after each simulation. It is also applied by a transistor-level static timing analyzer after each circuit simulation to compress the output waveform data. The second case is the most demanding in terms of the parameter mapping efficiency. For the classical one-parameter model this step consists of determining the 20% and 80% points on the waveform and finding the difference between them.

For the Weibull-based model we start from a variation of (8) which introduces a time shift parameter t_0 whose meaning will be explained later on.

$$W(t, t_0, \alpha, \beta) = 1 - e^{-\left(\frac{t - t_0}{\beta}\right)^{\alpha}} \quad (12)$$

For now let us consider the case with t_0 equal to zero. After rearranging the terms and applying the natural logarithm, we have

$$\ln(1 - W) = -\left(\frac{t}{\beta}\right)^{\alpha} \Rightarrow \left(\frac{t}{\beta}\right) = \left[\ln\left(\frac{1}{1 - W}\right)\right]^{\frac{1}{\alpha}} \quad (13)$$

Again taking natural logarithm of equation (13) and after some rearrangement, we obtain

$$\ln(t) = \ln(\beta) + \frac{1}{\alpha} \ln\left(\ln\left(\frac{1}{1 - W}\right)\right) \quad (14)$$

Equation (14) is a linear expression with variables $\ln(t)$ and $\ln(\ln(1/(1-W)))$ and parameters $\ln(\beta)$ and $1/\alpha$:

$$y = b + ax \quad (15)$$

where

$$y = \ln(t), b = \ln(\beta), a = \frac{1}{\alpha}, x = \ln\left(\ln\left(\frac{1}{1 - v}\right)\right), and\ v = W.$$

The high-level fitting algorithm to obtain α and β for any given (time, value) waveform is presented in Figure 4.

WEIBULL_FITTING(t,v)

1. Obtain time-value (t,v) waveform from circuit simulation.
2. Normalize v by VDD.
3. If (t,v) represents a falling transition, set $v = 1-v$.
4. Select 5-6 points (t_i, v_i) from the set (t,v) for fitting.
5. Perform a linear regression (least-squares method) on equation (15) to obtain b and a
6. Obtain α and β using equation (14) and (15) and return.

Figure 4 High-level Weibull fitting algorithm

It is important to determine what points to pick for step 4 of the fitting algorithm. These points should come from the region of signal that has the most influence on the propagation delay and the transition time of the output. We measured the delay through an inverter for the set of Weibull curves shown in Figure 3. Our experiments showed that variation in shape in the 0% of VDD to 20% of VDD region of input waveforms contributed around 5% variation in delay through the inverter. Similarly, the 80% to 100% region contributed around 1% variation in delay. However, variation in shape in the 20% to 80% region of the input waveforms contributed as much as 95% variation in delay. Thus, a good choice of points for fitting would be a set of points that fall in the region where their value is between 20% and 80% of VDD. Experimentally we determined that only 5-6 points are necessary for the fitting process.

Step 5 of the fitting algorithm requires a linear regression and least squares method should suffice for implementing this method. However, as we show in the following sub-section, implementation of step 5 requires some consideration of time-shifting the measured waveform.

3.2 Implementation

Used as presented in the previous section, the fitting algorithm from fits delay and not the shape. Figure 5 shows three identical original signals shifted in time-domain and their Weibull models produced by the fitting algorithm. Ideally, the fitting algorithm should produce the same α and β for all the three waveforms but that is not the case here. To solve this time-shift problem, we need a modified Weibull function with an extra parameter, t_0, which allows for time shifting as described in (12). The problem of estimating the parameters for the modified Weibull function can be reduced to a form equivalent to (14) given by:

$$\ln(t - t_0) = \ln(\beta) + \frac{1}{\alpha} \ln\left(\ln\left(\frac{1}{1 - W}\right)\right) \quad (16)$$

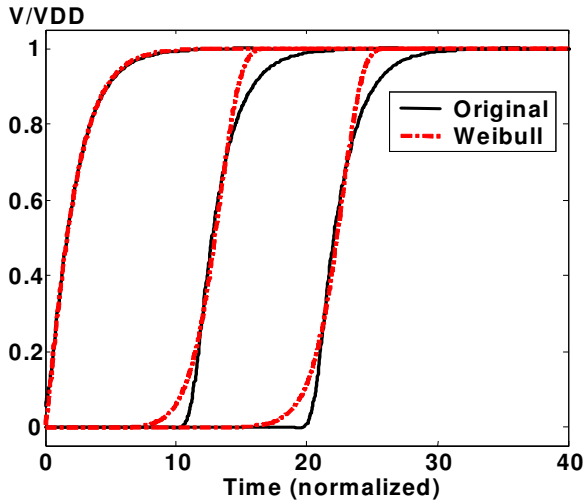

Figure 5 Time-shift problem

Note that this is still a two-parameter model since t_0 is not saved once α and β are obtained. However, now the regression is no longer linear and we have to use an iterative or heuristic method to find a good enough t_0 that minimizes least squares fitting error.

The goal of the fitting algorithm is to find α, β, and t_0 that minimize the least squares fitting error for equation (16). Equation (17) gives the expression for the square of fitting error for m (time, value) measurements with (t_i, v_i) as the measured points.

$$E(t_0,\alpha,\beta)=\sum_{i=1}^{m}\left(v_i-W(t_i,t_0,\alpha,\beta)\right)^2 \qquad (17)$$

Equation (17) poses a three-dimensional problem. However, it can be easily translated to one-dimensional problem by noting that once t_0 is fixed, α and β can be obtained by a simple linear regression on equation (15) by using $t = t_{measured} - t_0$. Thus, (17) can be rewritten as:

$$E(t_0)=\sum_{i=1}^{m}\left(v_i-W(t_i,t_0,\alpha(t_0),\beta(t_0))\right)^2 \qquad (18)$$

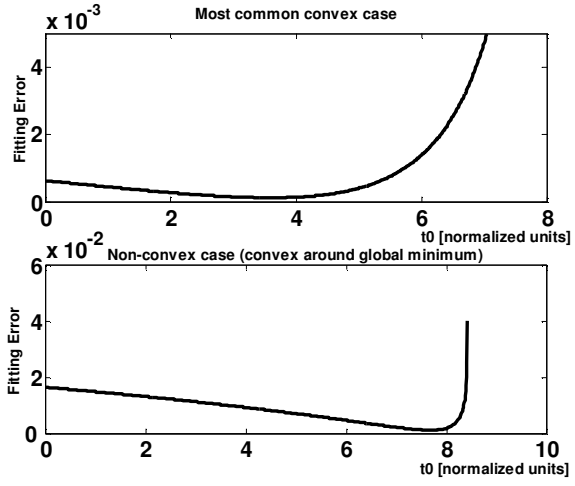

Figure 6 Convexity of fitting error

Minimum E can be obtained easily using a Newton's method [10] if E is convex with respect to t_0. Figure 6 plots $E(t_0)$ for two cases extracted from our benchmark set. The upper plot shows a typical case. The lower plot represents the worst-case from a convexity point of view that we encountered. A good starting point for iterative Newton's method can always be chosen as $t_{0,initial}$ = min(t_i) for i=1..m. This point corresponds to the boundary point on curve $E(t_0)$ after which $E(t_0)$ is complex because $t_i - t_0 \le 0$ if $t_i \le t_0$ and $\ln(t_i - t_0)$ is undefined for such case in real domain. Also note that the choice of initial point $t_{0,initial}$ = min(t_i) is also good because we can always reach the global minimum of $E(t_0)$ from that starting point as $E(t_0)$ is convex between $t_{0,initial}$ and the global minimum. Figure 7 shows the distribution for number of iterations required to obtain good values of t_0, α, and β for 2000 sample cases.

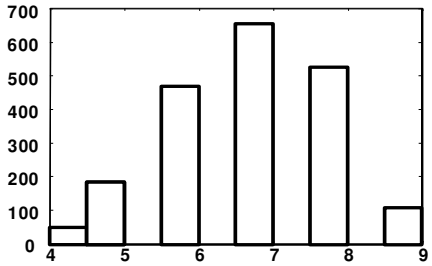

Figure 7 Histogram of number of iterations for non-linear fitting

4. GATE CHARACTERIZATION

The practicality of any waveform model also depends on how easy it is to use it in a design flow. The model has to be amiable to gate characterization. In this section, we present a gate characterization method for the Weibull-based model. The model's realizability is illustrated on many typical single and multiple input gates.

4.1 Gate characterization parameters and equations

To be consistent with the natural parameter approach, we characterize gates in terms of the transition time Δt, the shape factor k, and the output loading C_L. Thus, our goal is to determine the following three functions for any given gate and input.

$$\begin{aligned} delay &= f(\Delta t_{in}, k_{in}, C_L, a_1, a_2, ...) \\ \Delta t_{out} &= g(\Delta t_{in}, k_{in}, C_L, b_1, b_2, ...) \\ k_{out} &= h(\Delta t_{in}, k_{in}, C_L, c_1, c_2, ...) \end{aligned} \qquad (19)$$

Note that the functions $f(.)$, $g(.)$, and $h(.)$, will have the same form for all the gates but the constants a_1, a_2, …, b_1, b_2, …, c_1, c_2, …, etc. will be unique for a given gate and input conditions. Before we determine these functions and constants, it is necessary to determine the ranges of natural parameters Δt, k, and C_L over which the gates will be characterized.

It was observed for many circuits that the shape factor k ranges from -1.3 to 1.2 for an overwhelming majority of signals; hence we chose to characterize gates for $k \in$[-1.3,1.2]. This corresponds to α in the range [0.5,3.0] (equation (9)). Note that α in this range

covers all of the waveshapes shown in Figure 3. To determine the range for C_L, we observe that the output loading capacitance for typical CMOS gates is roughly 1x-10x the size of input capacitance. The input capacitance for any given gate can be obtained as follows – determine equivalent inverter for the gate, drive the inverter through a high resistance, measure the delay across that resistance and compare it with an *RC* delay where *C* is the gate input capacitance we are trying to compute. The minimum Δt necessary for characterization can be computed as follows – load a minimum size inverter with a copy of itself (which is also loaded by a similar inverter), apply a step input to first inverter and obtain the output transition time, apply the output of first inverter iteratively to its input until its transition time converges. Maximum Δt can be obtained in a similar fashion except that the second inverter in the chain should be replaced by an inverter of roughly 10x the minimum size.

Equation (20) shows the form of functions *f(.)*, *g(.)*, and *h(.)* that fits well with the Weibull-model for the range of parameters described above. Equation (20) has very few terms (maximum of nine). This simple form and high accuracy of characterization equations makes the Weibull-model highly suitable for gate characterization. After gates are characterized for the Weibull model, it is possible (at least in a gate-level timing analyzer) to propagate the Weibull waveform parameters without ever needing to plot the waveforms.

$$
\begin{aligned}
delay &= a_1 + a_2 k_{in} + a_3 k_{in}^2 + a_4 \Delta t_{in} + a_5 \Delta t_{in}^2 + a_6 \frac{1}{C_L^3} + \\
&\quad a_7 C_L + a_8 \frac{\Delta t_{in}}{C_L} + a_9 k_{in} \Delta t_{in} C_L \\
\Delta t_{out} &= b_1 + b_2 k_{in} + b_3 k_{in}^2 + b_4 \Delta t_{in} + b_5 \frac{1}{C_L} + b_6 C_L + \\
&\quad b_7 C_L^2 + b_8 \frac{C_L}{\Delta t_{in}} \\
k_{out} &= c_1 + c_2 k_{in} + c_3 \frac{1}{\Delta t_{in}^2} + c_4 \Delta t_{in} + c_5 \frac{1}{C_L} + c_6 C_L + \\
&\quad c_7 k_{in} C_L^2 + c_8 \frac{\Delta t_{in}}{C_L} + c_9 \frac{1}{\Delta t_{in} C_L^3}
\end{aligned}
\qquad (20)
$$

4.2 Gate characterization results

We characterized 22 different single and multiple input gates with single input switching conditions. We ran SPICE simulations on an equally spaced 4x4x4 grid of Δt_{in}, k_{in}, and C_L (total of 64 points) and measured delay and Δt_{out}. The shape factor k_{out} was obtained from the output waveform using the methodology described in section 3. We used a modified version of least squares fitting to obtain the constants a_1-a_9, b_1-b_8, and c_1-c_9 that minimize the relative error between (20) and the measured values. The measured values for an equally spaced 7x7x7 grid of Δt_{in}, k_{in}, and C_L covering the same range as the grid used for fitting were compared with values obtained from equation (20).

Simulation results show that delay, Δt_{out}, and k_{out} are smooth functions of Δt_{in}, k_{in}, and C_L and thus equation (20) approximates the actual values accurately. Table 1 shows the results for all the simulated gates and input combinations.

It is clear from the table that most of the errors are well below 5%. Some of the large errors in shape factor appeared as overestimates done by equation (20) for measured α>1.9. As shown in Figure 3, α>1.9 hardly changes the shape of the Weibull curve and thus the large errors in shape factor hardly have a physical impact. Moreover, errors in shape factor translated to well below less than 1.5% error in delay and output transition time of the next gate for almost all the cases and less than 5% error for all the cases.

Table 1 Gate Characterization Errors in % for 7x7x7 grid of (Δt_{in}, k_{in}, C_L) (measured values vs. equation (20))

	Delay			Transition Time			Shape Factor		
Gate	max |err|	avg err	std dev	max |err|	avg err	std dev	max |err|	avg err	std dev
INV A↑,X↓	3.18	-0.24	1.29	5.04	-0.13	1.85	6.53	0.66	2.37
INV A↓,X↑	3.86	-0.34	1.43	3.74	-0.04	1.16	8.86	-0.08	2.27
NAND2 A↑,X↓	3.78	-0.21	1.40	5.15	0.17	2.19	15.56	2.08	3.75
NAND2 B↓,X↑	3.35	-0.27	1.46	3.76	0.09	1.10	10.58	-0.17	2.44
NOR2 A↑,X↓	3.01	-0.29	1.25	4.85	-0.01	1.78	5.76	0.36	2.16
NOR2 B↓,X↑	3.94	-0.29	1.29	5.12	0.19	1.36	5.86	-0.32	2.20
AND2 A↓,X↓	1.90	-0.03	0.51	2.35	-0.26	0.78	5.67	0.25	1.38
AND2 B↑,X↑	2.69	-0.05	0.67	2.65	0.00	0.46	3.31	-0.05	0.99
OR2 B↓,X↓	1.14	-0.03	0.33	1.90	-0.21	0.77	3.79	0.22	1.28
OR2 A↑,X↑	1.06	-0.09	0.29	2.80	-0.35	0.98	1.53	-0.07	0.44
NAND3 A↑,X↓	3.65	-0.37	1.30	4.78	0.02	2.00	7.42	1.21	2.48
NAND3 B↑,X↓	3.00	-0.26	1.00	4.26	0.22	1.66	4.00	0.13	1.17
NAND3 C↑,X↓	2.82	-0.19	1.17	3.30	0.24	1.42	2.80	-0.34	0.92
NOR3 A↑,X↓	3.06	-0.20	1.21	4.49	0.11	1.64	6.15	0.38	2.20
NOR3 B↑,X↓	2.98	-0.26	1.23	4.76	0.07	1.66	5.81	0.36	2.14
NOR3 C↑,X↓	3.03	-0.27	1.26	5.03	-0.16	1.79	5.74	0.01	2.35
AND3 A↓,X↓	2.45	-0.01	0.64	5.75	0.43	1.83	3.01	-0.09	0.97
AND3 B↓,X↓	3.25	0.01	0.72	5.36	0.44	1.71	2.56	-0.09	0.92
AND3 C↓,X↓	4.29	-0.03	0.86	5.19	0.49	1.73	2.71	-0.07	0.96
OR3 A↓,X↓	1.21	-0.05	0.33	5.43	0.46	1.61	3.10	-0.08	1.01
OR3 B↓,X↓	0.99	-0.07	0.30	5.33	0.41	1.75	3.37	-0.10	1.10
OR3 C↓,X↓	1.30	0.00	0.29	5.22	0.42	1.67	3.27	-0.15	1.00

5. RESULTS

Let us first revisit the example shown in Figure 1. The Weibull model for the input waveform dramatically improves the results as shown in Figure 8. The delay error produced by Weibull approximation was 0.02%. The delay errors produced by ramp and standard shape were 14% and 9%, respectively. Similarly, Weibull approximation reduced transition time error down to 2.4% from 19% produced by ramp approximation and 11% produced by standard shape approximation.

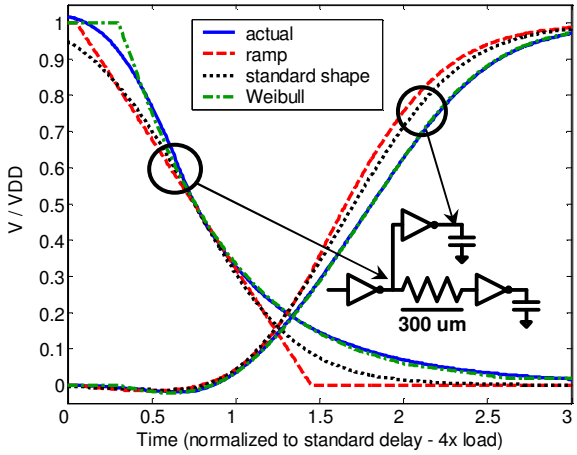

Figure 8 Weibull approximation for Figure 1

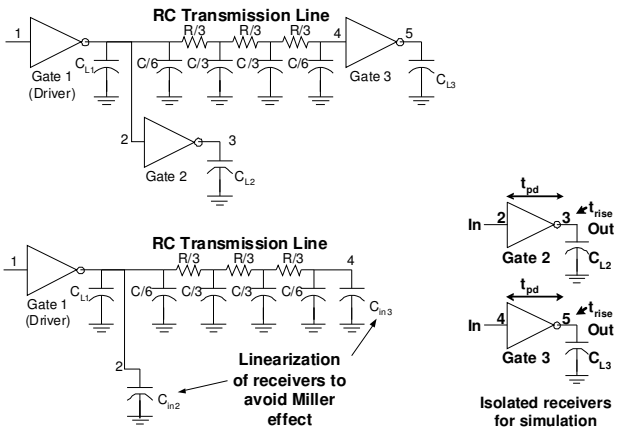

Figure 9 Synthetic benchmark for testing

In order to test the model on a more frequently occurring set of waveforms, we generated a synthetic benchmark on an industrial 90nm technology using the circuit shown in Figure 9. Voltage waveshapes were sampled at receiver inputs (nodes 2 and 4) by forcing a ramp on driver input (node 1). We obtained 1000 different circuits by varying the transition time at node 1, sizing of the gates, sizing of interconnect (length), impedance (length and metal layer) of interconnect relative to that of gates, and PMOS to NMOS transistor ratios for the gates. The combination of circuit parameters reflected industrial design guidelines. We must note that the interconnect length used in our benchmark varied between 100μm and 500μm. These lengths are quite common not only on microprocessors but on many other designs.

A check was also placed to ensure that the benchmark circuits generated by varying the above factors do not produce unrealistic waveforms. For example, we enforced that the interconnect path delay does not exceed the Elmore delay for this technology, otherwise there would have been a repeater on the interconnect line. Loading of gates 2 and 3 was varied to catch the sensitivity of the gate delay and the output transition time with respect to the shape of input waveform and the loading.

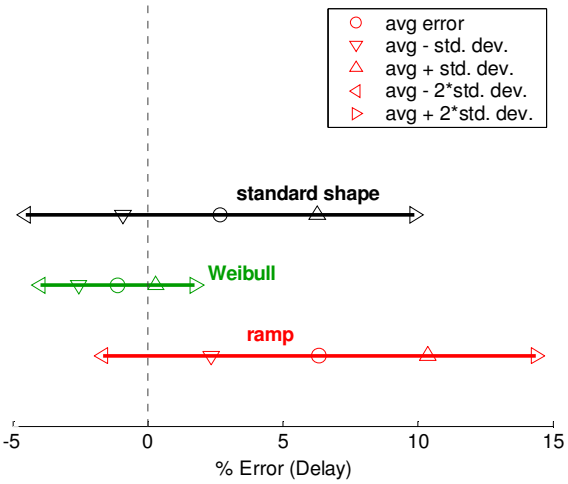

Figure 10 Delay error distribution

The 2000 waveforms obtained using the circuit in Figure 9 were approximated using ramps having their corresponding transition times (taken as 20% to 80% of VDD). These were fed as input to the receivers and the input to output delay and the output transition time were measured for all these waveforms. The results are shown in Figure 10. The errors incurred by the "standard shape" model (as described in Section 1) and the Weibull model are also shown.

5.1 Impact on noise

The Weibull model also offers other advantages over the ramp model. The Weibull model provides a smooth model for approximating waveforms. Hence we expect it to introduce less noise in the circuit when it is used for timing simulation and performance verification. Unlike the original waveforms and the Weibull model, a ramp model is not smooth and consequently it introduces noise that is not present on the real circuit. We used two coupled transmission lines to compare noise produced by the ramp model and the Weibull model for the 2000 waveforms in the experiments. Original waveforms and their ramp and Weibull approximations were placed on the aggressor net and the peak voltage due to cross coupling noise was measured on the quiet victim net. Noise produced on the victim net by the Weibull waveform on the aggressor net was very close to the noise produced on victim net by the original waveform on the aggressor net. Moreover, the Weibull approximation of original waveforms produced 9.4% less noise on average compared to ramp approximation (Figure 11). This is in line with our expectations and thus the Weibull approximation improves timing analysis accuracy for coupled circuits.

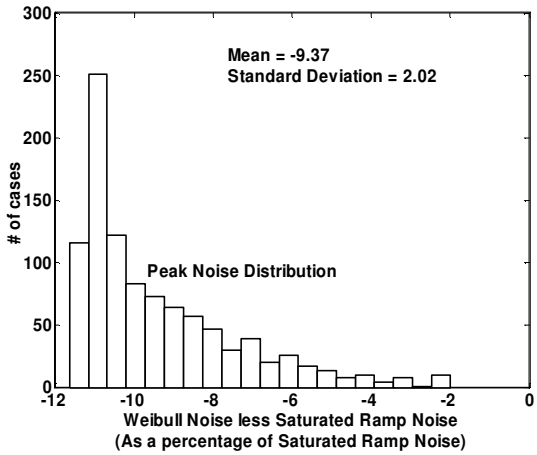

Figure 11 Weibull Noise vs. Saturated Ramp Noise

Using the Weibull model, it is also possible to compute cross-coupling noise analytically. To compute the response of an input waveform described by a transition time and shape factor k, first we need to compute the corresponding parameters α and β of the Weibull model using equations (9) and (11). Given the Weibull parameters α and β of the waveform, the frequency domain representation of the Weibull CDF is

$$W(\alpha,\beta,s)=\frac{m_0}{s}-\frac{m_1}{1!}+\frac{m_2}{2!}s-\cdots \qquad (21)$$

where m_0, m_1, …, etc. are the Weibull PDF moments which can computed analytically [6] as

$$m_i = \beta^i \Gamma\left(1+\frac{i}{\alpha}\right), \quad \Gamma(x) = \int_0^\infty y^{x-1} e^{-y}\, dy\ . \tag{22}$$

The moments m_i can be computed very quickly because the gamma function $\Gamma(x)$ is a well known mathematical function that is implemented efficiently in many math libraries. Since the circuit waveforms are modeled using Weibull, the response (including cross-coupling noise) $Y(\alpha,\beta,s)$ at any node on an interconnect circuit with transfer function $H(s)$ can be computed as

$$Y(\alpha,\beta,s) = W(\alpha,\beta,s)H(s) \tag{23}$$

with $W(\alpha,\beta,s)$ as the input to the circuit. Using standard moment matching techniques, $Y(\alpha,\beta,s)$ can be converted easily to any desired waveform model. That model can then be used to obtain the time-domain response.

6. CONCLUSIONS

In this paper, we have shown that modeling of signal waveshapes using the CDF of a Weibull distribution is significantly more accurate than using a one-parameter ramp approximation without requiring a significant runtime overhead. Experimental results show that the Weibull model can bring down the error in delay from ±15% to less than ±5%. Similarly, transition time error was brought down from ±19% to less ±5%. Thus, the Weibull model offers more accuracy without a significant loss in speed during timing analysis. The Weibull model is also highly suitable for gate characterization. Results show that errors in delay and transition time estimation are well below 5% for many single and multiple input gates. Moreover, the Weibull approximation offers other advantages such as improved accuracy in noise calculations and convenience in linear circuit analysis. Since the Weibull distribution covers the variety and complexity of waveshapes occurring on real circuits, it is well suited for timing analysis applications. Our future work will include waveform modeling for more complex waveshapes that show ringing and glitching effects.

7. REFERENCES

[1] Krauter, B. and Mehrotra, S., "Layout based frequency dependent inductance and resistance extraction for on-chip interconnect timing analysis," Proceedings of the 35th ACM/IEEE Design Automation Conference, pp 303-308, 1998.

[2] R. B. Hitchcock, G. L. Smith, and D. D. Cheng, "Timing analysis of computer hardware," IBM Journal of Research and Development, Vol. 26, 1982, pp. 100-105.

[3] Miki, Y., Abe, M., and Ogawa, Y., "PCHECK: A delay analysis tool for high performance LSI design," IEEE Custom Integrated Circuits Conference, pp 267-270, 1995.

[4] Dartu, F. and Pillage, L. T., "Modeling signal waveshapes for empirical CMOS gate delay models," 6th Intl. Workshop PATMOS '96, pp 57-66, 1996.

[5] Hashimoto, M., Yamada Y., and Onodera H., "Capturing crosstalk-induced waveform for accurate static timing analysis," Proceedings of ACM/SIGDA ISPD, pp 18-23, 2003.

[6] Hayter, A. J., *Probability and Statistics for Engineers and Scientists*, Second Edition. Duxbury Press, 2002.

[7] Liu, F., Kashyap, C., and Alpert, C., "A delay metric for RC circuits based on the Weibull distribution," Proceedings of the IEEE/ACM International Conference on Computer Aided Design, pp 620-624, 2002.

[8] Lin, T., Acar, E., and Pileggi, L., "h-gamma: An RC delay metric based on a Gamma distribution approximation of the homogenous response," Proceedings of the IEEE/ACM International Conference on Computer Aided Design, pp 19-25, 1998.

[9] Weste, N. H. E. and Eshragian, K., *Principles of CMOS VLSI Design*, 2nd edition, Addison-Wesley Publishing Company, 1992.

[10] Nocedal, J. and Wright, S., *Numerical Optimization.* Springer Series in Operations Research, 1999.