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FOREWORD

On behalf of the ICCAD 2003 Executive and Technical Program Committees, we would like to welcome you to the International Conference on Computer Aided Design. We hope that you enjoy this key event of our professional community and learn much about the latest advances in electronic design technology and automation.

As part of the continuing effort to keep the conference focused on the emerging problems of our field, ICCAD 2003 broadened its scope and, for the first time, actively solicited papers in the area of innovative design technologies for devices, circuits, and systems. This year, ICCAD attracted a record number of submissions, totaling 490 papers. From this pool of submissions, 129 papers were selected and compiled into an exciting technical program which is further enriched by multiple special sessions and events.

After its successful introduction in 2002, this year's ICCAD Sunday Workshop will be focused on emerging design problems and include six expert presentations on various ASIC, FPGA, and microprocessor design challenges. At the same time, the second "ACM/SIGDA CADathlon at ICCAD" will take place - a programming competition that gives students the opportunity to demonstrate their CAD knowledge and their skills in problem solving, programming, and teamwork. The Sunday program will be concluded by the ICCAD Opening Reception and the Sunday panel entitled "CAD for High-End Design: Help, Hope or Hype?"

The main ICCAD program begins on Monday morning with the conference keynote entitled, "CMOS, Scaling, and the Future" given by Mark Horowitz, Stanford University. The core technical program of the conference is composed of 37 regular paper sessions and six exciting embedded tutorials on "Design and CAD Challenges", "System Level Design and Verification", "Mixed Signal DFT", "Manufacturing-Aware Physical Design", "Dynamic Power Management", and "Large-Scale Circuit Placement". The Monday evening panel entitled "Semiconductor Slowdown: Who Will Blink First?" will discuss different viewpoints on the rapidly growing challenges from increasing integration densities and how design automation can help to address them.

Multiple side events complement the technical conference program and enrich the overall ICCAD schedule. The Technology Fair on Tuesday will provide a forum where conference attendees can meet industrial R&D colleagues to discuss technical problems and solutions, or to simply make new contacts for future relationships. The ICCAD Dinner on Tuesday evening is the social highlight of the conference and will establish a relaxed atmosphere for meeting other attendees and provide a chance to enjoy some exciting entertainment. The conference schedule concludes on Thursday with four new full day tutorials on 1) "Linux for EDA", 2) "Leakage Issues in IC Design: Trends, Estimation and Avoidance", 3) "Recent Advances in Formal Verification" and 4) "Embedded Software Development".

On behalf of the organizers of ICCAD, we would like to thank all people involved in preparing the 2003 event, in particular, the members of the Executive and Technical Program Committees, everyone at MPAssociates, and the many volunteers from our sponsoring societies. Last but not least, we would like to express our gratitude to all of the authors who submitted papers, since these contributions form the backbone of the conference.

We hope that you will enjoy the conference program and also find enough time to meet with your colleagues and friends for catching up on the latest in your work.

Andreas Kuehlmann
General Chair

Hidetoshi Onodera
Technical Program Chair
William J. McCalla ICCAD Best Paper Award
The "Best Paper Awards", selected by the ICCAD Program Committee, were selected through a rigorous and multi-stage review process. The Awards are given in memory of William J. McCalla, for his contributions to ICCAD and his CAD technical work through his career.

Noise Analysis for Optical Fiber Communication Systems
Paper 6C.1
Author: Alper Demir
Affiliation: KOC University, Sariyer-Istanbul, Turkey

Block-Based Static Timing Analysis with Uncertainty
Paper 8B.1
Author: Anirudh Devgan
Affiliation: IBM Research, Austin, TX

Author: Chandramouli Kashyap
Affiliation: IBM Microelectronics, Austin, TX

The following IEEE CAS Society Award will be presented at ICCAD.

CAS Industrial Pioneer Award
Prabhu Goel
Tharas Systems, Inc., Santa Clara, CA

For his contributions to design modeling and design verification through Verilog and Verilog based design tools that dramatically boosted the productivity of design engineers.

2003 SIGDA Outstanding New Faculty Award
Dennis Sylvester
Univ. of Michigan., Ann Arbor, MI

The SIGDA Outstanding New Faculty Award recognizes a junior faculty member early in her or his academic career who demonstrates outstanding potential as an educator and researcher in the field of electronic design automation. The award is presented annually at ICCAD, and consists of a $10,000 grant supporting the faculty member's research program, as well as a citation.
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ICCAD-2003 KEYNOTE

Mark Horowitz
Professor
Stanford Univ., Stanford, CA

CMOS, SCALING, AND THE FUTURE

Description: Technology scaling has driven integrated circuit designers for the past four decades, both enabling them to create ever more complex electronic systems, but also forcing them to change the way that they think about design. This talk is a mostly serious look at the factors driving designers today, looking at design issues that future designers will need to face.

Although technology scaling is a predictable and smooth process, designer's response is not smooth, and often has step-like changes when new tools or techniques are introduced. Some of the most dramatic design changes occur when the basic circuit technology changes, but other design changes can be as large, like the introduction of HDL and synthesis. We are currently facing a number of issues which might lead to large changes in design. The most critical is power. Previous shifts in circuit style, from bipolar (TTL and ECL, if you are old enough to remember) to nMOS, and then from nMOS to the CMOS style we have been using for roughly the past 20 years were partially driven by power issues. Yet today's CMOS chips dissipate more power than even the old bipolar chips did, and the scaling trends are not promising. The looming power constraints will force us to worry about performance efficiency instead of performance, since in the future the peak performance solution will always dissipate too much power.

Biography: Mark Horowitz is the Yahoo Founder's Professor of Electrical Engineering and Computer Science at Stanford University. He received his BS and MS in Electrical Engineering from MIT in 1978, and his PhD from Stanford in 1984. Dr. Horowitz is the recipient of a 1985 Presidential Young Investigator Award, and an IBM Faculty Development Award, as well as the 1993 Best Paper Award at the International Solid State Circuits Conference.

Dr. Horowitz's research area is in digital system design, and he has led a number of processor designs including MIPS-X, one of the first processors to include an on-chip instruction cache, TORCH, a statically-scheduled, superscalar processor that supported speculative execution, and FLASH, a flexible DSM machine. He has also worked in a number of other chip design areas including high-speed and low-power memory design, high-bandwidth interfaces, and fast floating point. In 1990 he took leave from Stanford to help start Rambus Inc., a company designing high-bandwidth chip interface technology. His current research includes multiprocessor design, low power circuits, memory design, and high-speed links.
TUTORIAL 1

LINUX FOR EDA

Speakers:

Stephen Edwards – Columbia University, New York, NY
Tom Grotton - Cadence Design Systems, Inc., San Jose, CA
Tim Marriott – Synopsys, Inc., Santa Clara, CA
Mel Nicholson – Synopsys, Inc., Santa Clara, CA
Fabio Somenzi – Univ. of Colorado, Boulder, CO

Background: Over the last three years a large number of EDA tools have become available under Linux. While it is clear that the EDA industry has adopted Linux as one of the main platforms, the process of migrating applications to it has not reached maturity yet. This tutorial is therefore addressed to people involved in developing, porting, or deploying EDA software in the Linux environment. The tutorial will cover portability issues, programmer productivity tools, and performance analysis tools. The tutorial will also include a section on grid computing and the benefits and complexities of using parallel computing for CAD applications. Finally, the tutorial will include a discussion of the challenges involved in making Linux the main development platform.

The tutorial is intended for designers and CAD engineers interested in Linux as a CAD platform. Basic background in software development is useful though not needed.
TUTORIAL 2

LEAKAGE ISSUES IN IC DESIGN:
TRENDS, ESTIMATION AND AVOIDANCE

Speakers:

Siva Narendra – Intel Labs., Hillsboro, OR
David Blaauw – Univ of Michigan, Ann Arbor, MI
Anirudh Devgan – IBM Research, Austin, TX
Farid Najm – Univ. of Toronto, Toronto, ON, Canada

Background: Leakage power is emerging as a key challenge in IC design. Traditionally, leakage has been considered as an important design variable in handheld devices and in standby circuit operation. However, this significant increase of leakage now warrants that it be considered as the key design variable in all IC designs. This tutorial presents a comprehensive review of leakage power issues in IC design. The tutorial is organized in four major parts. The first part provides an overview of technology and scaling trends which are causing the significant increase in leakage current. The device physics that leads to sub-threshold and gate leakage will be described, along with their dependence on circuit design variables. The second part of the tutorial will focus on circuit level leakage estimation and avoidance. Comprehensive description of multiple-Vt techniques for leakage avoidance will be presented along with associated leakage estimation techniques. The third part of the tutorial focuses on chip level effects on leakage. Leakage estimation techniques which consider both inter and intra-die process variations will be covered as well leakage minimization techniques such as Adaptive Body Bias (ABB) and power supply control. The final part of the tutorial covers system and circuit architectures for leakage avoidance. In standby mode, the leakage of the circuit can be lowered by putting it a low-leakage state. This section of the tutorial will cover topics including state assignment for leakage minimization, leakage-driven memory and cache circuits and architectures.

The tutorial is intended for designers and CAD engineers interested in next generation design techniques and methodologies and emerging power challenges. Basic background of VLSI and CAD is useful though not needed.
TUTORIAL 3

RECENT ADVANCES IN FORMAL VERIFICATION

Speakers:

- Pei-Hsin Ho - Synopsys Inc., Beaverton, OR
- Ken McMillan - Cadence Berkeley Labs., Berkeley, CA
- Vigyan Singhal - Jasper Design Automation, Inc., Fremont, CA

Background: Recent progress in model checking techniques has allowed formal verification to be applied to larger and more complex design blocks. This tutorial will examine some of the recent methods that have led to a remarkable expansion in the capacity of formal verification tools. The tutorial will be divided into three parts. The first section will discuss iterative abstraction methods. One key to verifying assertions in larger designs is to be able to automatically determine which parts of a design are relevant to a given property. In the past few years, a number of new techniques have been developed for this purpose. This has made it possible in many cases to verify assertions on designs blocks with thousands of registers. The second portion will cover the role of Boolean SAT solvers in model checking. Many recent model checking approaches make use of Boolean satisfiability solvers. We will look at how SAT solvers work, why and in what cases they can be applied effectively to large problems, and how they can be exploited in model checking. The final section will cover predicate abstraction. This approach has made it possible to apply model checking to verify properties of relatively large pieces of software, such as device drivers in the Windows and Linux kernels.

The tutorial is intended for designers and CAD engineers interested in next generation formal verification methods. Basic background of VLSI and CAD is useful though not needed.
TUTORIAL 4
EMBEDDED SOFTWARE DEVELOPMENT

Speakers:

Lance Brooks – Mentor Graphics Corp., Mobile, AL
Mike McGrath – Intel Corp., Chandler, AZ
Vladimir Ivanovic – California State Univ., Hayward, CA

Background: Embedded software development is unlike software development for desktop or network environments. It is unique not only because every embedded device serves a unique purpose, it is different due to the very nature of firmware being very close to specialized hardware. This tutorial will provide an overview of the various pieces involved to develop embedded applications in a cross-target environment, including: integrated development environments for creating the software; compilers and associated tools for building the software targeted for various embedded CPUs and System-on-Chips (SoCs); debuggers designed to debug software running on the many different types of embedded CPU cores; and finally the different types of debug connections to various target execution environments and actual embedded hardware. The tutorial will also cover the specific problems faced by designers writing software prior to the availability of hardware. Attendees will leave with a good understanding of various pieces and the roles they play so they are better prepared to develop embedded software.

The tutorial is intended for designers and CAD engineers interested in the design of embedded software. Basic background in software development and VLSI is useful though not needed.
SUNDAY PANEL:
CAD FOR HIGH-END DESIGN: HELP, HOPE OR HYPE?

Moderator: Leon Stok - IBM Corp., TJ Watson Research Ctr., Yorktown Heights, NY

While it is tempting to think of CAD as the center of the Universe, there is no denying that it’s the designers that really drive what we do. In keeping with the design focus of the ICCAD Sunday Program, this panel brings together speakers from our Sunday Workshop to discuss their views on the current state of CAD for VLSI. Our panelists are designers representing the industry’s most aggressive microprocessor, ASIC and FPGA-based system design efforts. They will share their views of the current state of CAD including: What’s working? What’s not working? And where do we as an industry need to go? This is a perfect forum for CAD professionals to meet their prime customers and for the designers to meet the CAD industry face to face. Will it be a love fest or a slug fest? Come and find out. Moderator Leon Stok is guaranteed to keep the discussion lively.

Panelists:

Stefan Rusu - Intel Corp., Santa Clara, CA
Peter Hofstee - IBM Corp., Austin, TX
Rick Paul - Cisco Systems Inc., San Jose, CA
Jeff Dauber - Apple Corp., Cupertino, CA
Joe Hanson - Altera Corp., San Jose, CA
Richard Vallee - Amirix Systems Inc., Halifax, NS, Canada
MONDAY PANEL:

SEMICONDUCTOR SLOWDOWN: WHO WILL BLINK FIRST?

Moderator: John Darringer - IBM Corp., TJ Watson Research Ctr., Yorktown Heights, NY

The entire electronics industry has benefited from decades of remarkable adherence to "Moore's Law". Is the fantastic ride over? Is this predicted slowdown for real? What will be the limiting factor? Will the technologists finally fail to deliver the sub-100nm factories on time? Will design automation tools be able to deliver completed designs with the needed productivity advances? Or will the designers finally fail to find an economically viable use for a billion transistors on a chip?

To debate these topics we have a distinguished panel of experts from academia and industry representing technology, tools and design. Come prepared with your questions for the open discussion.

Panelists:

Mark Horowitz - Stanford Univ., Stanford, CA
Yoshiharu Furui - Sony Semiconductor Kyushu Corp., Isahaya-shi, Nagasaki-ken Japan
Kerry Bernstein - IBM Corp., TJ Watson Research Ctr., Yorktown Heights, NY
Ivo Bolsens - Xilinx, Inc., San Jose, CA
Joseph Sawicki - Mentor Graphics Corp., Wilsonville, OR
Aki Fujimura - Cadence Design Systems, Inc., San Jose, CA
Bill Grundmann - Intel, Shrewsbury, MA
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Steve Haynal - Intel Corp., Hillsboro, OR

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Kia Bazargan - Univ. of Minnesota, Minneapolis, MN

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Ken McMillan - Cadence Berkeley Labs., Berkeley, CA

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Joerg Henkel - NEC Labs., Princeton, NJ

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Mustafa Celik - Magma Design Automation, Cupertino, CA

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