New Approach to CMOS Current Reference with Very Low Temperature Coefficient

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ABSTRACT

A novel CMOS current reference circuit with very low temperature coefficient is realized, by compensating the temperature performance of the resistor. This circuit gives out a current reference realizing a temperature coefficient of 50 ppm/ºC over the temperature range of (0ºC, 110ºC) and a supply voltage coefficient of 210 ppm/V. This circuit consumes 85 μA at room temperature and can work properly with a supply voltage of 1-V.

Categories and Subject Descriptors

B.7.1 [**Integrated Circuits**]: Types and Design Styles – *VLSI (very large scale integration).*

General Terms

Design

Keywords

Current reference, CMOS, temperature coefficient.

1. INTRODUCTION

The current reference circuit is a key component in analog circuits. Since there is no loss over long metal line for current in contrast with the possible loss for voltage, the current reference is more welcomed in complicated analog circuits where long metal lines are used often.

Moreover, the application environment of modern electronic systems is wider and hostile more and more, which underscores the acute need for reliable operation over a wide temperature range such as from -25ºC to 125ºC. A temperature independent current reference is very desirable for the robustness of such systems.

A temperature independent current reference circuit is introduced in this paper, which can operate with 1-V voltage. It shows excellent immunity to a large temperature variation by taking the temperature performance of the on-chip resistors in consideration.

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2. PROPOSED CIRCUIT ANALYSIS

This current reference circuit is shown in Figure 1. Three components ensure the temperature independence of the reference current. One is the base-emitter voltage V_{BE}, second is a term proportional to absolute temperature (PTAT), and the last is the on-chip resistors. Two diode connected PNP bipolar transistors (Q1 and Q2 in Figure 1) with ratio N drain the same current resulting in a ΔV_{BE} equal to $V_T \ln N$, where $V_T = kT/q$, T is the absolute temperature, and k is the Boltzmann constant. The currents in the nominally equal resistors R_1 and R_2 are proportional to V_{BE1} because of the equality of the two voltages *V1* and *V2* forced by the operational amplifier. Thus

$$I_1 = I_2 = \frac{V_T \ln N}{R_0} + \frac{V_{BE1}}{R_1} \tag{1}$$

To simplify the analysis, the temperature dependences of all the parameters are truncated to the first order, that is to say, it is assumed that all the parameters depend on the temperature linearly. Then V_T can be expressed as

$$V_T = \frac{kT}{q} = \frac{kT_0}{q}\left(1 + \frac{1}{T_0}\Delta T\right) = \frac{kT_0}{q}\left(1 + \alpha \cdot \Delta T\right) \tag{2}$$

Where T_0 is the nominal temperature, and $\Delta T = T - T_0$. Moreover, V_{BE1} can be expressed as

$$V_{BE1} = V_{BE1,T0}\left(1 - \beta \cdot \Delta T\right) \tag{3}$$

All on-chip resistors are temperature dependent also, so R_0 can be express as

$$R_0 = R_{0,T0}\left(1 + \gamma \cdot \Delta T\right) \tag{4}$$

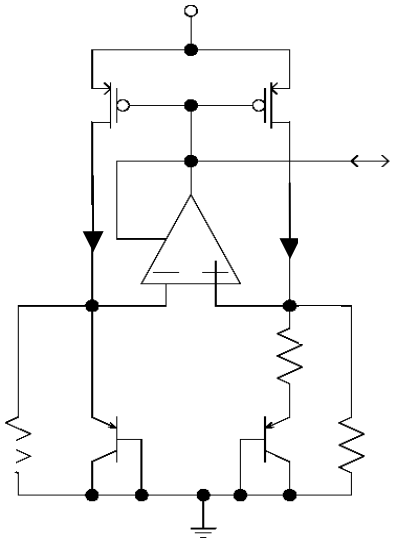
If the ratio of R_1 to R_0 is m, then in order to make I_1 independent of temperature, it should be satisfied that

$$m = \frac{qV_{BE1,T0}}{kT_0 \ln N} \cdot \frac{(\beta + \gamma)}{(\alpha - \gamma)} \tag{5}$$

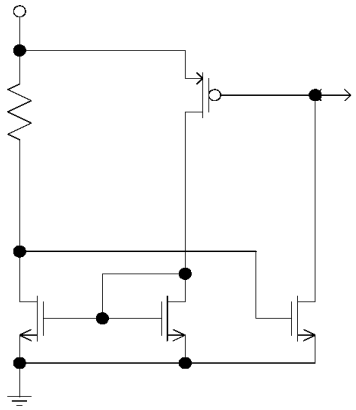
Under this condition, the constant current is

$$I_1 = \frac{1}{R_{0,T0}}\left(\frac{kT_0}{q}\ln N + \frac{V_{BE1,T0}}{m}\right) \tag{6}$$

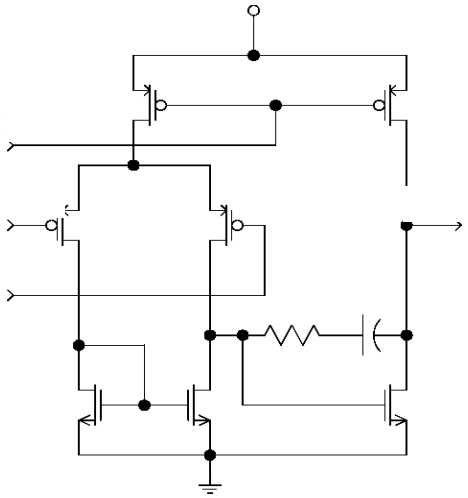
By connecting point *A* to the gates of other PMOS transistors, the temperature-independent currents in M1 and M2 are mirrored to them.



The output currents of this constant current generator may stay at zero without the help of a startup circuit, so some currents should flow through M1, M2 in Figure 1 to bring them out of the dead zone. As shown in Figure 2, the current through resistor *R* is mirrored from the constant current generator, if there are no currents in M1, M2, then the gate of MS is pulled up, as a result, V_A will be pulled down to ground, injecting some finite currents in M1, M2. After the start up phase, the value of R and the current through it make the gate of MS near to ground, thus disabling MS.



The circuit of the amplifier in Figure 1 is shown in Figure 3. PMOS differential pair is used as the input stage in order to accommodate a common mode input voltage as low as V_{BE}. In order to make it work properly under 1-V supply voltage, the bulk terminal of the two PMOS transistors of this input differential pair is connected to their source to eliminate the body effect. In order to minimize the error between the two input ports, the gain should be large enough, which results in the adoption of two stages amplification with current source as the loads. R and C are used for frequency compensation, assuring the stability of the operational amplifier. Furthermore, long channel transistors are used to reduce the mismatch and offset. The bias currents are mirrored from the constant current generator, improving the power supply rejection.



3. COMPARISON WITH OTHER DESIGNS

Although the current reference circuit proposed here is similar with the voltage reference circuit in [1], but the optimum value of *m* and criteria for its selection are different. For the voltage reference circuit, in order to make the voltage independent of temperature, the ratio of R_1/R_0 should be determined by the following equation:

$$m = \frac{qV_{BE1,T0}}{kT_0 \ln N} \cdot \frac{\beta}{\alpha} \tag{7}$$

Compared with the voltage reference circuit, the optimum value of *m* is also affected by the temperature performance of on-chip resistors in the current reference circuit, making the design and optimization of this circuit more difficult.

Deleting R_1 and R_2 in Figure 1, the leaved part is a PTAT current source, which is used as the core of the current reference in [2]. R_0 is an N-well resistor with negative temperature coefficient in [2]. The author claimed that "if the standard PTAT current reference is constructed with a resistor of this nature, a degree of temperature independence can be achieved." This conclusion is very questionable. As shown in Figure 1, if R_1 and R_2 are deleted, then the currents in M1 and M2 are also modified as

$$I_1 = I_2 = \frac{V_T \ln N}{R_0} \tag{8}$$

As $V_T \ln N$ increases with temperature's rise, if R_0 decreases with temperature's rise, it is obvious from equation (8) that the currents in M1 and M2 will increase continuously. That is to say, a resistor of this nature deteriorates temperature performance.

Despite the features of no resistance and simple structure of the circuit in [3], the output current of these two circuits is proportional to about $T^{0.4}$, so this is a pseudo constant current. The circuit in [4] is also an all-MOS implementation. Using MOS

transistors in the weak inversion region, a floating PTAT voltage source is built, and the current is proportional to about $T^{0.5}$. So this is also a pseudo constant current.

The temperature independence is achieved through the combination of a current source which is proportional to mobility and one which is inversely proportional to mobility by using a CMOS square root circuit in [5]. The final output current is derived as

$$I = \frac{1-\sqrt{m_3}}{1+2\sqrt{m_2}} \sqrt{m_1 m_4} \frac{\left(V_{DD} - 3|V_{TP}|\right)}{R} \tag{9}$$

Since $|V_{TP}|$ and R have negative and positive temperature coefficients respectively, they tend to cancel each other. But their temperature coefficients can not be designed and adjusted to cancel completely.

Deval et al. have proposed two bipolar current reference circuits [6, 7]. Although very different with our circuit, there are several similarities between them and our design, such as the adoption of ΔV_{BE} and V_{BE} to cancel each other, and the ratiometric property of the resistors. They achieved a temperature coefficient down to 120 ppm/ºC. But in their design, the resistor temperature dependency is ignored by assuming that it only induces second order effects, in contrast, it has been considered in our design.

The switched-capacitor technique has been used to realize constant current design [8]. The reference current of this method can be expressed as

$$I = \frac{CV_{REF}}{T_{CLK}} \tag{10}$$

Since the integrated capacitor has very low temperature coefficient, the reference current can achieve a very low temperature coefficient also. The demands for off-chip stable reference voltage and clock signal will limit its application range.

4. SIMULATION RESULTS

This circuit is simulated using 0.18 μm mixed-signal CMOS process with 1-V supply voltage. The PNP bipolar transistors used in the design are formed by P+/N well/P substrate vertical structure. N+ diffusion resistors without Silicide are adopted due to its minimum process variation among all the on-chip available resistors.

Figure 4 shows the dependence on power supply voltage of constant current at 25 ºC. It can be seen that this circuit can work properly when the supply voltage is larger than 1 -V, and the current keeps stable, achieving a voltage coefficient as low as 198 ppm/V.

The temperature performance of the output current of this circuit is also checked with the result shown in Figure 5. It can be seen that the temperature coefficient of the nominal 10 μA current is only 48 ppm/ºC in the temperature range from -25 ºC to 125 ºC.

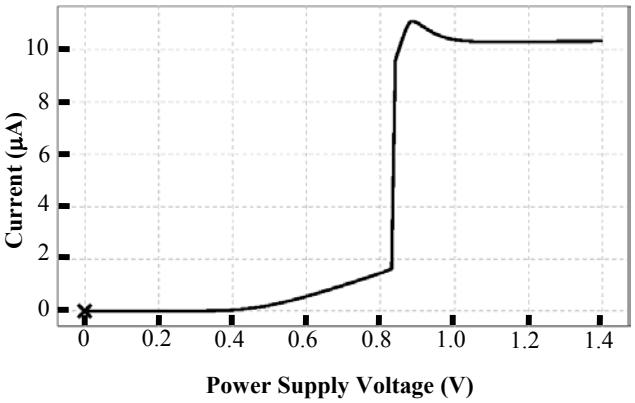


Figure 4. Simulated current vs. power supply voltage

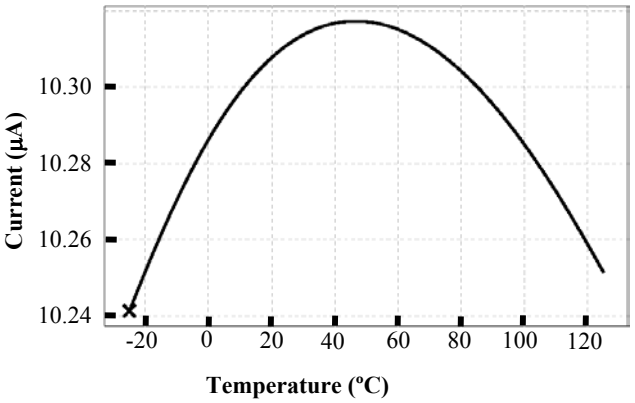


Figure 5. Simulated current vs. temperature

5. EXPERIMENTAL RESULTS

This circuit has been fabricated using a mixed-signal CMOS process. N+ diffusion resistors without Silicide adopted as the on-chip resistors, since it has the minimum process variation of about ±10%, which is ±15% or larger for other types of on-chip available resistors. No trimming options are used in the design, fabrication and test.

Figure 6 shows the microphotograph of the constant current reference circuit. Its area is about 560×330 μm. In order to reduce offset caused by fabrication, symmetry is ensured as much as possible in the layout. All differential pairs and current mirrors are placed common-centroid, and Q2 is designed as the multi-cells of Q1 with Q1 in the centre of it.

The performance of this circuit is characterized by measuring the current of an output buffer, which is 50 times of the reference current by current mirroring.

The measured current as a function of power supply voltage is shown in Figure 7. It can be concluded that this circuit works properly when the power supply voltage is higher than 1-V. the variation of the output current is less than 1 μA for the nominal output of 527 μA for 1-V and higher supply voltage, corresponding to a dependence on the power supply voltage as low as 190 ppm/V.

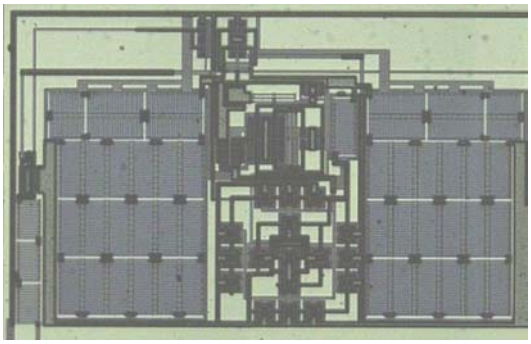


Figure 6. Microphotograph of the constant current reference circuit.

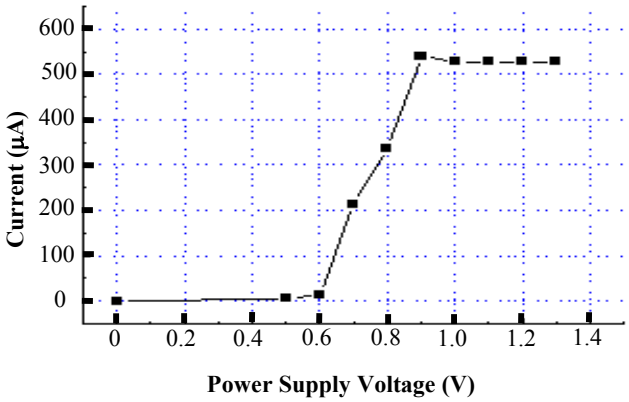


Figure 7. Measured current vs. power supply voltage

The measured current as a function of temperature is shown in Figure 8. Due to the limits of experimental devices, the performance of this circuit is verified from 0 ºC to 110 ºC. The achieved temperature coefficient is 50 ppm/ºC in the temperature range of (0 ºC, 110 ºC).

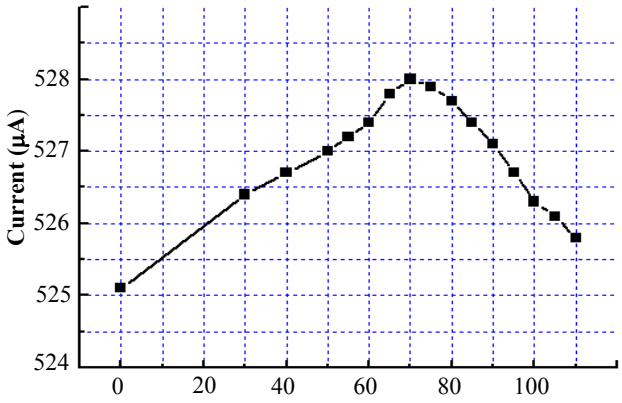


Figure 8. Measured current vs. temperature

6. ACKNOWLEDGMENTS

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7. REFERENCES

[1] Piero Malcovati, et al., "Curvature-Compensated BiCMOS Bandgap with 1-V Power Supply", IEEE Journal of Solid-State Circuits, vol. 36, No. 7, pp. 1076-1081, July 2001.

[2] Dean A. Badillo, "1.5V CMOS Current Reference with Extended Temperature Operating Range", IEEE Journal of Solid-State Circuits, vol. 33, No. 3, pp. 387-399, 1998.

[3] H. Oguey, D. Aebischer, "CMOS Current Reference without Resistance", IEEE J. of Solid-State Circuits, vol. 32, No. 7, pp. 1132-1135, July 1997.

[4] Willey M. Sansen, et al., "A CMOS Temperature-Compensated Current Reference", IEEE J. of Solid-State Circuits, vol. 23, No. 3, pp. 821-824, June 1988.

[5] C. H. Lee and H. J. Park, "All-CMOS temperature independent current reference," Electron. lett., vol. 32, pp. 1280-1281, July 1996.

[6] Y. Deval et al., "1-V Ratiometric temperature stable current reference", Proc. of ISCAS'1997, pp. 1984-1987, Hong Kong, June 1997

[7] Y. Deval et al., "Ratiometric temperature stable current reference", Electron. lett., vol. 29, pp. 1284-1285, July 1993.

[8] G. Torelli and A. D. LaPlaza, "Tracking switched-capacitor CMOS current reference", Circuits Devices Syst., vol. 145, no. 1, February IEE Proc.-1998.