Repeater and Current-sensing Hybrid Circuits for On-chip Interconnects *

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ABSTRACT

Designing interconnects is becoming an increasingly challenging problem with a few solutions. In this paper hybrid circuit based on the well known delay-optimal repeaters and the recently proposed differential current-sensing is presented. Comparison in terms of delay, power and area is drawn between various versions of the hybrid circuit with delay-optimal repeater insertion and differential current sensing in order to derive at the best possible solution. It is shown that driving 25% of the wire with repeaters and remaining with current-sensing is the best solution from delay standpoint (about 30% faster than delay-optimal repeaters). Not only do hybrid circuits consume less area, they are also a more acceptable solution from placement point of view due to fewer repeaters and a long segment of uninterrupted wire. Static power consumption inherited from differential current-sensing is the biggest drawback of the hybrid circuits.

Categories and Subject Descriptors

B.7.m [**Integrated Circuits**]: Miscellaneous—*On-chip Interconnects*

General Terms

Design

Keywords

Interconnect Circuits, Delay, Power, Area

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1. INTRODUCTION

With technology scaling, designers generally recognize that system performance is increasingly limited by the global interconnect delay. As the die size of CMOS integrated circuits continues to increase and feature sizes decrease, global interconnect becomes relatively slower, primarily due to the rapid increase in the electrical length [1, 4], thus creating a performance bottleneck. Additionally, power dissipated by future VLSI chips presents an ever increasing challenge for designers at all levels. The growing number of wires and the resources required to drive these wires increases the contribution of interconnects in the chip's total power dissipation.

To compound these issues, taller wires with reduced spacing increases the affects of coupling capacitance[9]. The technology scaling trends have also resulted in a significant increase in the inductance and the inductive coupling in interconnects [10]. Due to faster clock rate, the effect of inductance is going to be more pronounced in future technologies. Inductive and capacitive coupling make interconnect coupling noise significant [13]. Coupling noise between adjacent interconnects can cause disastrous effects on the logical functionality and long-term reliability of a VLSI circuit as well as complicate timing analysis.

Thus on-chip interconnects present a severe design challenge, not only in terms of delay but also in terms of power, resource utilization and signal integrity. Of the solutions proposed, the most popular is repeater insertion at regular intervals. Other solutions include differential signaling, current-sensing and boosters. This paper presents a hybrid of repeaters and current-sensing as a novel circuit technique to solve interconnect problems. The paper is organized as follows: Section 2 describes the repeater insertion method and discusses its advantages and shortcomings. Section 3 describes the current-sensing technique and discusses its benefits and pitfalls. Section 4 presents the hybrid solution and compares it with delay-optimal repeaters and current-sensing in terms of delay, power and area. Finally, conclusions and future work are discussed in Section 5.

2. REPEATERS

Repeater insertion at regular intervals and with uniform sizes makes the line delay linear with respect to the wire length. Bakoglu, in [1], shows that the delay of the repeater should be equal to the delay of the interconnect segment it drives in order to achieve an optimal solution. The repeater solution thus consists of determining the number and the size of buffers(or repeaters) to be inserted along the wire.

Effects such as the repeater gate capacitance and current drive capabilities, driver and repeater diffusion and overlap capacitances, the inverter's delay dependence on input edge rate and the wire inductance all impact the placement and sizing of the repeaters.

For the purpose of this study Bakoglu relations[1] shown in Equation 1 are used to determine the number and size of delay-optimal repeaters required to drive a line of given length.

$$k = \sqrt{\frac{0.4R_TC_T}{0.7R_oC_o}} \quad h = \sqrt{\frac{R_oC_T}{R_TC_o}} \tag{1}$$

where,
k is the number of repeaters in the repeater chain,
h is the size of each repeater (width of n-device),
R_T is the total resistance of the interconnect,
C_T is the total capacitance of the interconnect,
R_o is the output resistance of a minimum size inverter,
C_o is the input capacitance of a minimum size inverter.

Due to ease of design and their robust nature, repeaters have been the most popular solution to the interconnect challenge. However, the regular placement requirement constrains the global placement and routing problem[3].

With scaling the performance benefit of repeaters is getting limited. It has been shown that the number of repeaters per mm increase with technology scaling. Moreover, the number of repeaters in a clock cycle reduces [8]. Although the number of repeaters required on a wire grow linearly with its electrical length, the number of wires requiring repeaters is growing quadratically as technology scales. Additionally, the amount and percentage of power dissipated by interconnect circuits is increasing, with the increase in the number of repeaters required[12, 9]. Repeaters, being more than 150 times minimum size inverter in size, will be a source of leakage power. Thus, although repeaters do provide a robust, easy to implement and a relatively noise immune solution, performance limiting and power dissipation trends motivate the use of alternate circuit techniques.

3. CURRENT-SENSING

Current-sensing or current-mode determines the logic value transmitted on a wire based on the current through the wire. In current-sensing, the line is terminated by a short, which shunts the wire capacitance. This limits the voltage swing on the wire and saves dynamic power and time. Current-sensing techniques are very popular in memories and have also been proposed for on-chip interconnects and crossbars [7, 11, 2]. [5] compares differential current-sensing technique with optimal repeater insertion and discusses its advantages and disadvantages.

Both differential[5] and single-ended [11] current-sensing perform better than optimal repeater insertion in terms of delay. This study focuses on differential current-sensing because of its noise performance[6]. A differential current-sense amplifier proposed in [7] is used (Figure 1) to compare differential current-sensing and delay-optimal repeaters using a simulation setup shown in Figure 2 and implemented in a 0.18μ technology. Details discussing the working of current-sensing can be found in [7] and [5]. Since no partitioning was used in the current-sensing method, the delay increased quadratically with respect to wirelength and for very long wire lengths, current-sensing delay was greater than the optimal repeater delay. Current-sensing delay is also very sensitive to the driver size and the delay saturates as the driver size is increased.

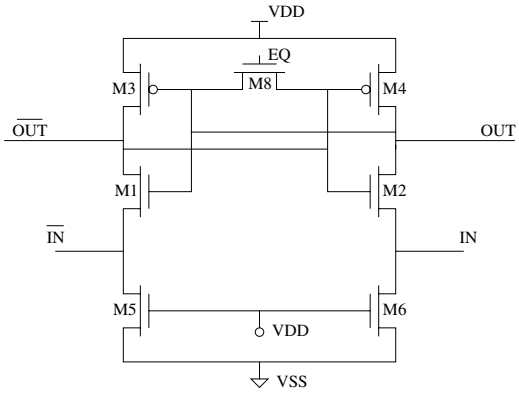

Figure 1: Modified Clamped Bit-Line Sense Amplifier(MCBLSA)

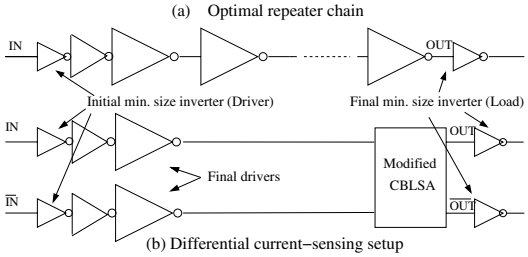

Figure 2: Setup for the simulation

Though faster than repeaters for certain line lengths, current-sensing is not power efficient. Static power dominates the total power dissipated in current-sensing making this technique not suitable for wires with small data activity. Moreover, the differential signaling method uses much more routing area than delay-optimal repeaters.

4. HYBRID CIRCUIT TECHNIQUE

As seen in Section 2 and Section 3 both repeaters and current-sensing have some advantages and disadvantages. To summarize, repeaters are easy to implement and noise immune but do not fare well in terms of delay and power as technology scales. Current-sensing on the other hand can provide a better solution if designing for speed. Current-sensing also performs better than repeaters as technology scales [8]. This motivates the idea of using a hybrid circuit which attempts to exploit the advantages of both techniques.

Figure 3 shows the proposed hybrid circuit solution. In this technique, a certain percentage of the wire is driven by repeaters and the remaining by differential current-sensing. In order to evaluate the performance of this technique, simulations were performed in a 0.18μ technology and comparisons were made against homogeneous delay-optimal repeaters and current-sensing systems. Three different hybrid transition points at 25, 50 and 75% of wire were considered.

4.1 Delay

Figure 4 show the delay estimates using HSPICE simula-

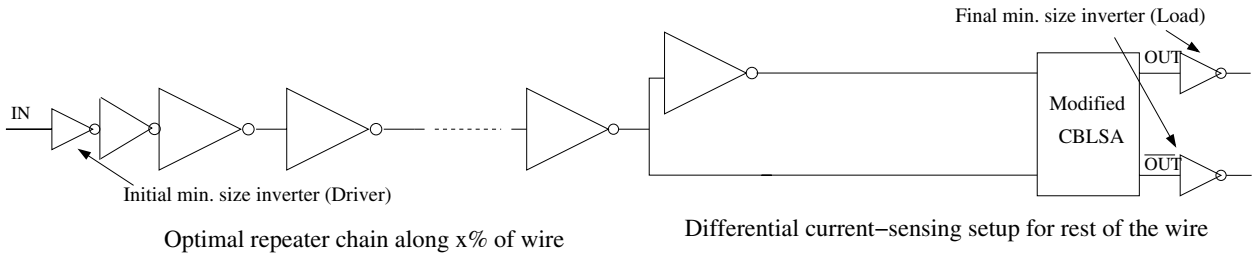

Figure 3: Hybrid of delay-optimal repeaters and differential current-sensing

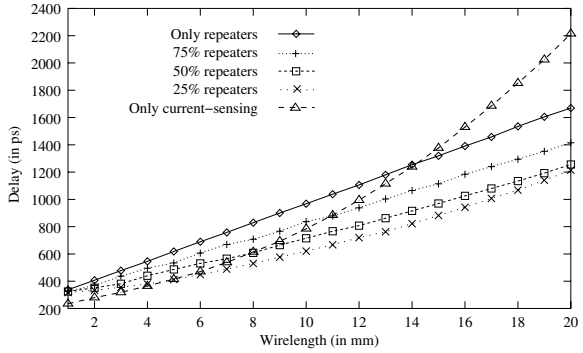

Figure 4: Delay comparison for various circuit techniques

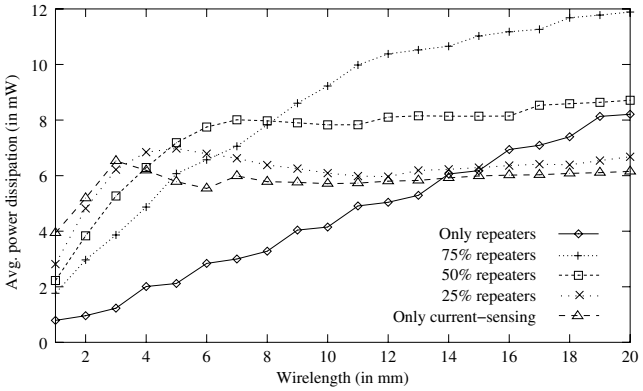

Figure 5: Power comparison for various circuit techniques

tions for various circuit techniques. As seen in the plot, as the percentage of wire driven by repeaters is increased, the delay behaves more like the repeater-only delay i.e. linear in relation with wirelength and closer to delay-optimal repeater delay. Moreover, 25% repeater hybrid provides the fastest solution for most of the wirelengths. The 25% hybrid is faster than delay-optimal repeaters by about 30% on an average.

4.2 Power

Figure 5 shows the average power dissipation comparison between various hybrids, delay-optimal repeaters and current-sensing. Power consumption trends for hybrid circuits are very similar to their delay trends. As seen in Figure 5, repeaters-only solution consumes the least power for most wirelengths. Higher power consumption in hybrids is mainly due to the static power consumption in current-sensing part of the circuit. These estimates are based on an activity factor assumption of 50% and the repeaters-only solution will be more attractive from a power stand point if the activity factor is lower.

However, these simulations were performed for a 0.18μ technology, which does not have significant leakage power. As will be shown in Section 4.3, the hybrids have lower amount of active area than repeaters, thus making them less leaky and hence more attractive with technology scaling. Moreover, static power is easier to manage and the power distribution system is not strained by it.

4.3 Area

Without layout level details it is difficult to accurately estimate the exact area taken by any circuit. However, to compare two circuits a fair estimation of the area of the circuit can be made by the cumulative channel area (Width of transistor × Length of transistor). Since the length of transistors used in all the circuits is the same, the cumulative width of the transistors will be a fair estimate. Figure 6 shows the cumulative width of the transistors for the circuit techniques under study. As expected, repeaters-only system consumes the most active area, mainly because of the large number of repeaters along the wire (Figure 7). These repeaters are also big in size (180 times minimum size inverter). Current-sensing, on the other hand has a single driver, hence it consumes least amount of active area. The hybrids are somewhere in between as the number of repeaters reduce with reduction in the fraction of wirelength driven by the repeaters (Figure 7). Although, driver size for current-sensing segment increases (Figure 8), but since there is just one driver this increase is very small as compared to putting as extra repeater. Note that the repeater size remains constant at 180 times minimum size inverter across all circuit techniques.

5. CONCLUSIONS

In this paper we presented a novel circuit technique as a candidate solution to the interconnect design problem. The hybrid circuit solution based on the well known delay-optimal repeater solution and the recently proposed differential current-sensing method provides a solution which is faster than delay-optimal repeaters across all wirelengths. It also consumes less active area than the delay-optimal repeaters. It was shown that driving 25% of the wire with repeaters and remaining with current-sensing is the best solution from delay standpoint. By having fewer repeaters

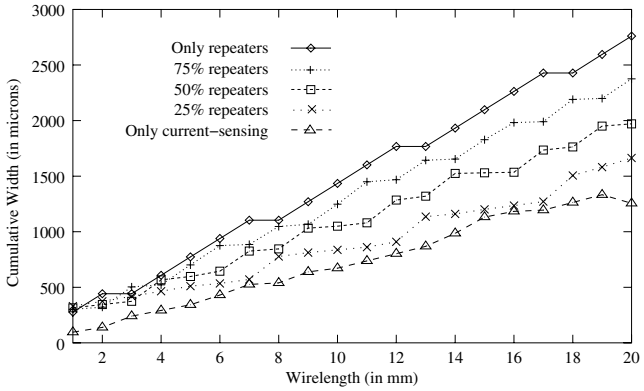

Figure 6: Cumulative width for various circuit techniques

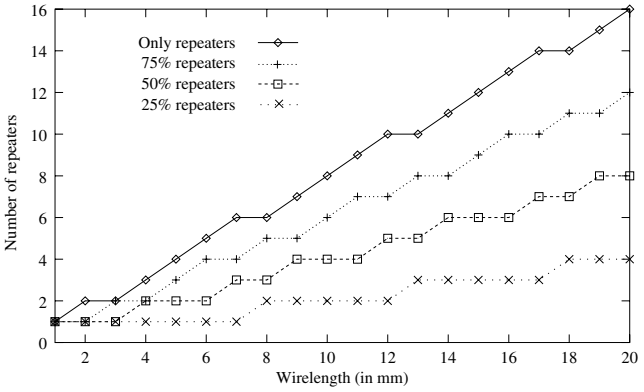

Figure 7: Number of repeaters for various circuit techniques

along the wire and having a long segment of uninterrupted wire, hybrid circuit solution will be a more acceptable in constrained placement scenarios.

The hybrid circuit solution, on the other hand, consumes more power than current-sensing and repeaters-only system for most wire lengths. Most of this power is static power in the current-sensing segment. Moreover, this hybrid circuit solution has similar pitfalls as differential current-sensing with regards to more routing area due to differential signaling, less noise immunity due to low swing signaling, an enable signal etc.. Although most of these limitations are less severe as compared to current-sensing, finding a solution to them will make the hybrid solution more applicable and attractive.

6. ACKNOWLEDGMENTS

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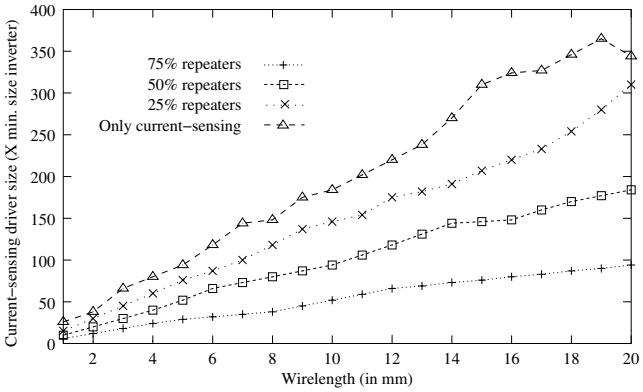

Figure 8: Current-sensing driver size for various circuit techniques

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