40 MHz 0.25 um CMOS Embedded 1T Bit-Line Decoupled DRAM FIFO for Mixed-Signal Applications

Michael I. Fuller, James P. Mabry*, John A. Hossack, Travis N. Blalock*
Dept. of Biomedical Engineering / *Dept. of Electrical and Computer Engineering
University of Virginia, Charlottesville, VA
mikefuller@virginia.edu, blalock@virginia.edu

ABSTRACT
An embedded 40 MHz FIFO buffer for use in mixed-signal information processing applications is presented. The buffer design uses a 1T DRAM topology for its unit memory cell component, a sense amplifier, and two circular shift registers for implementing refresh and read-write pointers. The sense amplifier uses bit-line decoupling to improve readout performance. Our particular application requires the storage of 800 samples of a received ultrasound signal that pass through 48 channels consisting of a preamplifier, a sample-and-hold, and an 8-bit ADC. Data is written into memory in parallel in a sequential, burst-mode fashion and read sequentially at leisure, with interspersed refresh of the memory cells. Layout and design issues concerning implementing memory in a standard 0.25 um process are discussed and simulation results are presented.

Categories and Subject Descriptors
B.7.1 **[Integrated Circuits]**: Types and Design Styles – *memory technologies*.

General Terms: Design.

Keywords: CMOS, FIFO, DRAM, embedded memory, ultrasound.

1. INTRODUCTION
The use of ultrasound in medical imaging applications offers many advantages over other imaging modalities, including real-time imaging capability, lack of ionizing radiation, high spatial resolution, good soft tissue contrast, portability, and relatively low cost. The past twenty years have seen remarkable technological development as ultrasound has progressed from providing one-dimensional M-mode images to the much more useful 2-D brightness mode (B-mode) and C-scan images. More recently, advances in integrated circuit technology have enabled the formation of real-time and 3-D images, along with a means of providing Doppler information for the measurement of blood flow.

GLSVLSI'03, April 28-29, 2003, Washington, DC, USA.

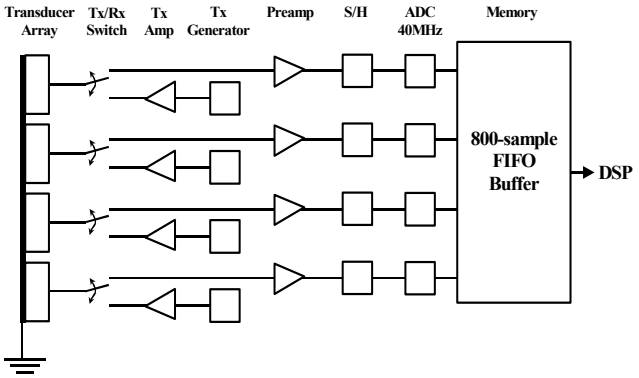

Figure 1. Typical phased array ultrasound system architecture. Modern systems typically contain 128 channels rather than the 4 shown here. Tx indicates transmit, Rx indicates receive.

Figure 1 shows the block diagram of a typical phased array ultrasound system. An ultrasound signal begins in each channel's transmit generator, which outputs a waveform varying with time and having a scaled amplitude and delay relative to that of adjacent channels. This waveform, whose amplitude is often on the order of 100 V, induces a mechanical vibration in the piezoelectric transducer. The total contribution of all active channels results in an ultrasound beam focused within the tissue of interest. Following transmission, the Tx/Rx switch is altered to connect the transducer elements to the receive circuitry so that echoes originating from the tissue can be detected. The received echoes are amplified by the preamplifiers, captured by the sample-and-holds, digitized by the analog to digital converters (ADCs), and stored in memory.

Once in memory, the data is passed to a digital signal processor (DSP), which performs the delay and summing operations necessary to form image lines. This entire process is repeated to form the remaining image lines. Typical line rates, limited by the round-trip travel time of the acoustic pulses, are less than 10 kHz. Though this amounts to more than adequate 2-D frame rates approaching 50 frames per second, 3-D real-time imaging requires much more processing power, often in the form of parallel receive beamformers that focus multiple image lines simultaneously.

Efforts have been made to integrate portions of receive and beamforming circuitry such as in [1] and [2], but neither of these attempts to integrate low-noise preamplifiers, sample-and-holds and analog to digital converters along with memory on a single ASIC. Fitting the processing power necessary for 3-D real-time ultrasound

imaging alongside associated receive circuitry on the same chip presents a number of interesting design challenges. One such challenge is providing a means for storing the received RF data until it can be processed, especially when constrained to a standard 0.25 µm process rather than a specialized DRAM process. Due to focusing requirements, image slice thickness, transmit and receive geometries, delay precision, and other system parameters, our application requires a frame size of 200 samples deep acquired at 40 MHz. For averaging and doppler capability, it is necessary to acquire four such frames in rapid succession, leading to a memory in the form of a FIFO buffer 800 samples deep. It is this memory design that is the focus of this paper.

2. FIFO BUFFER DESIGN DESCRIPTION

This memory design is partitioned into 48 channels, each containing 800 rows of 8 bits (see Figure 2). Data is written to all 48 memory channels at once in a sequential fashion, filling 800 rows in 800 clock cycles (20 us). The read operation is also sequential, but at a slower, intermittent rate. Subsequent write cycles only occur after all the data from the previous write cycle is read, so both the write and read control signals are handled by a single circular shift register.

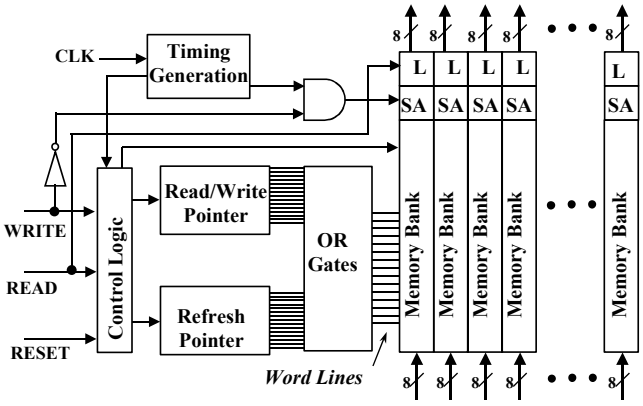

Figure 2. Block diagram of FIFO buffer

As with all dynamic memory topologies, refresh must be performed periodically, and this is accomplished with a second circular shift register active in the dead time between read operations. Each memory channel contains 8 folded bit-lines consisting of one sense amplifier, 800 1T DRAM cells, 2 dummy DRAM cells, four tri-state buffers, and a latch.

2.1 1T DRAM unit cell

The unit memory cell consists of a switching transistor and a drain and source connected device to act as a storage capacitor (see Figure 3). The source of the switching transistor is tied to a bit-line, and the gate to a word line.

Due to the infrequency of read operations relative to the clock frequency, it is possible to refresh the memory often enough to minimize the effects of charge leakage. Thus, the dominant effects on the minimum required storage capacitance are the bit- line capacitance and sensitivity of the sense amplifier. The sense amplifier (see Section 2.2) responds to changes in voltage on the bit-line after a read operation, which is proportional to the ratio of the storage capacitance to the bit-line capacitance (C_S / C_{BL}). A folded bit-line scheme [3] was chosen to cut the bit-line capacitance in half as well as exploit the complementary branches of the sense amplifier. One dummy memory cell is placed on each bit-line and its storage capacitance is equal to half that of the standard memory cell as is discussed in [3]. Once the bit-line capacitance was extracted from the layout, simulation showed that a minimum storage capacitance of 20 fF was necessary for reliable sensing by the sense amplifier.

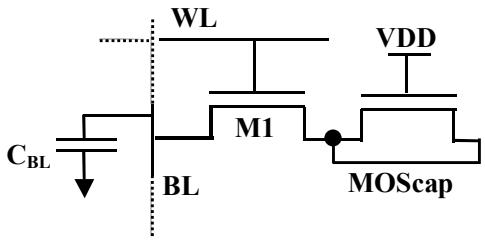

Figure 3. 1T dynamic memory cell

2.2 Sense Amplifier

Two problems arise when an attempt is made to read a 1T dynamic memory cell. First, the voltage variation induced on the bit-line by a read operation is only a few millivolts and therefore difficult to detect. Second, the read operation is destructive. Both problems are solved by the addition of a sense amplifier, which can quickly drive the bit-line high or low in response to these small voltages and allow refreshing of the memory cell.

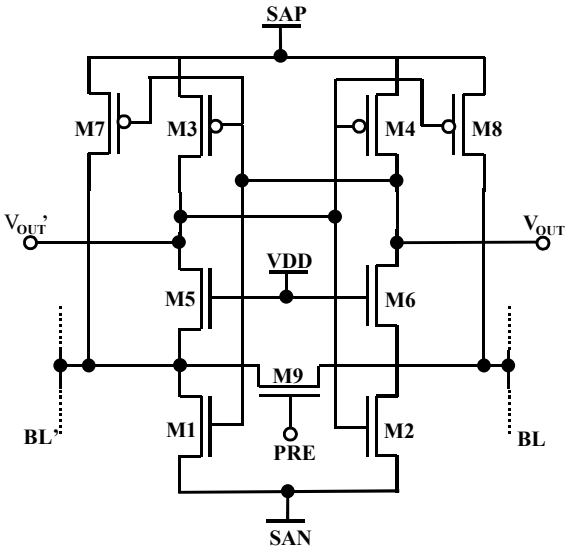

Figure 4. Modified cross-coupled sense amplifier with bit-line decoupling.

The sense amplifier topology used in this design (see Figure 4) is a modified version of the conventional sense amplifier discussed in [4]. M1 through M4 behave as a bistable flip-flop. During a sense operation, the drains of M1 and M2 (and correspondingly the complementary bit-lines) are both brought to half of V_{DD} through M9. A small increase in voltage on BL (in this case induced by the reading of a "1" from a memory cell) is sensed by the cross-coupled amplifier, causing the source of M2 to be driven high and the source of M1 to be driven low via positive feedback. The opposite is true for a small decrease in voltage on BL.

M5 and M6 serve as resistive decoupling devices between the output nodes and the highly capacitive bit-lines, allowing data read from the memory cell to be available faster. M7 and M8 were added to pull up the bit-lines more quickly to ensure that charge is restored to the memory cell by the end of the read operation. Note that the sense amplifier is active only during a read or refresh operation. It is turned off via devices connecting the sense amplifier to SAP and SAN, providing power savings capability.

2.3 Control Logic

The buffer control logic (see Figure 5) during normal operation is in one of three states: read, write, or refresh. In all three states, the control unit is responsible for activating a word line corresponding to one of the 800 rows, as well as controlling which half of the folded bit-line is active versus complementary.

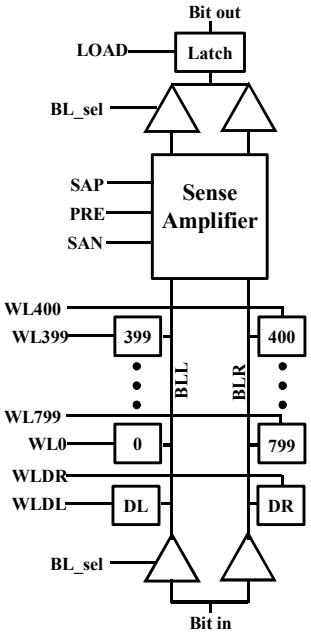

Figure 5. Block diagram of a folded bit-line and corresponding control signals.

During a write operation, the sense amplifier is inactive and the read/write pointer controls the sequential word line activation and bit-line selection. Once all data is written, control is then shared between the read pointer and the refresh pointer. Read and refresh operations are identical in all respects except loading the output of the sense amplifier into the latch during the read operation. Precise timing is crucial for ensuring that data is preserved during sensing and refreshed properly after sensing (see Section 4).

3. LAYOUT CONSIDERATIONS

The primary concern in the layout of the embedded FIFO buffer is area minimization. As discussed previously, channel width is restricted to no more than 50 µm, which sets the maximum width available for 8 folded bit-lines and their associated circuit components. Shrinking the memory cells to fit this dimension in a standard 0.25 um process is a major design constraint.

The largest component of the 1T DRAM cell is the storage capacitor, which, at 5.55 fF/um^2 (gate capacitance for the 0.25 µm process), a 20 fF capacitor requires 3.6 um^2. The unit memory cell (see Figure 6) is laid out in such a way that neighboring cells can overlap and share word lines, bit-lines, and ground and power buses (see Figure 7), creating a dense and easily scalable memory structure that fits well within the constrained channel width.

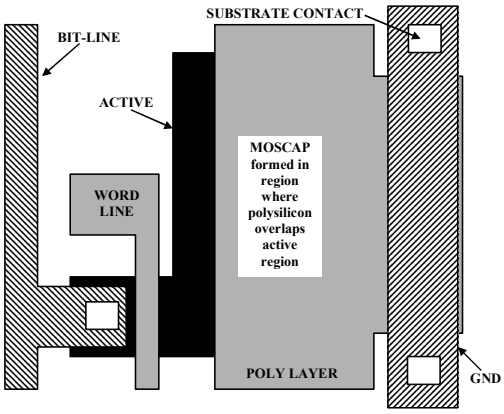

Figure 6. Layout of a unit memory cell. The contact to V_{DD} on the polysilicon layer of the MOScap is not shown.

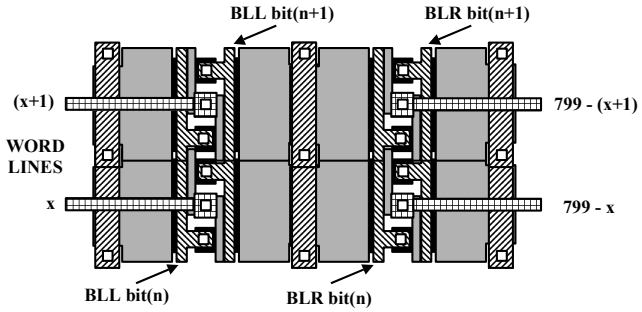

Figure 7. Layout of eight overlapping memory cells

A photomicrograph of the overall chip is shown in Figure 8. The 48-channel memory portion is the dense portion in the upper half, while the bottom portion contains the preamps, protection circuitry, sample-and-holds, and ADCs.

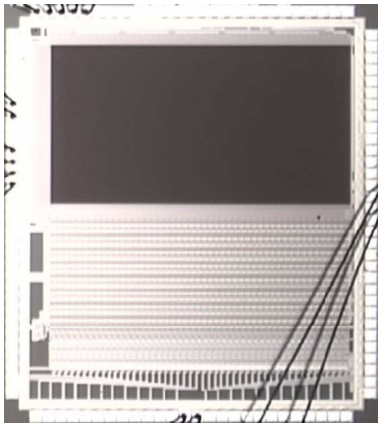

Figure 8. Photomicrograph of 48-channel prototype of an ultrasound system front-end.

4. SIMULATIONS

The results from simulating the 48 channel, 800 sample memory system are shown below. Due to the computational complexity of running lengthy simulations on a circuit of this size, a scaled-down equivalent model was simulated instead. The load characteristics of the word and control lines connected across 48 channels were characterized and replaced with capacitors so that only one channel was necessary in the simulations. The control unit was also characterized and substituted with an AHDL block.

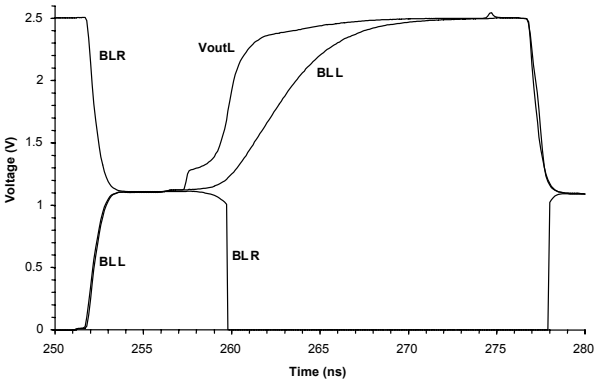

Figure 9. Waveform plot of sense amplifier outputs from the simulation of a READ/REFRESH operation.

Figures 9-10 show the sensing behavior and control signal timing, respectively, of the sense amplifier during a read or refresh operation. In this case, the memory cell is located on the left bit-line (BLL), and the right bit-line (BLR) serves as the complementary bit-line. The process begins as the precharge signal quickly brings BLL and BLR to the same potential. After the precharge control signal drops low, the word line is activated, giving the memory cell ample time to dump its charge on the bit-line before the sense amplifier is turned on with the SAN signal. The sense amplifier senses the small voltage difference between BLL and BLR and is able to drive its output (VoutL) high much more quickly than the highly capacitive BLL, due to the bit-line decoupling devices, M5 and M6. Once BLL is driven high, the word line is driven low before the sense amplifier is deactivated to ensure that the memory cell is fully refreshed.

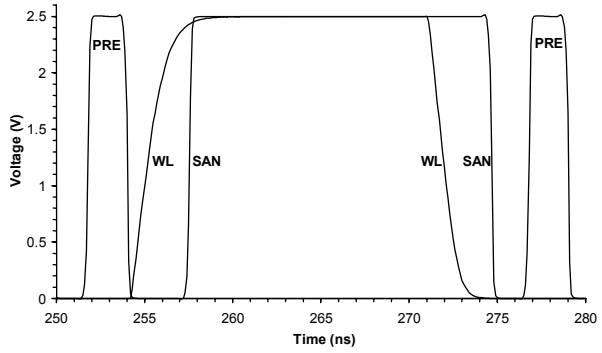

Figure 10. Waveform plot of precharge, word line and SAN control signals from simulation of READ/REFRESH operation.

Figure 11 shows the result of the writing and subsequent reading of six samples (010101) in a column of memory. The active memory cells are all on the left bit-line (BLL), and the first word line (WL<0>) and last word line (WL<5>) are shown to mark the beginning and end of each memory operation.

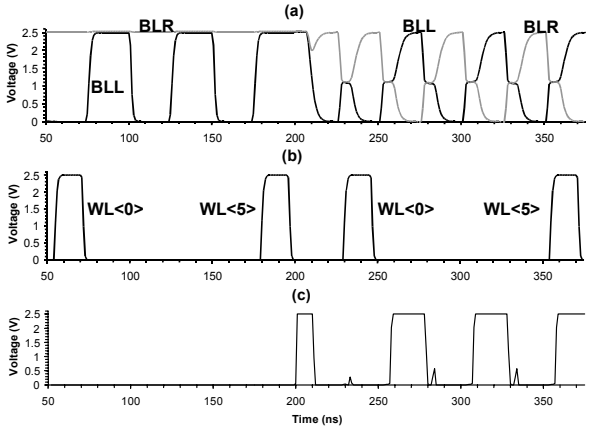

Figure 11. Simulation of 6-sample WRITE operation followed by 6-sample READ operation. (a) Right (BLR) and left (BLL) bit-lines, (b) word lines, and (c) output of the latch.

During WRITE, the sense amplifier is turned off and only BLL is active. One clock cycle is spent resetting the READ/WRITE pointer between the write and read operations. Once READ begins, OUT, which is taken at the output of the latch, follows the decoupled output of the sense amplifier. A refresh operation proceeds similarly to a read operation except the memory contents are never loaded into the latch.

5. CONCLUSIONS

An embedded FIFO buffer implemented with 1T DRAM memory cells in a standard 0.25 μm process was presented and shown to work in simulation. Through space-efficient layout strategies in the unit memory cell, the channel width of the memory was able to meet the channel width constraint of the 8-bit ADC. Total power consumption during a read or refresh operation was estimated to be 43 mW.

6. ACKNOWLEDGMENTS

Our thanks to William F. Walker and John A. Hossack for their contributions.

7. REFERENCES

[1] M. Anderson, G.E. Trahey, et al. "A Handle-Mounted Multiplexing Preamplifier for Synthetic Receive Aperture Imaging." 19th Annual Internat. Symp. on Ultrasonic Imaging and Tissue Characterization. Arlington, VA. 1994.

[2] B.G. Tomov, J.A. Jensen. "A new architecture for a single-chip multi-channel beamformer based on a standard FPGA." Proceedings IEEE Ultrasonics Symposium. pp. 1529-1533. Atlanta, GA. 2001.

[3] J. M. Rabaey. "Designing memory and array structures." Digital Integrated Circuits--A Design Perspective. Section 10. pp. 551-628. Prentice Hall, Inc. 1996.

[4] T. N. Blalock, R. C. Jaeger. A high-speed sensing scheme for 1T dynamic RAM's utilizing the clamped bit-line sense amplifier. IEEE Journal of Solid-State Circuits. Vol. 27. No. 4. April 1992.