A New Crosstalk Noise Model for DOMINO Logic Circuits

Seung Hoon Choi
Dept. of ECE, Purdue University
W. Lafayette, IN 47907, USA
choi5@ecn.purdue.edu

Kaushik Roy
Dept. of ECE, Purdue University
W. Lafayette, IN 47907, USA
kaushik@ecn.purdue.edu

Abstract

A new crosstalk noise model is proposed for DOMINO logic gates. Our noise model takes the effect of keeper into account and provides more accurate noise measure.

1 Introduction

With the scaling of technology into the nano-meter regime, interconnect delay may limit the performance improvement of a digital circuit [1]. As a practical solution to the problem, the aspect ratio (defined as the interconnect wire thickness divided by the width) of the interconnect is increased [1]. This, however, increases the coupling capacitance between neighboring wires, which makes a circuit more prone to failures due to crosstalk noise.

Crosstalk noise can affect a circuit in two ways – causes glitches and/or changes signal delays. Temporal properties of a circuit can be affected when capacitvely coupled neighboring signals experience simultaneous switching [2]. A functional failure is possible when an induced noise glitch is propagated and wrongly evaluated at the latch or primary output. Crosstalk-induced glitches can cause severe problems for high-speed dynamic circuits for which noise immunity is low. In this paper, we focus on the crosstalk-induced functional failure.

In DOMINO gates, noise immunity is sacrificed for high performance. The DC noise margin of DOMINO gates is equal to the threshold voltage of pull-down transistors. Unlike static CMOS gates, the charge lost from dynamic node due to noise cannot be restored in DOMINO gates. This makes DOMINO gates more vulnerable to noise than static CMOS gates. A keeper is used to restore any loss of charge from the dynamic. In this paper, we propose a new analytical noise model for DOMINO gates where the effect of keeper is taken into account. We show that our DOMINO noise model produces less pessimistic noise measure than other noise models.

2 DOMINO Noise Model

Figure 1 describes the noise model for DOMINO gates. We denote the signal of interest as *victim* (input of PDN) and the signal affecting the victim as *aggressor*. During the evaluation period, input signal either stays at 'low' or switches from 'low to high'. The victim is vulnerable to crosstalk noise when it stays at 'low'. Due to an aggressor switching, noise glitch is induced on a victim net through capacitive coupling. The number of aggressors coupled to a victim net can be more than one depending on the layout. However, this does not affect our model since we assume that the induced noise waveform at the input is readily available via transistor-level simulation or analytical model. The failure due to crosstalk noise at input for DOMINO gate is defined such that *failure occurs in a DOMINO gate when the voltage deviation at dynamic node exceeds DC noise margin of the following inverter*[1].

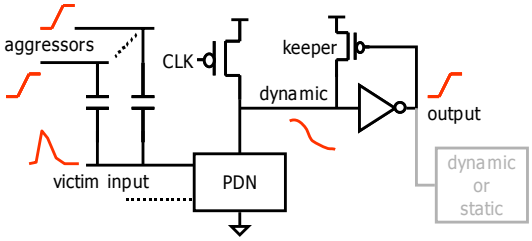

Figure 1. Crosstalk noise model for DOMINO gates

2.1 DOMINO noise margin

In order to obtain an analytical solution for noise margin for DOMINO gates, let us consider the current model for the PDN NMOS transistor. The transistors in deep-submicron technology experience short-channel effects [4]. As a result, there exists a linear relationship between drain-to-source current and gate voltage.

Therefore, the current flowing from the dynamic node in Figure 1 can be expressed as

$$i_d(t) = g_m \times (v_{in}(t) - V_{th}) \tag{1}$$

where i_d is the current at dynamic node, v_{in} is the input noise voltage, V_{th} is the threshold voltage of PDN and g_m (di_{ds}/dv_{gs}) is the transconductance of PDN. We calculate g_m considering V_{ds}=V_{dd}. The voltage deviation at the dynamic node is determined by ground capacitance at the node and the amount of charge lost due to noise activity. Therefore, voltage deviation, V_d, at dynamic node can be obtained by

$$Q_d = \int_T i_d(t)dt = \int_T g_m \times (v_{in}(t) - V_{th})dt$$
$$V_d = \frac{Q_d}{C_d} = \frac{\int_T g_m \times (v_{in}(t) - V_{th})dt}{C_d} \tag{2}$$

where Q_d is the amount of charge lost from the dynamic node and C_d is the ground capacitance at the node including all the parasitic and wire capacitances. Integration is performed for the time period T, for which the input noise $v_{in}(t)$ is larger than V_{th}. By comparing V_d with the DC noise margin of the inverter, NM_{inv}, we determine if a gate will

[1] This concept of failure is similar to the one proposed in [3]

have a failure. The DC noise margin is obtained from voltage transfer characteristic at unity gain point.

Depending on the voltage change at the dynamic node, current flows through the keeper supplying a certain amount of charge to the dynamic node. Therefore, the charge loss, Q_{d_new}, from the dynamic node is modified by

$$Q_{d\_new} = Q_d - Q_{keep}$$

where Q_{keep} is the amount of charge supplied by keeper. The voltage deviation at dynamic node can be rewritten as

$$V_d = \frac{Q_{d\_new}}{C_d} = \frac{\int_T g_m \times (v_{in}(t) - V_{th})dt - Q_{keep}}{C_d} \qquad (3)$$

Q_{keep} can be obtained by integrating the current flowing through keeper with respect to time. The transient behavior of current flowing through the keeper is modeled as a triangular waveform. The peak current (peak of the triangular waveform), I_{k_max}, is obtained assuming the voltage deviation at the dynamic node equal to NM_{inv} (the condition for functional failure). It is also assumed that the gate of the keeper is grounded to simplify the estimation of keeper current. However, this does not introduce much error considering the fact that the gate voltage of the keeper remains close to zero due to the high gain of the inverter until the voltage deviation at the dynamic node exceeds the trip point of the inverter. The duration of keeper current is equal to T, for which the input noise is greater than V_{th} of PDN NMOS. The charge supplied by the keeper is obtained by integrating the transient current during T. The actual duration of the keeper current waveform is longer than T because of the feedback mechanism. This ensures that we do not underestimate the effect of crosstalk noise.

Finally, incorporating keeper charge into eq.(3), we get;

$$V_d = \frac{\int_T g_m \cdot (v_{in}(t) - V_{th})dt - \left|\frac{1}{2} \cdot T \cdot I_{k\_max}\right|}{C_d} \qquad (4)$$

According to the definition of the failure, V_d has to be larger than the DC noise margin of the inverter. Therefore, equating V_d to NM_{inv} in eq.(4) we get

$$\int_T (v_{in}(t) - V_{th})dt = \frac{NM_{inv} \cdot C_d + \left|\frac{1}{2} \cdot T \cdot I_{k\_max}\right|}{g_m}$$

We define the DOMINO noise margin as

$$DNM_{DOMINO} = \frac{NM_{inv} \cdot C_d + \left|\frac{1}{2} \cdot T \cdot I_{k\_max}\right|}{g_m} \qquad (5)$$

DNM_{DOMINO} has the unit of volt.sec and is compared with time-integration of input noise to verify functional failure. Note that the keeper effect does not contribute to any extra computational cost since T is obtained from the already available input noise pulse and I_{k_max} can also be pre-characterized. Also note that neglecting the keeper effect, DOMINO noise margin reduces to dynamic noise margin proposed in [3].

Table 1 Number of violations for different noise models

PDN width (um)	1.8	3.6	5.4	7.2	9.0	10.8
DC NM	4500	4500	4500	4500	4500	4500
Dynamic NM	3067	3168	3213	3230	3247	3258
DOMINO NM	2829	2949	2990	3011	3017	3024
True violation	2316	2387	2409	2412	2410	2410

3 Comparison of various noise models

We verified our noise model for DOMINO gates with 0.18um technology and with the supply voltage equal to 1.8V. DOMINO inverter is used for the experiments. To account for the possible combinations of input noise, 4500 different noise pulses were generated. These noise pulses had triangular shapes with different heights and widths.

DOMINO gates with different sizes of PDN NMOS are verified. Results are summarized in Table 1. Each cell represents the number of violations identified by using different noise models. DC NM compares the peak of the noise with V_{th} of PDN. Dynamic NM incorporates the model proposed in [3]. DOMINO noise margin given by eq.(5) is used for DOMINO noise model. "True violation" shown on the last row of the table represents the number of input noise that caused a complete switching of a signal at the output of a DOMINO gate. By comparing the number of violations identified by different noise models with the number of "true violation", the conservatism of the model can be distinguished. A complete switching of a signal at the output does not necessarily mean the functional failure of a circuit. It depends on the sensitization condition of the path through which the noise is propagated to the primary output. However we restrict our attention to local violation of a logic value.

It is observed from the table that by using DOMINO noise model we can reduce the conservatism compared to DC NM and DNM analysis. It is also observed that all true violations are covered by these three different noise models.

4 Conclusions

We proposed a DOMINO noise model and a DOMINO noise margin to verify crosstalk-induced functional failures in DOMINO logic circuits. Our noise model provides less pessimistic results compared to DC noise analysis and dynamic noise analysis.

References

[1] M. Bohr, "Interconnect scaling – the real limiter to high performance ULSI," *International Electronic Device meeting*, pp.241-244, 1995.

[2] R. Arunachalam et al, "TACO: Timing analysis with coupling," *Proc. of DAC*, pp.266-269, 2000.

[3] S. H. Choi et al, , Dynamic Noise Analysis with Capacitive and Inductive Coupling," *Proc. of ASP-DAC*, pp.65-70, 2002.

[4] Y. Taur and T. H. Ning, "Fundamentals of Modern VLSI Devices," Cambridge University Press, 1998.