PANEL
Libraries: Lifejacket or Straitjacket

Chair: Carl Sechen, University of Washington
Organizers: Chandu Visweswariah & Gerard Mas
Panelists: Barbara Chappel, Intel Corp., Jim Hogan, Artisan Components, Inc.,
Andrew Moore, TSMC, Tadahiko Nakamura, STARC, Gregory Northrop, IBM Corp.,
Anjaneya Thakar, Synopsys, Inc.

Discussion topic:
The end of libraries as we know them

With the advent of nanotechnologies, the so-called “productivity gap” between the number of transistors we can design and the hundreds of millions we can physically place on a chip is growing. Not only is the complexity increasing in the macrocosm of SoCs and system-level design, it is also exploding at the microcosmic level of wires, transistors and shapes. Time-to-market, first-time-right and high-performance pressures worsen the situation.

Over the last 3 decades, standard cell libraries have been an obvious and useful method for taming this complexity. Library abstractions have contributed to productive design, containment of the data explosion problem, and simplification of methodology, design and tools.

While the library paradigm has served us extremely well, thus far, there may be several reasons why this ride will not continue in the future. Three trends are conspiring to necessitate a paradigm shift:

- Performance requirements,
- Low power, and
- System-on-a-chip integration.

To maximize performance, designers are forced to use transistor-level options that were hitherto only available to custom designers. The advent of transistor-level options such as multiple threshold voltage choices, multiple oxide thickness and transistor sizes (including choices of beta ratios and taper ratios) is causing the sample space for ASIC library creation to explode, and the very notion of a library to be questioned.

To minimize the power without sacrificing the performance, all possible design options have to be used i.e. clock gating, transistor sizing, sleep modes and sleep transistors, leakage-reduction transistor topologies, multiple voltage islands and multiple clock domains. The library ramifications represent a sharp divergence from present practice and call for more parameterized representations of our library cells.

Successful SoCs imply integration of diverse functions on a single chip. They include mixed analog/digital circuits, high-voltage I/O cells, extremely dense embedded memories including 6T-SRAMs and multi-foundry library offerings. Economic constraints drive different design styles and heterogeneous functions to be integrated within a single silicon die, often developed by different teams. Signal processing, radio signal, global control, video and audio functions (and all the methodology implications thereof) have to coexist within the same chip. Will each of these domains have their own library, how will all these libraries coexist and what will be the rules for mixing and matching?

The crunch so far has been addressed by library providers allocating more resources and more efforts in developing and characterizing libraries. At the same time, the gap between ASIC performance and custom-designed circuits continues to grow. This trend is clearly unsustainable. So, what part will libraries play in a future design methodology aimed at a system-on-chip with ultimate performance and low power goals?

The distinguished panel of industrial and academic experts will explore the issue along with other questions such as: Can sub-micron technologies continue to grow library size? Will we soon have libraries containing 10,000 cells? Will tools and characterization methods cope? Will design styles and methodologies be profoundly impacted? Is it the end of libraries as we know them?

Position statement: Lifejacket team

“Automation will play an ever-increasing role in library construction, particularly in physical design. In addition to the device scaling crisis, there is a lithography crisis on the horizon. Cells will be slightly less compact but more regular as to be design automation adapted. This will further encourage libraries to be organized into classes of cells, with much in common in both design and analysis within a class. The net result is that libraries will neither go away nor explode, but will rather cover a different slice of the design space.” said Greg Northrop
“New market requirements may cause library offers to explode. This phenomenon could only be reduced with a significant amount of investments as the process would require various techniques as well as expertise. One company may not be able to deal with the issue on its own. It is a challenge that needs companies’ common effort as per the Japan model.” said Tadahiko Nakamura.

“Nanotechnology is here today and has an important, long-lived future - and so do standard cell libraries. Libraries have become more - not less - important due to increasing circuit design complexity as CMOS is aggressively scaled. Standard libraries are an important tool for both evaluating technology trade-offs and for providing effective, reliable design solutions for chip-design teams.” said Barbara Chappell.

**Position statement: Straitjacket team**

“Given the broad portfolio of semiconductor processes, and the large range of device categories within each process, how can users not be confused with the large library offers?” said Andrew Moore.

As things stand today, libraries are a real “straitjacket” for designers. It restricts and constrains designers’ creativity and limits design optimization. However, this problem also represents an opportunity for EDA tools community to meet this challenge and turn libraries into a “lifejacket”. This implies that, in the future, library developments will be highly efficient and flexible allowing design specific libraries that might contain large number of “customized” cells within the same silicon die” Said Anjaneya Thakar.