PANEL
COT - Customer Owned Trouble

Chair: Bob Dahlberg, Reshape Inc.

Abstract
Increasingly, system houses are attracted to the customer-owned tooling (COT) model to gain more control of their schedules and costs. COT project risk and cost are high, often seeming more like customer owned “trouble,” so the design team needs to be expertly prepared. The pathways to implement a COT design include (a) Manage the sourcing (internal or third party resources) of individual supply chain and cost reduction functions; (b) Use an integrated design-to-parts service; or (c) A hybrid of these two extremes. This panel will consider the pros and cons for each approach.

Position Statements

Gina Gloski
ESilicon Corporation
The COT movement is here to stay. Can it spell Trouble? Absolutely. First, let’s examine the drivers of COT. The increasing complexity of today’s chip designs has forced specialization in the design & manufacturing supply chain – resulting in the worldwide “dis-integration” of that supply chain. This trend creates the “Complexity Paradox.” That is, just when advanced technology is forcing the unification of design and manufacturing (requiring tight communication), the supply chain is dis-integrating (resulting in poor communication). Someone needs to put the supply chain back together, and make it work in a tightly integrated fashion.

Who will be the “general contractor” for IC design and manufacturing? The customer can try. This is somewhat like trying to build your own house after reading a book and visiting Home Depot. This is the COT model, and this is where the Trouble starts. Successful tapeout and volume delivery of a 0.18 micron design will take at least nine full-time equivalent (FTE) headcount over a dozen specialties. At 0.13 micron, the numbers grow to 16 FTE’s across two-dozen specialties, not to mention the infrastructure requirements – all of this being outside the core competency of the typical customer.

Clearly, a general contractor is needed. Companies that can “re-integrate” the specialized, worldwide supply chain reliably and predictably will take the Trouble out of COT.

Aurangzeb Khan
Cadence Design Systems, Inc.
A COT design approach can provide greater flexibility in wafer supply, broader access to intellectual property and reduced overall cost. To gain these advantages, customers need to manage the increased risk in forming and operating an effective COT supply chain.

The COT challenge is compounded by the exponential increase in design complexity for nanometer-class system-on-chip (SoC) designs. Project scale, design content and the technical requirements for successful design are all going up concurrently. In addition, the business climate has also become progressively more challenging. Business success increasingly requires first-to-market delivery of innovative and competitive new products with rapid ramp to volume production. The manufacturing life of individual designs is trending downward, from many years to (typically) about one year. The cost of being late is high: ~$800K in re-manufacturing costs and ~$100M - $500M in opportunity costs.

To successfully implement a COT model, companies must aggregate their capabilities to: a) address the architectural and functional design requirements of the IC; b) perform silicon engineering to take the design from RTL through GDS2, creating a silicon design that meets functional and electrical design requirements; c) develop methodology automation to make an efficient process for platform and derivative designs; d) create high-value IP and integrate IP from myriad suppliers; e) package, test and qualify parts; and finally, f) manage the inventory and logistics of volume production.

Building resilient and strong supply chain partnerships is the best way to approach this challenge. By partnering with companies that specialize in specific steps of the product delivery value chain, system and IC designers can benefit from best-in-class product delivery capability and economies of scale, ensuring first-to-market and first-to-volume design delivery. All parties become focused and aligned by the primary objective of delivering system/IC products. Partnering within such a supply chain enables companies to focus on their core competency and competitive differentiation, continuously driving innovation and product excellence.
Kaushik Patel
Azenda Network Devices

It’s not unusual for companies to have major trouble with the traditional COT model. Project and even enterprise failure has its roots in the "hands-off" netlist handoff flow and then blindly relies on a third party to take a design through the entire physical design process including timing closure. For COT designs, with each 0.13u tapeout costing more than $2 million (physical design+masks+fab), there has to be a major emphasis on making sure that each tapeout yields production quality product. The costs associated with multiple all layer turns can no longer be managed within the funding constraints of a start-up.

To avoid the trouble scenario, we have developed a COT model where we define the overall chip pinout, macro floorplan including external IP and timing constraints. We rely on an outsourced model for the actual physical design including all the checks necessary to ensure production quality first tapeout. Most important is our in-house team that has an in-depth knowledge of the physical design process, timing closure and signal integrity analysis to ensure volume on first silicon. This approach has proved to be very successful for our first products.

Paul Ruddy
Cisco Systems, Inc.

COT is an integral component of our ASIC strategy. As a strategic capability, COT provides many benefits other than just lowest cost. Among these are visibility and control over the entire development process and the ability to optimize a design for specific Cisco requirements. The benefits of COT can only be fully realized with in-house resources for both development and production.

We have in-house capabilities for all aspects of COT, including physical design, IP, manufacturing development and manufacturing operations. In addition to enabling some of the key benefits of COT, the in-house capabilities are also leveraged by non-COT engagements – both ASIC and standard product. In-depth knowledge of technology, cost structures and production practices help Cisco to be more effective in all of our silicon engagements.

We believe that our COT efforts should utilize the capabilities available from our design services, IP and manufacturing partners. We maintain a lean execution model, and utilize outsourcing to complement what we do internally. With the COT "ecosystem" that exists today, there are many areas where a small internal staff can leverage the much greater resources of our partners. However, to have the "best of both worlds" (in-house and outsourced) our internal COT capabilities need to be above a critical mass and be utilized as an integral part of our strategy.

It is important to focus on the level you invest in for COT as part of an overall ASIC strategy. Those investments, whether in technology, IP or execution resources, need to be carefully targeted to maintain a balanced role of COT for a system house like Cisco.

Naveed Sherwani
Intel Corporation

The key attractive feature of traditional ASIC model is that a single vendor is responsible for the ASIC. The high per piece prices is driving customers towards the COT model. Unfortunately, they are finding out that cost of design teams, latest design tools, investment required to update the methodology, and business development costs (to engage with dozens of providers) far outweigh any potential benefits. Detailed studies have shown that unless you are doing more than 15-20 chips per year it is difficult to amortize the COT costs.

Risks in COT are also significant, and abound. The major risk is posed by scaling challenges. In 0.18 micron, we had to account for RC, while signal and power integrity became additional key issues at 0.13 micron. As we move to 90 nm, Soft Error Rates (SER), leakage and other issues pose significant challenges.

COT teams, typically in-house “general contractors” that are doing less than 15-20 designs per year are very likely to face trouble with a capital T. This is simply because the small number of designs they complete do not allow them to gain the experience needed to successfully complete the chips, especially in facing the up coming scaling challenges. The famous semiconductor learning curve effect equally applies to product and test engineering.

As a result, we do not believe that it is possible to make a “general contractor” model work for COT, unless a contractor has significant volume to cultivate the requisite experience in design, product and test engineering.

Ronnie Vasishta
LSI Logic Corporation

Deep sub micron challenges have become a significant hurdle to getting to a successful design tape out. These challenges extend from silicon transistor and interconnect modeling, design verification and simulation to high reliability and cost effective production and test. The industry point EDA tools still lag in being able to provide a complete solution to the design challenge.

The inability to predict the design throughput time or even whether the design will meet specifications at the end of the cycle means that many are unable to engage in the leading edge technology.

For complex SOC design, the best solution is to work with a complete solution provider or IDM who is responsible for every link in the chain and has honed a design methodology that uses a combination of internal and external tools. This solution provider, by completing many designs per year, is able to provide economies of scale. The foundries are now moving to work more closely with the traditional IDMs as the foundries see the IDMs capable of producing more reduced risk tape outs at the 130nm technologies and beyond.