Panel

Reshaping EDA for Power

Chair: Jam Rabaey, University of California at Berkeley
Organizers: Dennis Sylvester, University of Michigan & David Blaauw, University of Michigan
Panelists: Kerry Bernstein, IBM, Jerry Frenkil, Sequence Design Inc., Mark Horowitz, Stanford University, Wolfgang Nebel, Oldenburg University, Takayasu Sakurai, University of Tokyo, Andrew Yang, Apache Design Solutions

Abstract
Today’s rising power densities have been widely cited as the foremost challenge to continued CMOS scaling. In fact, the current power crisis is reminiscent of the final days of previous technologies, such as the once popular bipolar and NMOS technologies and even vacuum tubes. How CMOS technology will respond to the current power challenge to extend CMOS scaling to sub-90nm technology is an important question for designer and CAD tool developers alike. With aggressive scaling a number of new challenges have arisen, such as leakage control, heat removal and power supply distribution, that need to be addressed using new design techniques in conjunction with new CAD solutions.

This panel brings together experts in circuit design and CAD tool development to discuss the current status of low-power design and provide opinions on what new EDA capabilities are most important in the power-constrained design era. For instance, how will power be distributed in a robust fashion in sub-90nm ICs, and what are the critical EDA analysis and optimization capabilities? What are the best techniques for leakage reduction, not only in standby modes, but also in the active mode? And how far will voltage scaling take us in attacking the dynamic power consumption issue? What will a power-centric design flow look like and how will it change the way we design ICs? The objective of the panel is to explore these issues and formulate a list of critical issues that need to be addressed by the EDA community to enable successful scaling of CMOS into the sub-90nm era.