Invited Talk

Design Technology Challenges for System and Chip Level Designs in Very Deep Submicron Technologies

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Abstract
With very deep submicron process technologies, previously ignorable phenomena now have great impact on the robustness of IC designs. At the same time, the smaller feature sizes also enable an exponential increase in number of functions (or transistor count) available on chip. Complexity in process technology and design is widening the Design Technology gap, which, if not addressed properly, will threaten the continuation of process scaling and the industry’s ability to benefit from it. The complexity of process and design technology, its impact on new designs, new products development and future solutions will be discussed in this presentation.

Biography
Mr. James Lin has been working in the semiconductor industry for more than 22 years. He has been working in various areas ranging from circuit and logic designs to test and product engineering. Currently, James is the Vice President of Technology Infrastructure Group of National Semiconductor Corporation, Santa Clara, California, where he is responsible for the research and development activities in Design Tools integration and development, Design flow, Design libraries and methodology.

Mr. Lin received MSEE from the Pennsylvania State University and is a member of IEEE and Chinese American Semiconductor Professional Association.

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