Techical Program Co-Chairs’ Message

On behalf of the Technical Program Committee of ASP-DAC 2003, we would like to welcome all of you to the conference held from January 21 through 24, 2003 in Kitakyushu City, Japan.

The Technical Program Committee of the conference is organized by 104 professionals on EDA, LSI design, and embedded system design with 9 Topic Groups. Each Topic Group selected high quality papers on System Level Design Methodology for SoC (System LSI), Embedded and Real-Time Systems and Software, Synthesis and Verification in RT and Logic Level Design, Optimization and Verification in Circuit and Physical Design, Test Technology and Design for Testability, Analog and RF Circuit Design, Design for Manufacturability (TCAD), Reconfigurable Systems and Fully Programmable Systems, and Leading Edge Design Examples, respectively.

We had 235 paper submissions for regular sessions from 22 countries/regions in Asia, North America, Europe, and Africa. Among these papers, 79 and 40 papers were accepted as regular and short papers, respectively. Accordingly, the acceptance ratio is 50.6%. These papers will be presented in 27 technical sessions in four parallel tracks. Three papers among all accepted papers were awarded as Best Papers by the Best Paper Selection Sub-Committee in the Technical Program Committee.

Beside these regular technical sessions, we prepare three Keynote Address speeches, three Panel Discussions, four Invites Talks, and one Embedded Tutorial. Keynote Address I is titled "Designing Robust Systems with Uncertain Information," presented by G. De Micheli (Stanford Univ.). Keynote Address II is titled "Radical Reaction Based Semiconductor Manufacturing for Small Volume and Very High Speed Production with a Very Wide Variety of Semiconductor Chips" to be presented by T. Ohmi (Tohoku Univ.). Keynote Address III is titled "The Role of IP in Ensuring SoC Yield" to be presented by Y. Zorian (Virage Logic).

Following Panel Discussions will be performed: Session 4B is titled "Anatomy of Platform-Based Design - Is it the golden solution for SoC design productivity?" organized by T. Inoue and T. Nakamura (STARC). Session 5C is titled "Adaptive Computing - What can it do, where can it go?" organized by R. Reuss (DARPA). Session 6B is titled "Roles of Funding Agencies" organized by K. Nakajima (UMD and NAIST) and Brian Schott (USC).

Several Invited Talk sessions are also organized by a number of distinguished researchers. Session 5B is titled "Virtual Core Based Reuse Methodology for SoC Design," that consists of three paper presentations and a tool demonstration presented. Session 6C, somewhat different form others, is titled "Legal Protection for Semiconductor Intellectual Property (IP)." Session 7B is titled "Design Methodologies for 50M Gate ASICs." Session 7C is titled "Mixed Signal Test." Embedded Tutorial session (4D) is on low power and power management technologies.

As Co-Chairs of Technical Program Committee, we would like to thank all members of the Technical Program Committee, Topic Chairs M. Fujita, H. Takada, S. Minato, H. Terai, K. Nakamae, A. Matsuzawa, K. Nishi, K. Nakajima, H. Amano, and their Vice Topic Chairs, reviewers of papers, session organizers and moderators, and authors and speakers who submitted papers and will give presentation in the conference. We are grateful to the Publication Co-Chairs K. Fujiyoshi and K. Kobayashi for their contribution to prepare advance and final program brochures and the proceedings of the conference. We also appreciate TPC Vice Chair M. Yanagisawa, TPC Secretaries Y. Takeuchi, J. Kitamichi, and K. Sakanushi for their contribution to handle huge number of paper submission, prepare technical program of the conference.

We would be more than happy if you could attend the conference and find something new in the directions of EDA and design technologies in ASP-DAC 2003.

Masaharu Imai and Jason Cong
Co-Chairs: ASP-DAC 2003 Program Committee