# On Effective Criterion of Path Selection for Delay Testing

Masayasu Fukunaga[1], Seiji Kajihara[1,2], Sadami Takeoka[3], Shinichi Yosimura[3]
1: Department of Computer Science and Electronics, Kyushu Institute of Technology
2: Center for Microelectronics System, Kyushu Institute of Technology
3: Matsushita Electric Industrial Co., Ltd., Semiconductor Company
E-mail : fukunaga@aries30.cse.kyutech.ac.jp, kajihara@cse.kyutech.ac.jp,
takeoka@mrg.csdd.mei.co.jp, syoshi@ngk.csdd.mei.co.jp

**Abstract – Since a logic circuit often has too many paths to test delay of all paths in the circuit, it is necessary for path delay testing to limit the number of paths to be tested. Paths to be tested should be ones with large delay that more likely cause a fault. In addition, a test set for the paths are required to detect other models of faults as many as possible. In this paper, we investigate criteria of path selection for path delay testing. We first define typical two criteria to be investigated here, and then experimentally show the feature of paths selected with each criterion, with respect to fault coverage of other delay fault models. From our experiments, we observe that test patterns for the longest paths cannot cover many other faults such as gate delay faults or segment delay faults.**

## I. INTRODUCTION

It is getting more and more important for high perforemance VLSIs to test the timing behavior of manufactured circuits. DC functional test such as scan test can detect static faults such as stuck-at faults, but not detect dynamic faults such as delay faults. There are some fault models for delay faults, which are transition fault, gate delay fault, segment delay fault, and path delay fault [1]. Among them, the path delay fault model has an advantage because it models localized as well as distributed excessive delays. Hence, test patterns generated for path delay faults can detect many defects such as stuck-at faults or other delay faults. From these reasons, we can attain high quality test by testing path delay faults.

Though it is ideal that all the path delay faults are tested by a test set, it is actually difficult to test all path delay faults of a circuit. This is because the number of paths can be exponential in the circuit size, and is typically very large. In addition, there is a case that most of the path delay faults are untestable [2],[3]. In order to generate test patterns for path delay faults, it is considered to limit the number of paths to be tested before test generation [4-7].

When selecting paths to be tested, it is desirable to satisfy the following three conditions:

(1) Signal propagation delay of the selected paths is large.
(2) The selected paths are testable.
(3) Test patterns for the selected paths have high fault coverage for other models of faults like stuck-at faults or other delay faults.

Even if we test paths extracted by a static timing analyzer, it is insufficient to detect delay defects of the circuit because conditions (2) and (3) are not considered enough.

A path selection method which is taking on account of conditions (1) and (2) has been proposed in [7]. The method deals with condition (1) such that, for each line in the circuit, all the longest paths through the line are included in the set of selected paths. As for condition (2), the method avoids selecting untestable paths as target paths. However, condition (3) was not considered at all.

In this paper, we experimentally investigate how the difference of criteria for path selection influences detection of delay defects modeled as other faults. If a test set for path delay faults selected with a criterion can detect more faults of other fault models, high quality test can be attained. In this paper we first define two criteria to be investigated; one is that the predefined number of longer paths of the circuit is selected in order of the path length. Another criterion is that, for each line in the circuit, all the longest paths through the line are selected similarly to [4],[7]. In order to evaluate each criterion, we then apply path selection procedures based on each criterion for ISCAS benchmark circuits, and compare the feature of paths selected with each criterion, with respect to coverage of other delay fault models. From our experiments, we observe that tests for the longest paths cannot cover many other faults such as gate delay faults or segment delay faults. Also we observe that testing paths selected with the later criterion covers most of other models of faults as well as path delay faults for the longest paths of the circuit

This paper is organized as follows. In Section 2, we review delay fault models and describe faults detected by path delay testing. In Section 3, we present path selection criteria to be investigated in this paper. In Section 4, we discuss the features of the criteria from experimental results for ISCAS benchmark circuits. Finally we give a conclusion in Section 5.

## II. PRELIMINARIES

### A. Delay fault models

In this paper, we aim at a combinational circuit or a full scan sequential circuit, and assume single faults. There are some delay fault models that have been developed to

represent delay defects. The transition fault model describes excessive propagation delay of a signal line due to a defect [8]. The gate delay fault model describes excessive switching delay of a logic gate [9]. The path delay fault model describes excessive propagation delay of a path between a primary input (or a pseudo primary input) and a primary output (or a pseudo primary output) of a circuit [10]. The segment delay fault describes excessive propagation delay of successive lines, that is a partial path [11].

For a path $P$, if line $l_i$ is included in $P$, $l_i$ is referred to as an on-path input of $P$. A line $l_j$ is referred to as an off-path input associated with on-path input $l_i$ of $P$ if $l_j$ is not an on-input but it drives a gate $G$ that is also driven by $l_i$. When an input vector that assigns non-controlling values on every off-input of the path exists, regardless of the final value of the on-input of the path, we call the path $P$ non-robust testable path. When no input vectors that enable the path $P$ to be non-robust testable exist, we call the path $P$ non-robust untestable path. Some methods for identifying untestable paths have been presented in [2,3,12-14]. Also it has been reported that most of the path delay faults in circuits with large number of paths are untestable. Note that while untestable paths identified by these methods are certainly untestable, other paths are not necessarily testable. A path not identified as untestable is referred to as a potentially testable path [7].

The length of path $P$, in this paper, is defined as a time of the accumulated gate delay on $P$, where delay time of each gate is used in a given cell library. Hence the longest path is one with the largest delay time.

B. Faults detected by path delay testing

If path delay faults were detected by a test set, many defects on the paths would be detected simultaneously. For example in a circuit of Fig. 1, a path delay fault on path *a-c-e-g* with rising transition is detected by test patterns ($a$,$b$,$d$,$f$) =(0,0,1,1), (1,0,1,1). The test patterns also detect segment delay faults on *a-c-e-g* as well as gate delay faults at *G0, G1, G2*. Thus, if all path delay faults of the circuit were tested, most of delay defects would be detected. Therefore, we can attain high quality test by a test set for the path delay faults. However it is impractical to test all path delay faults of the circuit, because the number of paths is typically very large. Hence, it is considered to limit the number of paths to be tested before test generation.

By limiting paths to be tested to a part of paths of the circuit, some delay defects on a path that was not tested may not be detected. Therefore depending on criterion of path selection, fault coverage for delay defects would be changed.

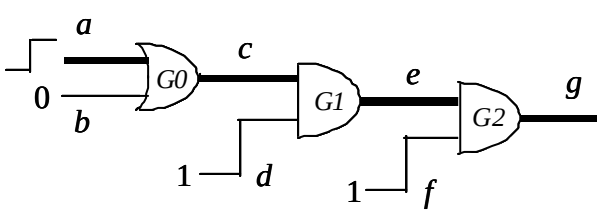



Fig 1. Faults detected by path delay testing

In the following sections, we investigate two criteria for path selection.

## III. PATH SELECTION CRITERIA

As a set of paths to be tested, it is desirable to select paths that more likely cause a timing defect, i.e., longer paths should be selected. And the set of paths should not contain untestable paths. A procedure to select longest potentially testable paths is given in [7]. In order to evaluate how test patterns for the selected paths have high fault coverage for other models of faults, we consider two criteria for path selection as follows:

**Criterion 1: Select *N* longest paths in order of the path length.**

Note that $N$ is a predefined arbitrary number and paths selected are potentially testable. We illustrate the outline of this criterion in Fig. 3. In this criterion, we first search the longest path in a circuit (Fig. 3 (a)). Next, we search the next longest path and repeat this process until the number of selected path reaches to $N$ (Fig. 3 (b)).

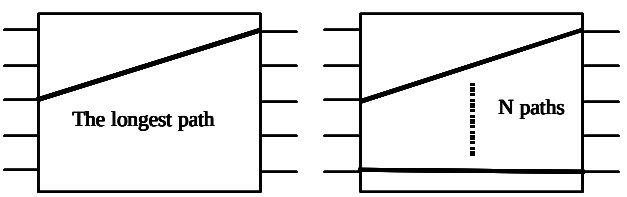
When we employ Criterion 1, the length of every selected path is longer than the length of any unselected path. Therefore, the probability that the selected paths are faulty would be higher than that of unselected one. On the other hand, the selected paths may not be distributed all over the circuit and may locally be concentrated in some area.

The other criterion is given below:

**Criterion 2: For each line of the circuit, select all the longest paths through the line.**

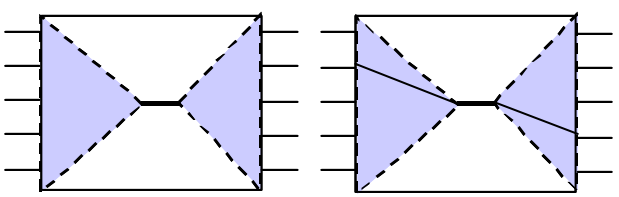
Note that only potentially testable paths are selected too.

We illustrate the outline of this criterion in Fig. 4. In this criterion, we first set a target line, and mark the lines of




(a) Search the longest path (b) Search the N longest paths

Fig 3. Outline of the Criterion 1



(a) Set the target line and mark (b) Select the longest path

Fig 4. Outline of the Criterion 2

which the transition is reachable from/to the target line (Fig. 4 (a)). Next, we select the longest path consisting of the marked lines (Fig. 4 (b)).

When we employ Criterion 2, the selected paths would be distributed uniformly all over the circuit. On the other hand, an unselected path may be longer than a selected path.

A longest path for a line is sometimes the same as that of for another line [7]. For example in Fig. 1, the longest path for line *a* and line *c* is the same. Since the longest path for a gate output is included in the longest paths for fanin lines of the gate. Therefore, we should not select the longest paths for all lines but should select for partial lines.

Criterion 2 can be changed as follows:

**Criterion 2': For each line that is a primary input or a fanout branch of the circuit, select all the longest paths through the line.**

We refer to Criterion 2' as Criterion 2 in the rest of the paper.

We give examples of path selection with the above criteria. Given a circuit in Fig. 2, Table 1 shows paths in decreasing order of path length. Assume that the path length is determined by the number of logic gates on the path. The longest path of the circuit is *c-d-f-j-l-o-p* on which there are five gates. If the number of selected paths, *N*, is three in Criterion 1, then paths *c-d-f-j-l-o-p*, *a-e-i-j-l-o-p* and *b-f-j-l-o-p* are selected. If *N* is five, the four longest paths and arbitrary one of the paths with length two are selected.

If Criterion 2 is applied for the circuit, seven paths given in Table 2 are selected. In this case, the longest path for line *a* is the same as that for line *i*. Similarly, the longest path for line *c* and line *l* is identical. Thus the number of selected paths is seven although the amount of primary inputs and fanout branches are nine. If there is more than one longest path for a line, all the paths are selected.

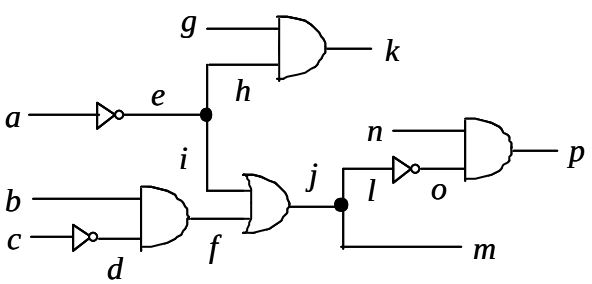



Fig 2. Example circuit

Table 1. Criterion 1

| path length | path |
|---|---|
| 5 | c-d-f-j-l-o-p |
| 4 | a-e-i-j-l-o-p |
| 4 | b-f-j-l-o-p |
| 3 | c-d-f-j-m |
| 2 | a-e-h-k |
| 2 | a-e-i-j-m |
| 2 | b-f-j-m |

Table 2. Criterion 2

| target line | selected path |
|---|---|
| a,i | a-e-i-j-l-o-p |
| b | b-f-j-l-o-p |
| c,l | c-d-f-j-l-o-p |
| g | g-k |
| h | a-e-h-k |
| m | c-d-f-j-m |
| n | n-p |

## IV. RESULTS AND DISCUSSIONS

### A. Experiment

We implemented the path selection method with both criteria described above using C programming language on a PC (Pentium III 1GHz, 1152MB memory, OS: Free BSD 4.5) and applied it to ISCAS benchmark circuits. For selected paths with each criterion, we compared coverage for segments and investigated the difference of the selected paths each other. In order to make a fair comparison, we set the number of selected paths *N* in Criterion 1 to the same one with selected paths with Criterion 2. Path selection with Criterion 1 is repeated until the number of selected paths reaches to *N*. Also we avoided selecting non-robust untestable paths by using the partial path sensitization [7], i.e., all the selected paths are potentially non-robust testable.

### B. Coverage for segment delay faults

Table 3 and Table 4 show results with Criterion 1 and Criterion 2, respectively. In the tables, the first three columns shows the circuit name, the number of paths of the circuit and the number of selected paths, respectively. The remaining columns give coverage of segments when segment length is 1 to 3. When the segment length is 1, each segment means a line. Hence if a selected path passes through the line, transition faults on the path would be detected by test patterns to detect the path delay fault. In Table 3 and Table 4, the column head "#lines" shows the number of lines of the circuit, and the column head "#covered lines" shows the number of lines through that selected paths. The column head "%coverage" shows the percentage of covered lines by the selected paths. When the segment length is 2, each segment means successive two lines. Hence if a selected path passes through the segment, gate delay faults on the pass would be detected by test patterns to detect the path delay fault. Not only gate delay faults but also segment delay faults consisting of a fanout stem and its fanout branch can be included in the case of segment length=2. When the segment length is 3, each segment means successive three lines on which at least one gate is included.

From Table 3 we can observe that the paths selected with Criterion 1 could not cover more than 70% of segments on the average. We can also imagine that the paths concentrate in parts around critical paths of the circuit. Therefore, a test set for the paths would miss a lot of delay defects such as transition faults or gate delay faults.

On the other hand, we can observe from Table 4 that the paths selected with Criterion 2 cover almost all segments of the circuit. Therefore, a test set for the path delay faults would have high fault coverage for stuck-at faults, transition faults, and gate delay faults. Even for segment delay faults, the test set would keep high fault coverage when segment

Table 3. Segment coverage of Criterion 1

| circit | #total paths | #selected paths | Segment Length =1 | | | Segment Length =2 | | | Segment Length =3 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | #lines | #covered lines | %coverage | #seg. | #covered seg. | %coverage | #seg. | #covered seg. | %coverage |
| c880 | 17,284 | 1,851 | 1,760 | 579 | 32.90 | 2,332 | 677 | 29.03 | 2,870 | 779 | 27.14 |
| c1355 | 8,346,432 | 107,296 | 2,710 | 1,828 | 67.45 | 3,664 | 2,272 | 62.01 | 5,136 | 2,880 | 56.07 |
| c1908 | 1,458,114 | 7,087 | 3,800 | 1,004 | 26.42 | 4,970 | 1,276 | 25.67 | 6,904 | 1,577 | 22.84 |
| c2670 | 1,359,920 | 7,441 | 5,340 | 924 | 17.30 | 6,640 | 1,134 | 17.08 | 8,568 | 1,378 | 16.08 |
| c3540 | 57,353,342 | 10,194 | 7,080 | 1,526 | 21.55 | 9,520 | 1,870 | 19.64 | 12,620 | 2,281 | 18.07 |
| c5315 | 2,682,610 | 10,867 | 10,630 | 1,865 | 17.54 | 14,432 | 2,308 | 15.99 | 19,060 | 2,939 | 15.42 |
| c7552 | 1,452,988 | 9,387 | 15,104 | 3,535 | 23.40 | 19,954 | 4,222 | 21.16 | 28,008 | 5,021 | 17.93 |
| s5378 | 27,084 | 9,050 | 10,590 | 5,534 | 52.26 | 13,028 | 6,493 | 49.84 | 15,702 | 7,465 | 47.54 |
| s9234 | 489,708 | 14,005 | 18,468 | 6,679 | 36.17 | 22,722 | 7,769 | 34.19 | 27,576 | 9,005 | 32.66 |
| s13207 | 2,690,738 | 28,857 | 26,358 | 2,512 | 9.53 | 31,386 | 3,440 | 10.96 | 37,082 | 4,464 | 12.04 |
| s15850 | 329,476,092 | 68,383 | 31,694 | 1,198 | 3.78 | 38,218 | 1,408 | 3.68 | 45,766 | 1,682 | 3.68 |
| s35932 | 394,282 | 37,508 | 71,224 | 40,865 | 57.38 | 92,106 | 49,389 | 53.62 | 103,670 | 58,422 | 56.35 |
| s38417 | 2,783,158 | 203,458 | 76,678 | 11,256 | 14.68 | 93,048 | 12,900 | 13.86 | 111,332 | 14,712 | 13.21 |
| s38584 | 2,161,446 | 56,517 | 76,864 | 2,111 | 2.75 | 100,942 | 2,547 | 2.52 | 124,202 | 3,135 | 2.52 |
| Average | | | | | 27.37 | | | 25.66 | | | 24.40 |

Table 4. Segment coverage of Criterion 2

| circit | #total paths | #selected paths | Segment Length =1 | | | Segment Length =2 | | | Segment Length =3 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | #lines | #covered lines | %coverage | #seg. | #covered seg. | %coverage | #seg. | #covered seg. | %coverage |
| c880 | 17,284 | 1,851 | 1,760 | 1,760 | 100.00 | 2,332 | 2,332 | 100.00 | 2,870 | 2,663 | 92.79 |
| c1355 | 8,346,432 | 107,296 | 2,710 | 2,710 | 100.00 | 3,664 | 3,664 | 100.00 | 5,136 | 4,968 | 96.73 |
| c1908 | 1,458,114 | 7,087 | 3,800 | 3,787 | 99.66 | 4,970 | 4,948 | 99.56 | 6,904 | 6,303 | 91.29 |
| c2670 | 1,359,920 | 7,441 | 5,340 | 5,303 | 99.31 | 6,640 | 6,577 | 99.05 | 8,568 | 8,255 | 96.35 |
| c3540 | 57,353,342 | 10,194 | 7,080 | 6,838 | 96.58 | 9,520 | 9,156 | 96.18 | 12,620 | 11,347 | 89.91 |
| c5315 | 2,682,610 | 10,867 | 10,630 | 10,599 | 99.71 | 14,432 | 14,372 | 99.58 | 19,060 | 18,056 | 94.73 |
| c7552 | 1,452,988 | 9,387 | 15,104 | 15,052 | 99.66 | 19,954 | 19,859 | 99.52 | 28,008 | 25,560 | 91.26 |
| s5378 | 27,084 | 9,050 | 10,590 | 10,508 | 99.23 | 13,028 | 12,903 | 99.04 | 15,702 | 15,275 | 97.28 |
| s9234 | 489,708 | 14,005 | 18,468 | 17,138 | 92.80 | 22,722 | 20,908 | 92.02 | 27,576 | 24,277 | 88.04 |
| s13207 | 2,690,738 | 28,857 | 26,358 | 26,131 | 99.14 | 31,386 | 30,997 | 98.76 | 37,082 | 35,321 | 95.25 |
| s15850 | 329,476,092 | 68,383 | 31,694 | 31,069 | 98.03 | 38,218 | 37,150 | 97.21 | 45,766 | 42,335 | 92.50 |
| s35932 | 394,282 | 37,508 | 71,224 | 64,136 | 90.05 | 92,106 | 81,178 | 88.14 | 103,670 | 87,611 | 84.51 |
| s38417 | 2,783,158 | 203,458 | 76,678 | 76,512 | 99.78 | 93,048 | 92,770 | 99.70 | 111,332 | 108,766 | 97.70 |
| s38584 | 2,161,446 | 56,517 | 76,864 | 73,569 | 95.71 | 100,942 | 95,966 | 95.07 | 124,202 | 110,961 | 89.34 |
| Average | | | | | 97.83 | | | 97.42 | | | 92.69 |

length is not long.

C. Overlap of selected paths

Some paths selected with Criterion 2 are not included in the set of paths selected with Criterion 1. Such paths are shorter than any path selected with Criterion 1. However, there are many paths that are selected with both criteria. In Table 5 we shows how paths selected are overlapped with the both criteria. The column headed *#overlapped paths* in Table 5 shows the number of paths that are selected with both Criterion 1 and Criterion 2, and the column headed *%overlapped paths* shows the percentage of the overlapped paths. While the percentage of the overlapped paths was different depending on the circuit, it was less than 40% for 11 of 14 benchmark circuits. In short, paths selected with Criterion 2 do not include many longer paths of the circuit. However, it is theoretically guaranteed that the longest paths of the circuit are included in the paths selected with Criterion 2. Furthermore, the longer the length of a path selected with Criterion 1 was, the higher the percentage of the overlapped path was. We divided the paths selected with Criterion 1 into ten subsets such that each subset contains 10% from the longer paths, and showed, in Fig. 5, the percentage of the overlapped paths in each subset on the

Table 5. Paths overlapped between two criteria

| circuit | #selected paths | #overlapped paths | %overlapped paths |
|---|---|---|---|
| c880 | 1,851 | 458 | 24.74 |
| c1355 | 107,296 | 61,440 | 57.26 |
| c1908 | 7,087 | 1,454 | 20.52 |
| c2670 | 7,441 | 1,072 | 14.41 |
| c3540 | 10,194 | 1,376 | 13.50 |
| c5315 | 10,867 | 1,266 | 11.65 |
| c7552 | 9,387 | 668 | 7.12 |
| s5378 | 9,050 | 4,303 | 47.55 |
| s9234 | 14,005 | 3,860 | 27.56 |
| s13207 | 28,857 | 5,624 | 19.49 |
| s15850 | 68,383 | 5,234 | 7.65 |
| s35932 | 37,508 | 23,940 | 63.83 |
| s38417 | 203,458 | 78,523 | 38.59 |
| s38584 | 56,517 | 10,705 | 18.94 |

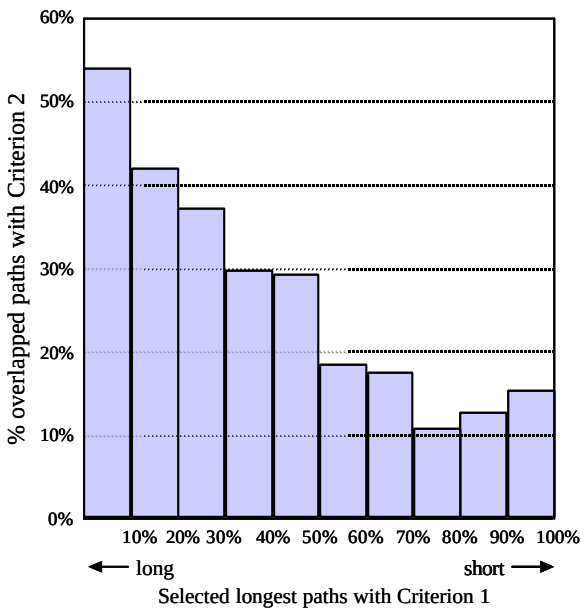



Fig 5. Distribution of overlapped paths

average for all the benchmark circuits. Thus, even if we select paths with criterion 2, many longer paths in the circuit are selected.

D. CPU time

Table 6 shows the result of CPU time with this experiment. From the table 6, we can observe that path selection by Criterion 2 is faster than Criterion 1 almost all benchmark circuits. Also, for large circuits, the difference of CPU time of two criteria is very large. This is because that the process of path selection by Criterion 1 is based on the iteration.

Table 6. CPU time of two criteria

| circuit | #selected paths | CPU time on Criterion 1 (sec) | CPU time on Criterion 2 (sec) |
|---|---|---|---|
| c880 | 1,851 | 1.53 | 4.63 |
| c1355 | 107,296 | 52.56 | 76.58 |
| c1908 | 7,087 | 165.90 | 57.13 |
| c2670 | 7,441 | 33.69 | 17.14 |
| c3540 | 10,194 | 3148.42 | 397.18 |
| c5315 | 10,867 | 55.80 | 36.63 |
| c7552 | 9,387 | 105.26 | 55.92 |
| s5378 | 9,050 | 46.50 | 28.50 |
| s9234 | 14,005 | 280.64 | 49.97 |
| s13207 | 28,857 | 1432.12 | 131.60 |
| s15850 | 68,383 | 2709.13 | 598.73 |
| s35932 | 37,508 | 503.47 | 670.65 |
| s38417 | 203,458 | 2112.69 | 487.69 |
| s38584 | 56,517 | 5598.49 | 784.48 |

## V. CONCLUSION

In this paper, we investigated criteria of path selection for path delay testing. For two typical criteria, we experimentally showed the features of paths selected with each criterion, with respect to fault coverage of other delay fault models. From our experiments, we observed that test patterns for the longest paths selected with Criterion 1 would not cover many other faults such as gate delay faults or segment delay faults. Also we found that testing paths selected with Criterion 2 would cover most of other models of faults as well as path delay faults of the longest paths in the circuit.

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