Error Correction Circuit using Difference-set Cyclic Code

Yukihiro Kato

Department of Systems Engineering and Science
Graduate School of Engineering
Tokyo Metropolitan Institute of Technology
Hino, Tokyo 191-0065, Japan
Tel: +81-42-585-8651
FAX: +81-42-585-8651
e-mail: qm013516@cc.tmit.ac.jp

Tomokazu Morita

Department of Electric systems Engineering
Faculty of Engineering
Tokyo Metropolitan Institute of Technology
Hino, Tokyo, 191-0065, Japan
Tel: +81-42-585-8600
Fax: +81-42-583-5119
e-mail : qu001246@cc.tmit.ac.jp

Abstract -- An error correction receiver using difference-set cyclic code has been designed. Highly reliable operation, short critical path, and small circuit size are key issues. The synchronization circuit is optimized in its circuit size by detecting 10 kinds of bit sequences for synchronization. The circuit action is governed by state machine combined with a Johnson counter and a timer. The critical path length is estimated to be 4.8, which is less than average value.

I. INTRODUCTION

A differential-set cyclic code error correction receiver has been designed. Following the introduction of the block diagram in Sec. II, synchronization circuit and state machine are described in Sec. III and IV , respectively. The circuit is written in VHDL and synthesized for FPGA as a target device, whose results are summarized in Sec. V.

II. BLOCK DIAGRAM

Figure 1 illustrates the block diagram of the receiver. The data path is comprised of synchronization circuit, 21-bit shift register, and error correction circuit. The receiver operation is governed by the state machine.

Note that the error detection logic is a linear feedback shift register (LFSR), just described in the specification of this task.
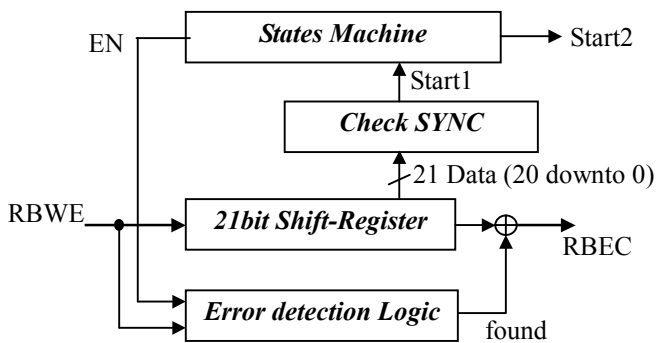

Fig. 1   Block Diagram

III. SYNCHRONOUS SIGNAL DETECTION

The issue in the synchronization is how to detect desired bit patterns containing errors. The authors figure out that the source program of the transmitter ("transmitter.vhd") indicates the bit sequences for synchronization are finite, i.e., only 10 kinds of patterns (E1--E10) listed in Table I, where errors occur at every 10 bits.

Hence, the synchronization circuit has been constructed so that the received sequence saved in the 21-bit shift register is compared with 10 bit-patterns in parallel.

The more advanced means is considered about the synchronization detection method.

The difference from a synchronization signal is counted at intervals of 7 bits. If the difference bit is to three, it will accept as a synchronization signal. The advantage which is this design. The 1st, It can treat efficiently 7 bits of 21bit synchronization signals at a time. The 2nd, since an output becomes 2 bits, bit slice adder of 7 inputs does not have the bit that becomes useless. The 3rd, the output result of fbit slice adder[1], can discover four or more errors using a logic circuit.

A critical path is set to two steps of full adders in bit slice adder of the 3-bit output of 7-bit inputs. Moreover, in order to discover the difference from a 21-bit synchronized signal, the bit which is a part of 21-bit signal inputted into the shift register, is reversed. The reversed bit is a position of "1" in a regular synchronized signal. All bits are set to 0 if certainly the same as a synchronized signal.

Table. 1   Error Pattern
Italic =Error bits, T=without errors synchronous signal
E1-10= the pattern in consideration of the error

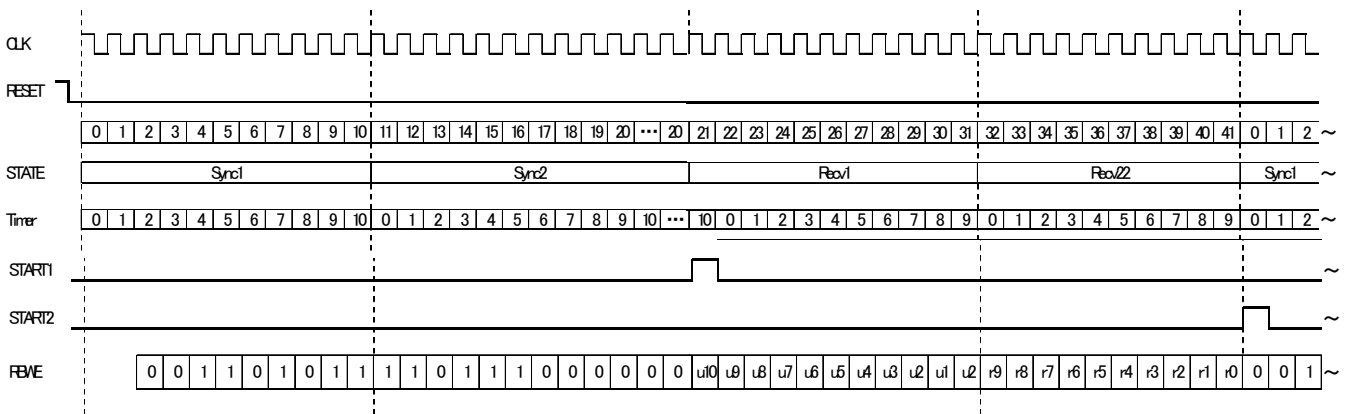| T	0	0	1	1	0	1	0	1	1	1	1	0	1	1	1	0	0	0	0	0	0
E1	*1*	0	1	1	0	1	0	1	1	1	*0*	0	1	1	1	0	0	0	0	0	*1*
E2	0	*1*	1	0	1	0	1	1	1	1	*1*	1	1	1	0	0	0	0	0	0	0
E3	0	0	*0*	1	0	1	0	1	1	1	0	*0*	1	1	0	0	0	0	0	0	0
E4	0	0	1	*0*	0	1	0	1	1	1	0	1	*0*	1	0	0	0	0	0	0	0
E5	0	0	1	1	*1*	1	0	1	1	1	0	1	1	*0*	0	0	0	0	0	0	0
E6	0	0	1	1	0	*0*	0	1	1	1	0	1	1	1	*1*	0	0	0	0	0	0
E7	0	0	1	1	0	1	*1*	1	1	1	0	1	1	1	0	*1*	0	0	0	0	0
E8	0	0	1	1	0	1	0	*0*	1	1	0	1	1	1	0	0	*1*	0	0	0	0
E9	0	0	1	1	0	1	0	1	*0*	1	0	1	1	1	0	0	0	*1*	0	0	0
E10	0	0	1	1	0	1	0	1	1	*0*	0	1	0	1	1	1	0	0	0	*1*	0

Fig. 2   Timing chart

IV. STATE MACHINE

Figure 2 shows the timing chart diagram f the receiver, consisting of two stages, i.e., synchronization and receiving stages. Each stage is further divided into 2 states, so that the entire operation is defined by 4 states as shown in the state diagram (figure 3). The state machine is implemented with 2-bit Johnson counter [1], and the state transition is invoked by the timer counting 9 or 10 clocks. Here, the transition from SYNC2 to RECV1 requires an additional condition of the detection of the synchronization signal.

Our design eliminates 5 or 6-bit comparators required in the conventional design, resulting in hazardless state transition, smaller size of the circuit, and enables quick modification of the bit length of the signal through the modification of the timer length.

In order to reduce the power consumption, the synchronization circuit and the error detection logic are temporally suspended; namely, synchronization circuit operates within SYNC2 state during the timer counts 10 or greater. Error detection circuits works during RECV2 state.
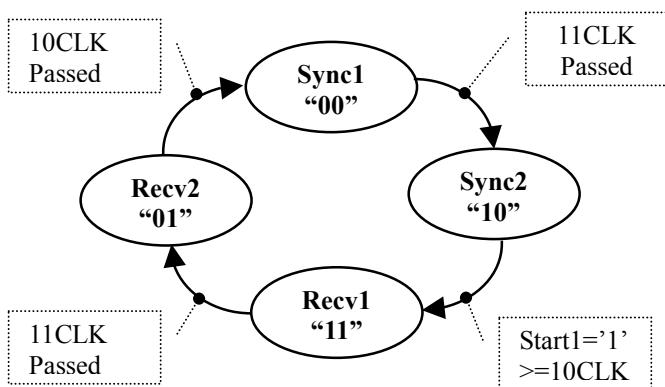

Fig. 3   Four-states Changing Machine diagram

IV. Implementation and Performance

The receiver has been written by VHDL, and synthesized with Xilinx XST synthesis tool [2], where the target device is Xilinx Spartan-II FGPA (XC2S150-5).

A. *Critical Path*

The speed of the receiver has been evaluated by the procedure described in the specification of the predefined task. A 50-inputs XOR circuit is synthesized into 6-stage gates, and the total maximum delay is 13.0 ns, corresponding to 2.17ns for each stage. The maximum delay path of the present receiver is 10.60 ns, resulting in 4.88 unit delay. But that of another circuit using full adder is 8.61 unit delay. This value is smaller than the average (~5 unit delay) reported at the previous contest [3]

B. *Circuit size*

The receiver has been implemented with 32 slices, which occupy only 2 % of the total 1728 slices prepared in the target device.

VI. SUMMARY

An error correction receiver using difference-set cyclic code has been designed with emphasis on the optimum design of the synchronization circuit and the state machine. Our design shows highly reliable operation, short critical path, and small circuit size, and easy configuration modification. The smaller circuit hides a possibility of being highly efficient machines, not only a hardware system with low power consumption but also highly an efficient system such as a cellular phone.

REFERENCES

[1] Y. Koboyashi, "The logic circuit design of ASIC", CQ Publishing Corporation (1998) [in Japanese]
[2] Xilinx Synthesis Tools, version4.1
[3] Design Wave Magazine Design Contest, 6 March 2002, Ryukyu University; *see also* Design Wave Magazine, July 2002, CQ Publishing Corporation [in Japanese].