Design of a CMOS Test Chip for Package Models and I/O Characteristics Verification

Chetan Despande and Tom Chen*

1 Introduction

Reliable packages for modern chips are crucial for satisfactory system performance. In order to ascertain package's performance, an equivalent electrical model is plugged into circuit simulations and the package's performance characteristics can be analyzed. However, one implicit assumption designers make is that these equivalent electrical models are accurate for performance characterization of packages. For modern high-speed designs, verification of the accuracy of these models is imperative and can only be carried out on real-silicon. In addition, signal integrity for inter-chip communication is crucial from a systems perspective. To study the signal integrity of data under different PVT (process variation, voltage, and temperature) conditions, appropriate test structures are needed. Data can be subjected to controlled variations through these structures and its integrity can be studied. And finally, testing package reliability at high temperatures is important since on-chip temperatures are increasing dramatically as processes continue to scale. The test chip presented in this design is intended to allow 1) circuit and package designers to evaluate and validate the accuracy of package models under a variety of environment conditions; 2) system designers to evaluate package/system level signal integrity issue before actual chips are available; and 3) system designers to evaluate on-chip temperatures and to study thermal integrity of packages. The test chip includes a variety of features to achieve these goals. The test chip is fabricated at TSMC in a 0.18 μm CMOS process. The measurement results and the die microphotograph will be sent later as soon as they are available. This paper presents the layout based simulation results.

2 Description of the Test Chip

The chip has six core blocks consisting of a 3to8 decoder. Each output of the decoder drive a different set of ring-oscillators to generate different current settings. Figure 1 shows the block diagram of the core. The decoder is controlled using three bits. Each of the decoder outputs drive 640 ring oscillators drawing approximately 0.54A of average current. By varying the control signals, additional blocks can be turned on, drawing more step currents. The layout of the core is shown in Figure 2. For a given package design, the efficiency of the package response to the current requirements on the chip for varying amounts of on-chip bypass capacitance can be examined with the test chip using controllable on-chip bypass capacitance. The chip consists of three output pad rings, each driving 16-bit data array. The data array is a 1024 bit shift register, which is loaded using a single data pattern that is pre-determined. After every 64 registers, the output is taken as input stream to the 16-bit bus in the output pad ring. The the slew rate of the output data can be controlled. The I/O cell incorporates selectable driver impedances to drive the data off the chip. To counter power supply droop under high frequency switching conditions, controllable bypass capacitors have been incorporated in the I/O cell to study power supply droop and its effect on data performance under different bypass capacitor configurations. The layout of the I/O cell is as shown in Figure 2. For thermal-mechanical integrity evaluations, daisy chains have been employed in this design. The test chip has blocks that draw currents to the order of tens of amperes at high operating frequencies. Some of these blocks can be made to switch, generating heat, while other parts of the chip can be controlled to be relatively cooler. Thus, a significant temperature gradient across the die can be generated and thermal expansion effects can be studied. Temperatures on the chip are collected by 10 temperature sensors placed at different regions on the die. Table 1 lists the features of the test chip. Figure 3 shows the top level layout with the six core blocks, the input pad ring for the control signals and the three output pad rings to drive data off the chip. At the center of the chip is the data array that generates the sixteen bit data and the repeaters for global routes.

Process	TSMC $0.18\mu m$ process
Power Supply	1.8v (Core)/1.5v (I/O)
Die Size	(9.8 x 13)mm
FET Count	1.8 million
I/O pins	122
VDD and GND pins	2950

Table 1: Features on the Test Chip

*This work was partially supported by Hewlett Packard Co. Chetan Despande and Tom Chen are with the Department of Electrical and Computer Engineering, Colorado State University, Fort Collins, Colorado, USA

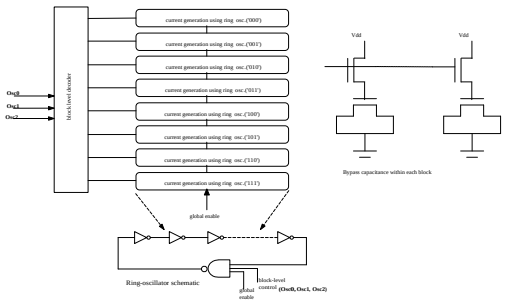


Figure 1: Block diagram of the core.

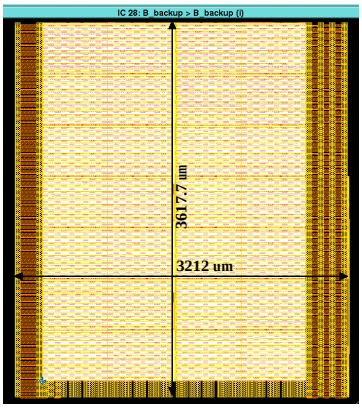


Figure 2: Layout of the core and I/O cell

3 Simulation Results

We just received the silicon die back from the manufacturer and have not performed measurements of the chip yet. Therefore, the simulation results is presented here. Figure 4 shows the layout based simulation of the core drawing a step load. Figure 5 are the simulation showing the effect of controllable bypass capacitances to reduce power supply droop. This simulation was done using a given package model to take package response into account. It can be seen that as the amount of bypass capacitance turned on increases, the quality of the signal at the pad improves substantially. Figure 5 clearly shows the improvement in the power supply droop with additional amounts of bypass capacitance.

4 Conclusions

A test chip design for package model verification has been presented. Package models can be practically verified before actual chips are available allowing concurrent engineering of chip design, package design, and system design. The programmability of the test chip allows it to be used for many different products.

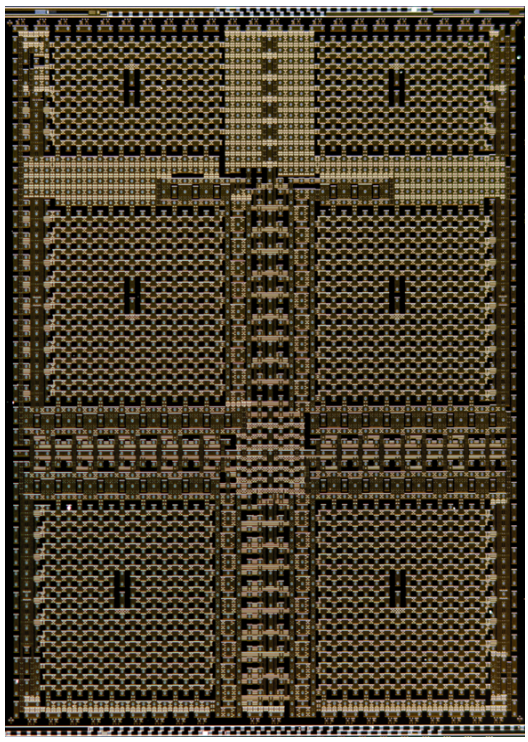


Figure 3: Microphotograph of the test chip

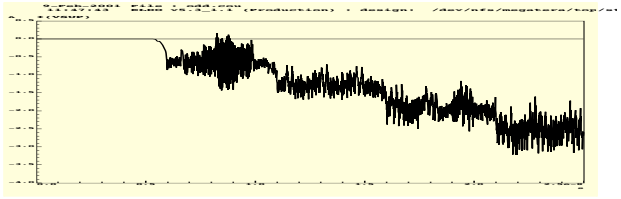
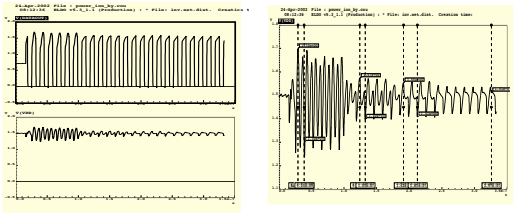


Figure 4: Current steps drawn by the blocks in the core



(a) (b)

Figure 5: Power supply droop and data at the pad showing the droop reduction with increasing bypass cap.