A Power and Resolution Adaptive Flash Analog-to-Digital Converter

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ABSTRACT

A new power and resolution adaptive flash ADC, named PRA-ADC, is proposed. The PRA-ADC enables exponential power reduction with linear resolution reduction. Unused parallel voltage comparators are switched to standby mode. The voltage comparators consume only the leakage power during the standby mode. The PRA-ADC, capable of operating at 5-bit, 6-bit, 7-bit, and 8-bit precision, dissipates 69 mW at 5-bit and 435 mW at 8-bit. The PRA-ADC was designed and simulated with 0.18 μm CMOS technology. The PRA-ADC design is applicable to RF portable communication devices, allowing tighter management of power and efficiency.

Categories and Subject Descriptors

B.7.1 [**Integrated Circuits**]: Types and Design Styles—*VLSI*

General Terms

Design

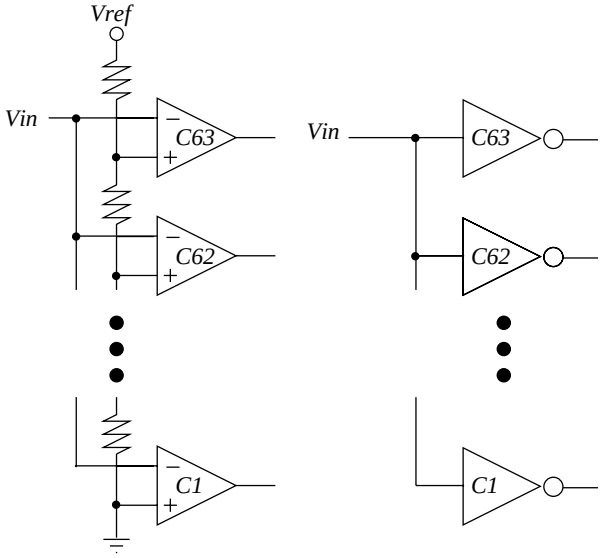
Keywords

Analog-to-Digital Converter, Flash ADC, Threshold Inverter Quantization, TIQ Comparator, Adaptive

1. INTRODUCTION

Resolution, speed, and power consumption are the three key parameters for an analog-to-digital converter (ADC). These parameters cannot be changed once an ADC chip has been fabricated. Of course, one can use only 6-bit precision from an 8-bit ADC chip, while full 8-bit operation takes place internally. Such an application is non-optimal, resulting in slower speed and extra power consumption due to full 8-bit internal operation. This proposition applies to the flash ADCs, which are parallel high-speed high-power ADCs.

A new flash ADC design is proposed in this paper, a true variable power and variable resolution ADC. It is named Power and Resolution Adaptive ADC (PRA-ADC). PRA-ADC can operate at higher speed and will consume less power when it operates at a lower resolution. The PRA-ADC feature is highly desirable in many wireless mobile applications. For example, the strength of a radio frequency (RF) signal varies greatly depending on geographic location. Optimally, the ADC resolution can be reduced upon the reception of strong signal, and the resolution can be increased upon the reception of weak signal. Substantial reduction of power consumption at lower resolution will prolong the battery-powered operation.



(a) Differential comparator (b) TIQ comparator

Figure 1: Two comparator architectures

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PRA-ADC design is based on the flash ADC architecture named Threshold Inverter Quantization (TIQ) ADC, designed and fabricated on chip by the authors[5, 6]. The next section outlines the key features of the TIQ ADC.

2. THE TIQ ADC

The TIQ ADC is a flash ADC which consists of $2^n - 1$ voltage comparators and 2^n bit to n bit encoder. The distinguishing feature of the TIQ ADC from the other flash ADCs[1, 3, 4, 7] is the use of CMOS inverters as voltage comparators. Figure 1 shows both the conventional flash ADC and the TIQ ADC. The conventional flash ADC uses differential voltage comparators along with a resistor ladder circuit to quantize analog input signal into digital signal. The TIQ ADC uses digital inverters having different internal threshold voltages to quantize analog input signal into digital signal. The built-in threshold voltage of a CMOS inverter acts as the reference voltage in voltage comparison. The TIQ comparator is simple and fast. Use of the resistor ladder circuit is eliminated. The TIQ comparator does not require switches, clock signals, or coupling capacitors. It is suitable for the standard CMOS technology and adaptable to future CMOS technology, down scaling beyond 100 nanometer.

Different inverter threshold voltage is obtained by changing the PMOS and NMOS transistor sizes of a CMOS inverter circuit. For an n bit TIQ ADC, one designs $2^n - 1$ inverters, each inverter threshold voltage different from all other inverters' threshold voltages. The authors also developed a systematic design method of $2^n - 1$ inverters such that the differential non-linearity (DNL) of the TIQ ADC is limited below the 0.25 LSB over the process variation, the temperature change, and the power supply voltage drift[2].

The voltage gain of the inverter comparator is boosted by cascading a number of inverters as needed following the first inverter. The gain boosting inverters can be all identical to each other.

On the negative side, the TIQ ADC exhibits up to ± 5 % variation of the ADC gain and offset errors due to the process, temperature, and power supply voltage variation. The linearity of the ADC also varies mainly due to the process variation; however, the variation is small and especially the DNL variation can be controlled within 0.25 LSB. A number of possible solutions exist for the gain and offset errors. One solution suitable on DSP applications is correcting the gain and offset errors numerically after the data acquisition. The raw data can be pre-processed with single multiply and single add/subtract operation to correct the gain and offset errors.

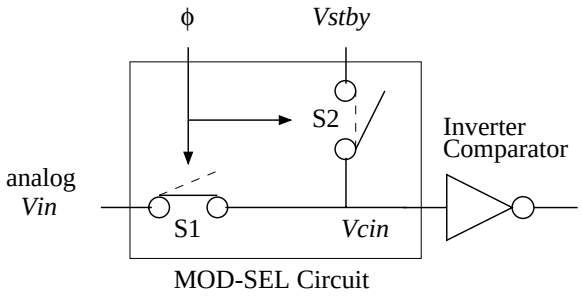

Figure 2: Active mode or standby mode selector circuit

3. PRA-ADC DESIGN

The key feature of the inverter comparator in TIQ ADC is the fact that the comparator can easily and quickly switch from active mode to standby mode. Figure 2 shows the simple addition to the inverter comparator input to select analog input voltage or V_{stby} voltage, selecting the active mode or standby mode. In the active mode, the switch S1 is on and the switch S2 is off, connecting the analog input signal to the inverter comparator input. In the standby mode, S1 is off and S2 is on, connecting V_{stby} voltage to the inverter comparator. The analog input signal voltage varies between the ground and the Vdd, but the V_{stby} voltage is fixed either to the ground or to the Vdd. In standby mode, the power consumption of the inverter comparator is due to only the leakage current of a PMOS or an NMOS transistor. A great deal of power saving is achieved per inverter comparator when it enters the standby mode.

In the PRA-ADC, the unused inverter comparators are switched to the standby mode to reduce power consumption. An 8-bit flash ADC requires $2^8 - 1 = 255$ voltage comparators and a 7-bit flash ADC requires $2^7 - 1 = 127$ voltage comparators. The 8-bit PRA-ADC has 255 inverter comparators. When it is operating at 7-bit precision, every other inverter comparator is switched to the standby mode, achieving almost 50% ADC power consumption reduction. When it is operating at 6-bit precision, every three out of four inverter comparators are switched to the standby mode, achieving almost 75% ADC power consumption reduction. Subsequently the 5-bit precision results almost 87.5% power reduction. The inverter comparators' power consumption is the dominant component of the TIQ ADC power consumption, and overall power consumption is di-

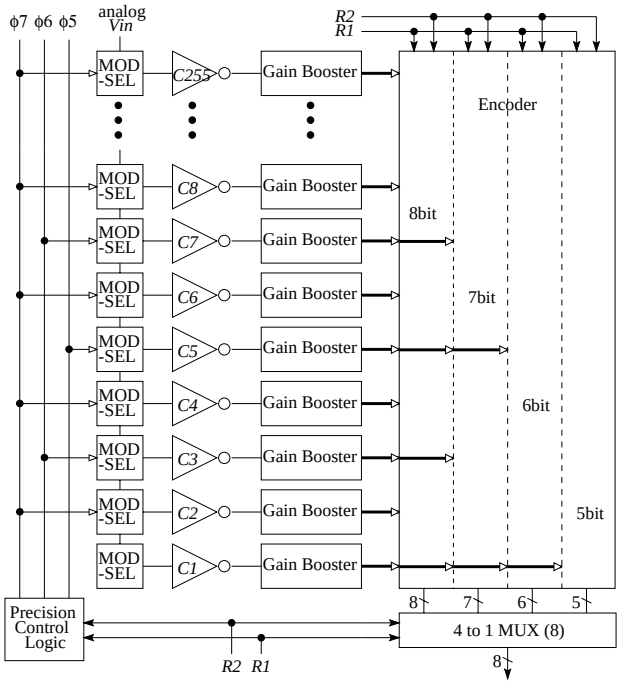

Figure 3: The power and resolution adaptive ADC

RA-ADC Precision	*R2R1*	ϕ7	ϕ6	ϕ5
8-bit	0 0	1	1	1
7-bit	0 1	0	1	1
6-bit	1 0	0	0	1
5-bit	1 1	0	0	0

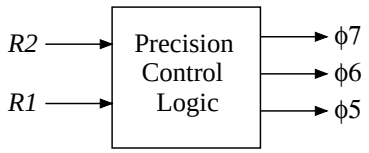

Figure 4: The precision control logic

rectly proportional to the number of active comparators at any given time.

3.1 PRA-ADC Circuit

Figure 3 shows the proposed PRA-ADC. The input signal R1 and R2 controls the ADC precision. The precision control logic unit on the lower left of Figure 3 generates the mode selection signals to selectively activate the inverter comparator. Figure 4 shows the truth table of the precision control logic.

The gain booster unit consists of a number of cascaded inverters. If the inverter comparator is in standby mode, the inverters in the gain booster unit are also in standby mode.

The authors use ROM to encode the thermometer code to binary code. Four encoders are connected in parallel, shown on the right side of Figure 3. The 8-bit encoder is a 256×8 ROM, the 7-bit encoder is a 128×7 ROM, the 6-bit encoder is a 64×6 ROM, and the 5-bit encoder is a 32×5 ROM. Appropriate ROM is selected by the precision control signals R1 and R2. Unselected ROMs are switched into the standby mode.

3.2 PRA-ADC Layout

Figure 5 shows the PRA-ADC layout using 0.18 μm CMOS design rule. Total area is $2.180mm^2$ ($345.72\mu m \times 630.48\mu m$).

The layout area overhead of adding the power and resolution adaptation feature to the fixed 8-bit TIQ ADC is 100%. The fixed 8-bit TIQ ADC consists of only the inverter comparator column, the gain booster column, and the 8-bit encoder ROM column. One can see the overhead layout area due to the mode selector column, 7-bit, 6-bit, and 5-bit encoder ROM columns in Figure 5.

4. SIMULATION RESULTS

Table 1 shows the summary of the simulation results. Power dissipation reduced by almost 50% for each resolution bit reduction. Figure 6 shows the comparison of the ideal 50% power reduction graph and the simulation results.

The third column of Table 1 shows the ADC speed increase as the resolution bit decrease. This is mainly due to the fact that the 128×7 ROM is faster than the 256×8 ROM and the 64×6 ROM is faster than the 128×7 ROM. The smaller ROM is faster than the larger ROM. Also comparing the 8-bit ADC speed and the 5-bit ADC speed, we can see the fact that the predominant signal delay is due to the encoder ROM circuit. The encoder ROM is the bottleneck of the TIQ ADCs, whereas the voltage comparators are the bottleneck in the non-TIQ ADCs.

The fourth column of Table 1 shows the mode switching overhead time. The power and resolution changes take place in less than 0.5ns, comparable to the PRA-ADC's high operating speed above 1 giga samples per second (GSPS). The PRA-ADC will suffer minimal analog signal loss during the

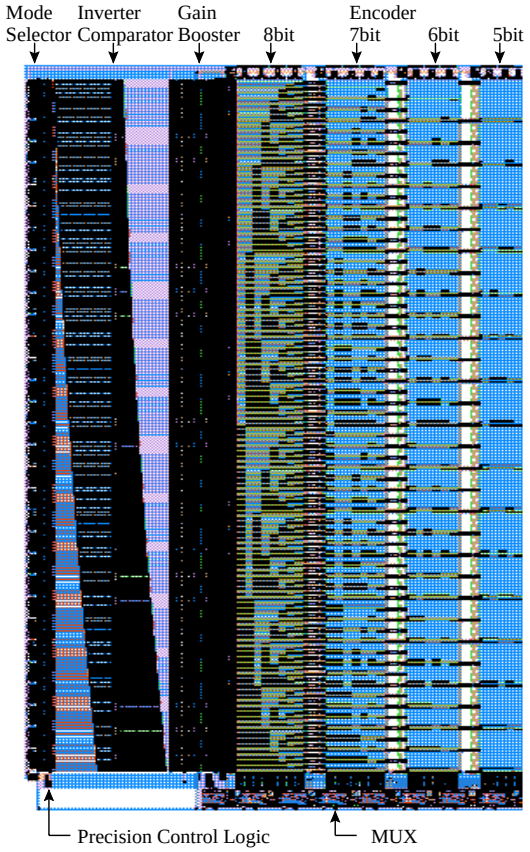

Figure 5: VLSI layout of the PRA-ADC

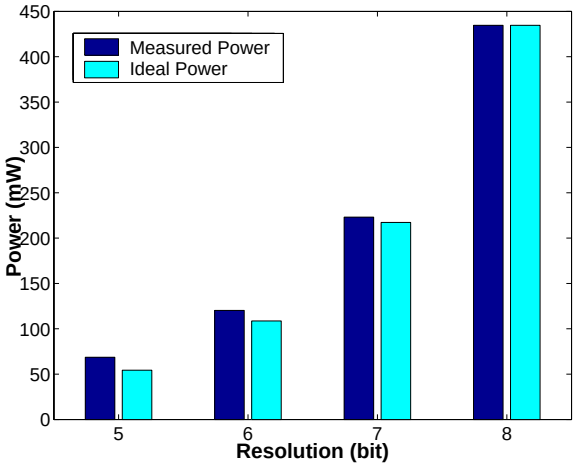

Figure 6: Power reduction comparison

Table 1: Summary of the simulation results

Resolution	Power(mW)	Speed(GSPS)	Mode switching O/H(ps)	INL(LSB)	DNL(LSB)	$V_{LSB}(mV)$
8bit	434.63	1.25	484.43 (5bit-to-8bit)	0.0347	0.0654	1.68
7bit	223.15	1.61	417.76 (8bit-to-7bit)	0.0162	0.0199	3.36
6bit	120.29	2.22	404.56 (7bit-to-6bit)	0.0025	0.0037	6.71
5bit	68.63	3.03	237.36 (6bit-to-5bit)	0.0015	0.0012	13.41

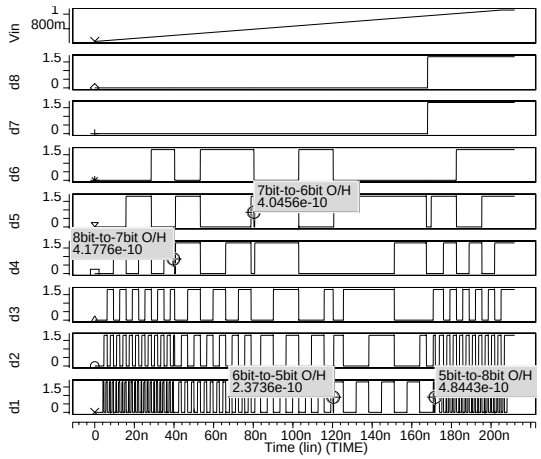

Figure 7: Resolution switching and switching overhead time

resolution change. Figure 7 shows the simulation result of the ADC resolution switching and the switching overhead times. The remaining columns in Table 1 show the linearity change and 1 LSB step voltage (V_{LSB}) change as the ADC resolution changes.

5. SUMMARY

The flash ADCs are parallel high-speed high-power ADCs, applicable in RF portable communication devices. In an effort to conserve energy, we proposed a new power and resolution adaptive flash ADC, called PRA-ADC. The PRA-ADC design allows exponential power reduction with linear resolution reduction. Unused parallel voltage comparators are switched to standby mode. The voltage comparators consume only the leakage power under the standby mode.

The PRA-ADC layout with 0.18 μm CMOS design rule show 100% area overhead. There is no noticeable performance overhead for the PRA-ADC. The voltage comparator switches between the active mode and the standby mode taking less than 0.5 ns while the ADC operates at over 1 GSPS speed. The PRA-ADC allows tighter management of power and efficiency.

The PRA-ADC is based on the TIQ flash ADC which was fabricated in 0.25 μm and 0.18 μm standard digital CMOS technology. The TIQ ADC operation has been verified up to 8-bit precision through the prototype chips.

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