±0.5V~ ±1.5V VHF CMOS LV/LP Four-Quadrant Analog Multiplier in Modified Bridged-Triode Scheme

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ABSTRACT
A new LV/LP CMOS four-quadrant analog multiplier designed in a modified bridged-triode scheme (MBTS) is presented. It brings in the benefits in terms of linearity, power consumption, frequency response and total harmonic distortion (THD). The fabricated chip in TSMC 0.35μm n-well SPQM CMOS technology has a nonlinearity error less than 0.8% over ±0.5V input range under a nominal supply voltage of ±1.5V, and consumes the total power dissipation of 2.7 mW only.

Categories & Subject Descriptors
B.7.1 **[Integrated Circuits]:** Types and Design Styles – *Algorithms implemented in hardware, Input/output circuits.*

General Terms
Design, Performance, Measurement.

Keywords
Analog multiplier, Modified Bridged-Triode Scheme (MBTS).

1. INTRODUCTION
Analog four-quadrant multiplier is a computational block for nonlinear operations on modern analog signals processing circuits, e.g., automatic gain controllers, modulators, waveform generators, etc. LV/LP (low-voltage/low-power) design has played key roles for light, long-lived mobile/hand-held portable electronics systems. Since systems-on-chip (SOC) are based on analog/digital mixed-mode VLSI signal processing, there is without doubt low-voltage/low-power design for analog CMOS circuits must be prerequisite. With the supply voltage reduction, however, many existing CMOS multipliers are faced with a serious design challenge that with a low battery while input operating voltage for a linear output signal swing becomes essential.

Conventional design technique for a CMOS analog multiplier circuit is based on the square-law characteristics of an MOS transistor [1]-[6]. A Gilbert multiplier cell [7] is first introduced in a bipolar technology, and a modified CMOS version of it is also described [8]; however, its power supply cannot be properly fitted into low voltage (≤3V) range. Few four-quadrant multipliers suitable for low supply voltages are presented in the literatures [9]-[13].

Most reported four-quadrant low voltage analog multipliers used cascoded differential input circuit to obtain larger output swing, but the architectures of the multipliers turned out to be more complicated. On the other hand, due to the complexity of the involved circuitry, they generally do not achieve a bandwidth wider than few tens of megahertz. Moreover, it should be considered that low-voltage (3V or less)/low power is a key target for such multipliers to be compatible with portable battery-operated mixed-mode VLSI systems. The four-quadrant analog multiplier presented here has been conceived as an attempt at meeting these contrasting requirements. The basic MOS four-quadrant analog multiplier first using MOS transistors operated in the triode region, used the tunable OTA proposed by Welland et al [14] as a unity-gain buffer. In this paper a low voltage CMOS four-quadrant analog multiplier with a modified bridged-triode scheme (MBTS) is presented. The multiplier can work appropriately under a lower supply voltages down to ±0.5V with desired linearity persisted. Description of MBTS in the proposed multiplier is given in Section 2. In Section 3, moreover frequency response, the effects of transistor nonlinearities, including mobility degradation and mismatches on threshold voltage and transconductance are analyzed. Varied offset-induced amplitude modulations related to DC levels in the both carrier and modulation input signals are also elucidated together with simulation results in Section 4. Prototype chip experimental results are reported in Section 5. Then a conclusion is made finally.

2. DESCRIPTION OF ANALOG MULTIPLIER IN MBTS
Fig. 1 shows the proposed low voltage CMOS four-quadrant multipliers, based on the modified bridged-triode scheme (MBTS). The MBTS in the multiplier is constructed into three subcircuits as following: input function by three complementary source followers (C.S.F.) in a push-pull form [15~17], signal multiplication section by two bridged NMOS transistors (i.e. M_5 and M_6) biased in the triode region mainly and output system by two load resistors strayed from the link of two symmetry current mirrors M_{1B} (M_{1E}) and M_{2B} (M_{2E}) for differential purpose. The MBTS multiplier bridge three symmetric complementary push-pull input source followers via two triode MOS, and so offer straight signal paths between two differential inputs and two triode-operated multiplying devices. It earns to bear the returns in better performances of linearity, power consumption, frequency response and total harmonic distortion (THD). The bias circuits for each input signal V_1 and V_2 in complementary source followers (C.S.F.) is formed by both P-Bias and N-bias as illustrated in Fig. 1. V_1 is input voltage delivered into the gates of both M_1 and M_2 in the

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complementary push-pull source followers, therefore source voltage of C.S.F. will pursue back to V_1. As the output node of C.S.F revealed in Fig.1, drain (source) voltage of M_5 and M_6 would track back to V_1 (V_2) in its certain way.

It is seen that in the region where the output of complementary push-pull source follower is between V_{Tp} and V_{Tn} there will be a "dull zone" wherein both transistors will be in cut-off region. In this region the voltage gain of both M_1 and M_2 is very small, the circuit therefore suffers from an important type of distortion well known as crossover distortion. This type of distortion is due to the almost nonexistent gain of the transistors in the cutoff region. To bring the voltage gain up toward unity for small input signal, it is necessary to bias the transistors with a small quiescent current so as to bias the transistors at a point that is slightly into the active region. This can be done by applying a small DC bias voltage between the gates of the two transistors, as shown in Fig. 1. To minimize the crossover distortion [15~17], the bias voltage in the P-Bias and N-Bias circuits must be sufficiently large to bias M_1 and M_2 enough in to the active region to ensure that the source follower voltage gain close to unity, even under quiescent condition (V_{in} = 0 and V_o = 0). The total bias voltage required between the two gates is in the range of about the sum of threshold voltage of complementary transistors, V_{Tp} + V_{Tn}. This bias condition assures that there is no crossover distortion at the input, and that all two input devices are conducting a small standby current with V_{in} = 0.

Neglecting the channel-length modulation, the mobility degradation (due to high field and short channel) and the body effect. The drain current I_D for two bridged NMOS transistor biased in the triode region can be given as

$$I_{D5} = \beta\left[\left(V_{GS5} - V_{Tn}\right)V_{DS5} - \frac{1}{2}V_{DS5}^{2}\right] \quad (1a)$$

$$I_{D6} = \beta\left[\left(V_{GS6} - V_{Tn}\right)V_{DS6} - \frac{1}{2}V_{DS6}^{2}\right] \quad (1b)$$

Where β and V_{Tn} is the transconductance and the threshold voltage of two bridged-triode NMOS devices (M_5 and M_6) shown in the proposed circuits. V_G is adjustable bias voltage for operating M_5 and M_6 in triode region. V_G–sub is p-type voltage subtractor [18~20] referred as bias circuit for input voltages (V_3 and V_4) into gate of M_5 and M_6 indicated in Fig. 1. The drain-source voltage of M_5 and M_6 can be expressed by

$$V_{DS5} = V_1 - V_2 = V_{DS6} \quad (2)$$

Hence, the drain-source voltage of M_5 and M_6 is equal to the difference between input signal V_1 and V_2. Therefore, the drain currents for M_5 and M_6 operated in the triode region can be rewritten as

$$I_{D5} = \beta\left[\left(V_3 + V_G - V_2 - V_{Tn}\right)\left(V_1 - V_2\right) - \frac{1}{2}\left(V_1 - V_2\right)^{2}\right] \quad (3a)$$

$$I_{D6} = \beta\left[\left(V_4 + V_G - V_2 - V_{Tn}\right)\left(V_1 - V_2\right) - \frac{1}{2}\left(V_1 - V_2\right)^{2}\right] \quad (3b)$$

Since load resistor (R_L) has the same current mesh loop topology as the bridged-triode NMOS (M_5 and M_6) does in symmetry current mirror branch as shown in Fig. 1, any output currents I_{O+} and I_{O-} flow into each load resistor will be regarded as a direct reflection of drain current I_{D5} and I_{D6} in M_5 and M_6 two bridged-triode NMOS, respectively. According to eqns. (3a) and (3b), the difference between the drain currents of M_5 and M_6 will be proportional to the product of the drain-source voltage (V_1–V_2) and the difference of their gate voltages (V_3–V_4).

$$I_O = I_{O^+} - I_{O^-} = I_{D5} - I_{D6} = \beta\left[\left(V_1 - V_2\right)\left(V_3 - V_4\right)\right] \quad (4)$$

Consequent output voltage difference owing to drain currents I_{D5} and I_{D6} flow through each R_L is equal to

$$V_O = V_{O^+} - V_{O^-} = R_L\left(I_{D5} - I_{D6}\right) \quad (5)$$

Hence multiplier function results when the above currents are sourced into load resistors R_L. The differential output voltage V_O of multiplier can be expressed as

$$V_O = R_L\beta\left[\left(V_1 - V_2\right)\left(V_3 - V_4\right)\right] = R_L\beta V_X V_Y \quad (6)$$

V_X and V_Y are alleged to be two differential input signals as (V_1–V_2) and (V_3–V_4), respectively. Thus four-quadrant operation in multiplying two differential signal variables V_X and V_Y is obtained. The voltage swing of the output can be adjusted by simply gain facto $R_L\beta$. Note that the substrate of M_5 and M_6 must connect to V_{SS} to allow bi-directional currents flow in the modified bridged-triode scheme. To ensure triode operation of transistors M_5 and M_6 the following constraints should be satisfied:

$$max\left(V_1, V_2\right) < min\left(V_3, V_4\right) + V_G - V_{Tn} \quad (7)$$

3. NONIDEAL EFFECTS AND FREQUENCY RESPONSE

Main nonideal contributions that affect the circuit's accuracy are due to the mobility degradation and to mismatches of both the transconductance and threshold voltages factors, while the body effect can be overcome if a p-well process is available. It is true for the two transistors in the triode region. However, those complementary transistors of the push-pull source followers on both sides will tend to compensate and minimize the nonideal error as introduced from the fact the effect of bulk-source voltages are opposite polarity. Surface mobility degradation generally has more significant impacts in saturation-based MOS than triode-based ones for high field and short channel effect. Hence mobility reduction effect will not be further discussed in our design of the bridged triode-based analog four-quadrant multiplier.

3.1 Nonideal Effects

Due to these nonidealities, the output current differs from that given by (4), and can be represented by

$$I_O = \beta V_X V_Y + \Delta I_{NI} \quad (8)$$

Where term ΔI_{NI}, difference of I_O from nominal value $\beta V_X V_Y$, represents the nonlinearities error introduced by the nonideal effects on the multiplier function. In order to evaluate the accuracy of the circuit, and to well understand the effects of each nonideality, we will determine deviation parameters ΔI_{NI}, for each single source of error.

The operating function of the proposed MBTS multiplier is based directly on the inherent factual multiplication of two separate voltage signals V_{GS} and V_{DS} in the MOS triode current equation. Generally, the square law of MOS transistor deviates from an ideal square law in the case of large drain current, strong gate field, and small channel length. This is due to the velocity saturation, the mobility degradation, and the short-channel effect. Providing the proper conditions for which these problems can be neglected is the key point in the design of the chip. Large signal nonidealities of the multiplier arise from many sources and reflect themselves as nonlinearities and harmonic distortions. Compared to conventional square-law-based multipliers that rely on accurate transistor matching to cancel second-order terms [21], triode-based multipliers make use of the inherently linear relationship between I_D and V_{GS} of a MOS transistor in the linear region. Thus, triode-based multiplier can tolerate mismatch without a significant increase in distortion. If the components are completely matched devices, the main causes of nonlinearities are the channel length

modulation and mobility reduction effects. The effect of channel length modulation can be greatly suppressed by using a regulated cascade (RGC) circuit [9]. While deriving (4), mobility reduction effect was neglected. In presence of this effect, (9) can be express in a Taylor series of the form

$$I_{O+} - I_{O-} = a_1 V_{in} + a_3 V_{in}^{\,3} + a_5 V_{in}^{\,5} + \cdots\cdots \quad (9)$$

Clearly the mobility reduction effect manifests itself as odd harmonics. The major contributor to the nonlinearity is a_3 / a_1,

$$\frac{a_3}{a_1} = \frac{\theta^2}{4\left[1+\theta\left(V_{CM}-V_{Tn}\right)\right]^2} \quad (10)$$

Where θ is the mobility reduction coefficient and V_{CM} is the common mode input voltage. In (10) it suggests that, as the common mode gate-source voltage decreases the distortion increases, which is the case for low voltage circuits. However, $\theta\,(V_{CM}-V_{Tn})$ is much smaller than unity, causing little increase in distortion. It is instructive to compare the above nonlinearity term from the triode MOS to that from saturated MOS. The ratio of relative distortion term α is defined as [22]

$$\alpha = \frac{\left|\frac{a_3}{a_1}\right|_{sat}}{\left|\frac{a_3}{a_1}\right|_{tri}} = \frac{1}{\theta\left(V_{CM}-V_{Tn}\right)\left[2+\theta\left(V_{CM}-V_{Tn}\right)\right]^2} \quad (11)$$

It should be noted that the input common voltages are assumed to be the same for both cases. From (11), if V_{CM} is low for small enough θ, the triode MOS introduces less distortion. In fact, for the proposed multiplier α is about 9, meaning much smaller distortion can be obtained by triode MOS in such bridged structure.

3.1.1 Mismatch error on β

Device mismatches due to process variations on the device aspect ratio, on the mobility as well as in the oxide thickness give rise to mismatch in the transconductance parameter. In order to evaluate it one should consider a variation of β in those bridged-triode transistors (e.g. M_5, M_6). (1a) and (1b) can be written as

$$I_{D5} = \left(\beta+\Delta\beta_5\right)\left[\left(V_{GS3}-V_{Tn}\right)\left(V_X\right) - \frac{1}{2}V_X^{\,2}\right] \quad (11a)$$

$$I_{D6} = \left(\beta+\Delta\beta_6\right)\left[\left(V_{GS4}-V_{Tn}\right)\left(-V_X\right) - \frac{1}{2}V_X^{\,2}\right] \quad (11b)$$

So the output current, I_O, is

$$\begin{aligned} I_O &= I_{D5} - I_{D6} \\ &= \beta V_X V_Y + \left(\Delta\beta_5 - \Delta\beta_6\right)\left[\left(V_G - V_2 - V_{Tn}\right)V_X - \frac{1}{2}V_X^{\,2}\right] \\ &\quad + \left(\Delta\beta_5 V_3 - \Delta\beta_6 V_4\right)V_X \end{aligned} \quad (12)$$

By comparing (12) to (8), one can obtain the corresponding ΔI_{NI} as

$$\begin{aligned} \Delta I_{NI} &= \left(\Delta\beta_5 - \Delta\beta_6\right)\left[\left(V_G - V_2 - V_{Tn}\right)V_X - \frac{1}{2}V_X^{\,2}\right] \\ &\quad + \left(\Delta\beta_5 V_3 - \Delta\beta_6 V_4\right)V_X \end{aligned} \quad (13)$$

3.1.2 Mismatch error on the threshold voltage

In order to evaluate the effect of mismatch error on the threshold voltage one should consider a variation on the threshold voltage in bridged-triode NMOS (M_5 and M_6). (1a) and (1b) can be expressed as

$$I_{D5} = \beta\left[\left(V_{GS3}-V_{Tn}-\Delta V_{Tn5}\right)V_X - \frac{1}{2}V_X^{\,2}\right] \quad (14a)$$

$$I_{D6} = \beta\left[\left(V_{GS4}-V_{Tn}-\Delta V_{Tn6}\right)V_X - \frac{1}{2}V_X^{\,2}\right] \quad (14b)$$

The output current, I_O, becomes

$$I_O = \beta V_X V_Y - \beta\left(\Delta V_{Tn5} - \Delta V_{Tn6}\right)V_X \quad (15)$$

Again, by comparing (15) to (8), one should find the corresponding term ΔI_{NI}, of the output current is given by

$$\Delta I_{NI} = -\beta\left(\Delta V_{Tn5} - \Delta V_{Tn6}\right)V_X \quad (16)$$

As for (13) and (16), the above terms which deviate from the nominal term by multiplier function of $\beta V_X V_Y$ are the contributions of nonideal errors due to transconductance and threshold voltage mismatch, respectively. For both inputs of dc 0.5V, the magnitude of the output error due to each error source has been simulated using the circuit simulator HSPICE with level 49 MOS model parameters of TSMC (Taiwan Semiconductor Manufacturing Corporation) 0.35μm standard CMOS process. The complementary push-pull source-follower stage gives about 0.2% error as described before. The 1% mismatches in the transconductance parameters of the bridged-triode transistors and the output resistors gives maximum errors of 0.16% and 1.1%, respectively.

3.2 Temperature Dependence

The gain factor of the multiplier depends on temperature through $R_L\beta$. The temperature coefficients of β and R_L are negative and positive, thus some cancellation is expected. To cancel the gain variation for a wider temperature range, the output resistors can be replaced with equivalent MOS resistors where $R_{\mathrm{MOS}} \propto [\beta(V_{GS}-V_{Tn})]^{-1}$ [23]. If the gate-to-source voltage of the equivalent MOS resistor is sufficiently large so that the effect of the threshold-voltage variation with temperature can be neglected, the temperature dependence of the gain factor $R_L\beta$ can be canceled directly. Therefore the temperature-compensated gain factors can be achieved, although the gain may be reduced to the small MOS resistance with a large gate-to-source voltage.

3.3 Frequency Response

The one-stage complementary source follower (C.S.F.) has one output node with no internal alternating current node, accordingly the frequency response is hardly degraded for the reason that C.S.F. is a unity gain buffer featuring a low-impedance characteristic. [15~17] The same argument holds for multiplication stages, through which signals flow to the output. Therefore, the frequency performance for MBTS analog multiplier could be enhanced. The dominant pole determines the frequency behavior of the multiplier circuit in Fig. 1 is given by

$$P_d = \frac{1}{R_O C_O} \quad (17)$$

Where

$$R_O = \left|\frac{1}{g_{ds5}} - \frac{1}{g_{ds6}}\right| \quad (18)$$

, And

$$C_O = C_{gs5} + C_{gs6} + C_{bs5} + C_{bs6} \quad (19)$$

In (18) and (19), g_{ds} represents the small-signal drain conductance parameter of the MOS transistor in the saturation region and C_{gs} and C_{bs} represent gate-to-source and bulk-to-source capacitance, respectively. The independent output nodes of the complementary push-pull source follower on both sides determine the frequency response of the proposed circuits. However the frequency is hardly degraded because each source node correlated with complementary push-pull source followers

distinguishes a merit of lower impedance. As shunted by the high output resistance of current mirrors, the frequency behavior of the overall circuits is exclusively reflected by the currents of push-pull source node of input stage flowing through the small load resistance, and will be least deteriorated either. Thus, the frequency response for this configuration of the proposed multiplier with such symmetry complementary source followers in MBTS is admirable.

4. SIMULATION RESULTS

The MBTS analog multiplier circuit in Fig. 1 was simulated with HSPICE *BSIM* level 49, 0.35μm N-well single–poly-quad–metal (SPQM) CMOS technology with the nominal parameters: V_{Tn}= 0.75V, V_{Tp}= –0.85V, K_n= 98.1μA/V^2, K_p= 33.61μA/V^2, θ_n= 0.078V^{-1} and θ_p= 0.12V^{-1}. The aspect ratios for all transistors denoted as sub-blocks in Fig. 1 are listed in Table I. All simulations were performed with power supply voltages of ±1.5V, R_L=1kΩ, common mode voltage V_G=1.2V and with all NMOS transistors sharing the same bulk, connected to V_{SS}. The load resistors can be characterized using the n-type polysilicon layer. The polysilicon is preferred as a load element because it has higher frequency response and larger signal swing than the active load. A better swing can be achieved by an optimized common mode value. The typical DC transfer curve of the proposed MBTS multiplier under four low supply voltages are given in Fig. 2. Similar curves were obtained by interchanging V_1–V_2 and V_3–V_4. The circuit has less than 0.8% nonlinearity error over a ±0.5V differential input operating voltage swing as shown in Fig. 2(a). While the supply battery voltage goes down to ±1V, the output voltage swing can be enhanced to the same level as battery voltage of ±1.5V simply by increasing the load resistance R_L from 1kΩ to 100kΩ without redesign the all the aspect ratio of MOS in the multiplier. As the supply battery voltage goes lower to ±0.5V, output swing still be able to enhanced merely by adjusting external load impedance and nonlinearity error in which could be confined under the desired range as shown in Fig. 2(c). Fig. 2(d) indicates that the output swing and linearity of the multiplier is hard to maintain the same standard as in Fig. 2(a)~(c) for extremely high load impedance when a very low battery is in nearly one-sevenths of original full battery supply. Since MBTS multiplier provides two straight signal paths for differential inputs (V_1–V_2) and (V_3–V_4) into drain/source and gate terminals of two multiplication devices accordingly, via three symmetric complementary push-pull source followers and two triode MOS directly. The output of complementary push-pull source follower can be regarded as "virtual-direct input" for the input signal of complementary push-pull source follower. So long as the output of complementary push-pull source follower ("virtual-direct input") can maintain its linear function of differential input in standby condition, despite the supply voltage from ±1.5V down to ±0.5V. Consequently any current fluctuation in drain current I_{D5} and I_{D6} of two bridged-triode NMOS (M_5 and M_6) due to two virtual-direct differential inputs (V_1–V_2) and (V_3–V_4) variation in the terminals of drain/source and gate in triode MOS will unswervingly replicate the same variation on the output currents flow in the course of two load resistors. The body effect of M_5 and M_6, nevertheless, may cause the threshold voltage shift and introduce linearity error in the output current. While supply voltage lower from ±1.5V (Fig.2(a)) to ±1V (Fig.2(b)) (down to ±0.5V (Fig.2(c))), the total power dissipation of MBTS multiplier goes also from 2.7mW, to 5.2μW (down to 7.1nW). For a 30kHz differential signal having 0.5V peak amplitude applied to V_1–V_2, with V_3–V_4 held constant at 0.5V, the output voltage has a THD (Total Harmonic Distortion) less than 1%. It brings in the advantages in terms of linearity, low voltage/low power consumption, frequency response and total harmonic distortion (THD). Therefore the proposed analog multiplier is expected to be suitable for VHF analog communication signal processing. The major characteristics of MBTS analog multiplier are summarized in Table II.

4.1 Offset-Induced Amplitude Modulation

Fig. 3 shows the various amplitude modulation output waveforms with a 1Vp-p, 1kHz triangular signal applied to V_3–V_4, and 1Vp-p, 10kHz sinusoidal signal to V_1-V_2.

$$V_{AM} = (V_C + V_{OC})(V_M + V_{OM}) \quad (20)$$

Where V_C and V_M correspond to carrier input and modulation (audio) input signals. V_{OC} (V_{OM}) represents DC offset in carrier input (modulation) input signal. Fig. 3(a) and (b) show 100% and partial amplitude modulation, a common ground between which is without offset in carrier input signal. However, an offset-induced 100% amplitude modulation waveform resulted from introducing nonzero DC offset in carrier signal. With concerned nonzero DC offsets in both carrier and modulation input signal, offset-induced partial amplitude modulation took place in Fig. 3(d) as well.

5. EXPERIMENTAL RESULTS

A tested chip of the circuit in Fig. 1 was fabricated through CIC in TSMC 0.35μm n-well SPQM CMOS technology. Two 1kΩ resistors as a loading element were connected to the output of tested chip. Dual supplies of ±1.5V and V_G=1.2V were used. Fig. 4 shows the experimental V_O against V_1-V_2 characteristics for constant values V_3–V_4=±0.05V and ±0.075V. The linearity error is less than 1% over a ±0.15V differential input range. The measured total harmonic distortion with 1V(peak) input signal at either input terminal with ±0.5V DC voltage at the other terminal is less than 1% for frequencies up to 180MHz.

Fig. 5 shows the measured output waveforms with 1Vp-p 100kHz sinusoidal and 2.5kHz triangular input signals. A phase shift was noticed in the modulation process as compared with the lower triangular sign (negative amplitude) in Fig. 5, which was ascribed to be a nonzero DC offset in both the carrier signal (100kHz) and modulation signal (2.5kHz). It is the property of an offset-induced partial amplitude modulation that was described in Fig. 3(d). A partial modulation waveform without the phase shift can be obtained if DC offset of the carrier signal is set to be zero, as shows in Fig. 6. This modulation process has a same way as mentioned in Fig. 3(b).

6. CONCLUSIONS

The low-voltage/low-power MBTS in the CMOS analog multiplier reported in this paper. This efficient structure of MBTS multiplier yields the benefits in performance of linearity, power consumption, frequency response and total harmonic distortion (THD). Even under a low battery supply voltage reduce to ±0.5V, the proposed scheme can keep the multiplier work well with proper nonlinearity remains solely by increasing external load resistance without resizing the aspect ratio of transistors in the entire circuit. The proposed modified bridged triode scheme in analog signal processing cell design is more suitable for low-voltage/low-power operation and expected to be useful in analog VLSI signal processing systems.

REFERENCES

[1] H. Wallinga and K. Bult, "Design and analysis of CMOS analog signal processing circuits by means of a graphical MOST model," *IEEE J. Solid-State Circuits*, Vol. SC-24, pp. 672-680,

June 1989.
[2] J. Pena-Finol and J. Connelly, "An MOS four-quadrant analog multiplier using the quarter-square technique," *IEEE J. Solid-State Circuits*, Vol. SC-22, pp. 1064-1073, Dec. 1987.
[3] Z. Wang, "A CMOS four quadrant analog multiplier with single ended voltage output and improved temperature performance," *IEEE J. Solid-State Circuits*, Vol. SC-26, pp. 1293-1301, 1991.
[4] S. L. Wang, *et al.*,"Wide dynamic range four-quadrant CMOS analog multiplier using linearized transconductance stage," *IEEE J. Solid-State Circuits*, Vol. SC-21, pp. 1120-1122, 1986.
[5] H. Song and C. Kim, "An MOS four-quadrant analog multiplier using simple two-input squaring circuits with source followers," *IEEE J. Solid-State Circuits*, Vol. SC-25, pp. 841-848, June 1990.
[6] C. Kim and S. Park, "Design and implementation of a new four-quadrant MOS analog multiplier," *J. Analog Integrated Circuits and Signal Processing*, Vol. 2, pp. 96-103, 1992.
[7] B Gilbert, "A high-performance monolithic multiplier using active feedback," *IEEE J. Solid-State Circuits*, Vol. SC-9, pp. 267-276, Dec. 1974.
[8] S. Qin and R. Geiger, "A ±5V CMOS analog multiplier," *IEEE J. Solid-State Circuits*, Vol. SC-22, pp. 1143-1146, Dec. 1987
[9] J. H. Jsay, S. I. Liu, J. J. Chen, and Y. P. Wu, "CMOS four-quadrant multiplier using triode transistor based on regulated cascade structure," *Electron. Lett.,* Vol. 31, pp. 962-963, 1995.
[10] A. L. Coban and P. E. Allen, "Low-Voltage, four-quadrant analogue CMOS multiplier," *Electron. Lett.*, Vol. 30, pp. 1044-1045, 1993.
[11] J. Ramirez-Angulo, "Highly linear four-quadrant analogue BiCMOS multiplier for ±5V supply operation," *Proc. IEEE Int. Symp. Circ. Syst*., pp. 1467-1470, 1993.
[12] E. Sackinger and W. Guggenbuhl, "A high-swing, high impedance MOS cascade circuit," *IEEE J. Solid State Circuits*, Vol. SC-25, pp. 289-298, Feb. 1990.
[13] S. C. Li, "A Symmetric Complementary Structure for RF CMOS Analog Squarer and Four-Quadrant Analog Multiplier," *J. Analog Integrated Circuits and Signal Processing*, Vol. 23, No. 2, pp.103~115, 2000.
[14] D. R. Welland *et al*, "A digital read/write channel with EEPR4 detection," *Solid-State Circuits Conference*, 41st ISSC, pp. 276 – 277, 1994.
[15] A. B. Greben, Bipolar and MOS analog integrated circuit design, John-Wiley & Sons: New York, 1984, pp. 297~299.
[16] S. Soclof, Design and applications of analog integrated circuits, Prentice-Hall: New Jersey, 1991, pp. 590~639.
[17] P. E. Allen and D. R. Holberg, CMOS analog circuit design, Holt, Rinehart and Winston: New York, 1987, pp. 302~304.
[18] P. L. Langlois, "Comment on 'A CMOS four-quadrant multiplier': effect of threshold voltage," *IEEE J. Solid State Circuits*, Vol. 25, No. 6, pp. 1595-1597, 1990.
[19] K. Bult and H. Wallinga, "A CMOS four-quadrant analog multiplier," *IEEE J. Solid State Circuits*, SC-21, pp. 430-435, 1986.
[20] S. C. Li, K. L. Lin, and W. C. Hong, "3GHz ±1V CMOS analogue squarer for nonlinear signal processing," *Int. Symp. of Nonlinear Theory and Its Applications (NOLTA' 97)*, Vol. 2, Hawaii, pp. 787-790, 1997.
[21] S. Sakurai and M. Ismail, High frequency wide range CMOS analog multiplier, *Electron. Lett.*, Vol.28, pp. 2228-2229, 1992.
[22] B. Nauta, Analog CMOS Filters for Very High Frequencies, Kluwer Academic Publishers: Massachusetts, 1993.
[23] M. Banu, and Y. P. Tsividis, "Floating voltage-controlled resistor in CMOS technology," *Electron. Lett.*, Vol. 18, pp. 678-679, 1982.

Table I
Aspect ratios of sub-blocks of MBTS multiplier in Fig. 1

	C.S.F	P-Bias	N-Bias	Current -Mirror	Bridged-Triode MOS

MOS	M_1	M_2	M_{3N}	M_{4N}	N_{3P}	M_{4P}	N	P	M_5, M6
$\frac{W}{L}$	$\frac{120}{0.4}$	$\frac{200}{0.4}$	$\frac{200}{0.4}$	$\frac{20}{20}$	$\frac{0.4}{20}$	$\frac{200}{0.4}$	$\frac{100}{0.4}$		$\frac{50}{0.4}$

Table II
Major Specs of MBTS analog multiplier in Fig. 1.

Power supplies	**±1.5V**
Nonlinearity error ($\|V_X\|$, $\|V_Y\|$ ≤0.5V)	**≤ 0.8%**
Total harmonic distortion	**≤ 1%**
-3dB bandwidth	**180~260MHz**
Input operating swing	**1Vp-p**
Static power dissipation	**2.69mW**
Total input equivalent noise (f =30kHz)	**90nV/ $\sqrt{Hz}$**
Total output noise (f =30kHz)	**16nV/ $\sqrt{Hz}$**

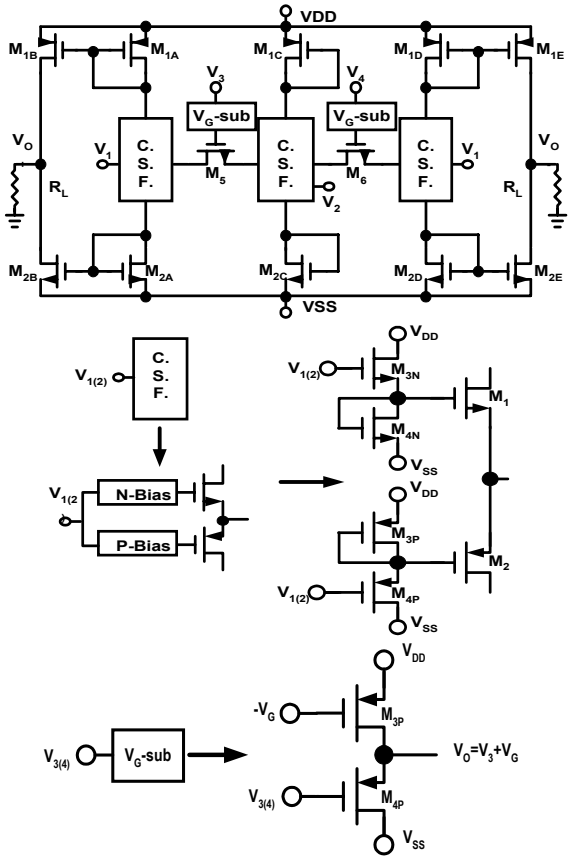
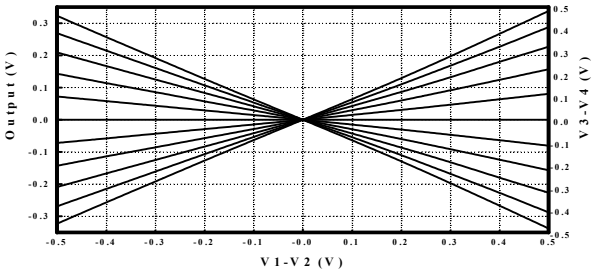
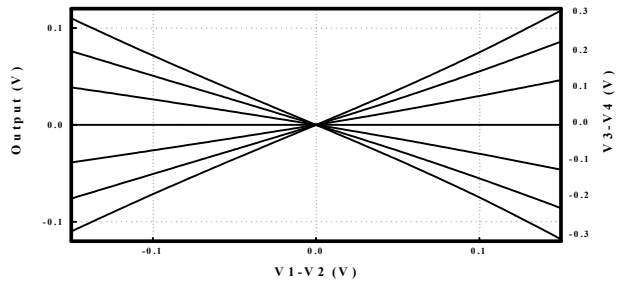


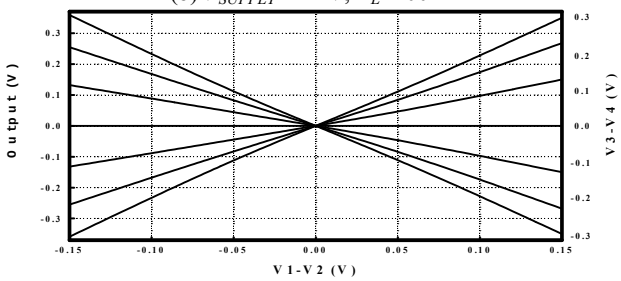
Fig. 1 MBTS realization of CMOS LV/LP four-quadrant analog multiplier.



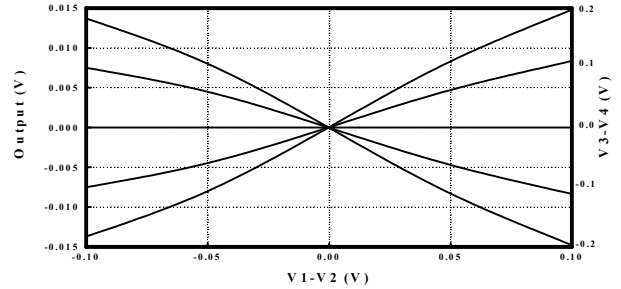
(a) V_{SUPPLY} = ±1.5V, R_L=1kΩ



(b) V_{SUPPLY} = ±1V, R_L=100kΩ

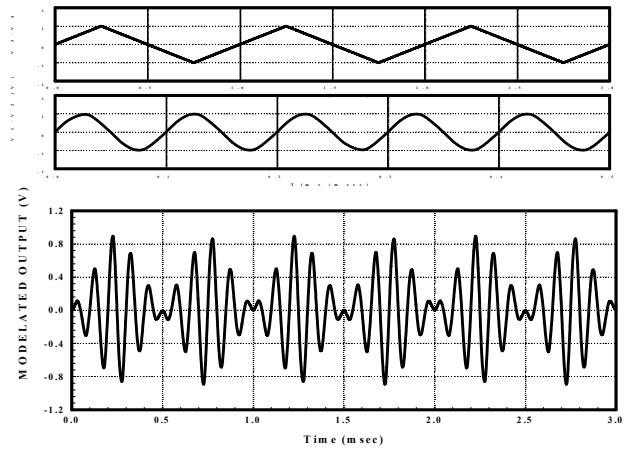


(c) V_{SUPPLY} = ±0.5V, R_L=100MΩ

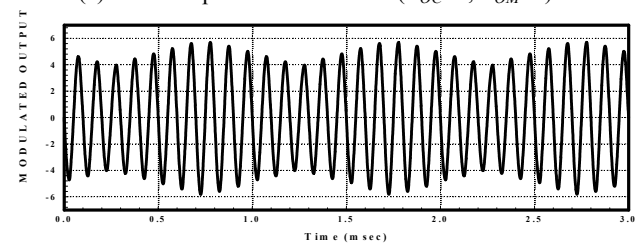


(d) V_{SUPPLY} = ±0.2V, R_L=1GΩ

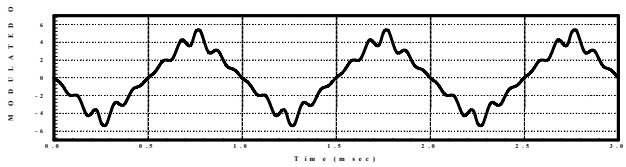
Fig. 2 Simulated DC transfer characteristics for varied low supply voltages (V_{SUPPLY}) and adjustable external load (R_L).



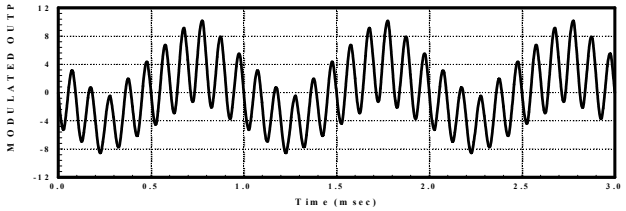
(a) 100% amplitude modulation. (V_{OC}=0, V_{OM}=0)



(b) Partial amplitude modulation. (V_{OC}=0, V_{OM} ≠0)



(c) Offset-induced 100% modulation. (V_{OC} ≠0, V_{OM} =0)



(d) Offset-induced partial modulation. (V_{OC}≠0, V_{OM} ≠0)

Fig. 3 1kHz triangular (modulation) and 10kHz sinusoidal (carrier) signal amplitude modulation. (a) 100% without offsets in both carrier and modulation input signal. (b) Partial modulation. (c) Offset-induced 100% amplitude modulation with nonzero carrier signal DC offset. (d) Offset-induced partial amplitude modulation with nonzero DC offset in both carrier and modulation input signals.

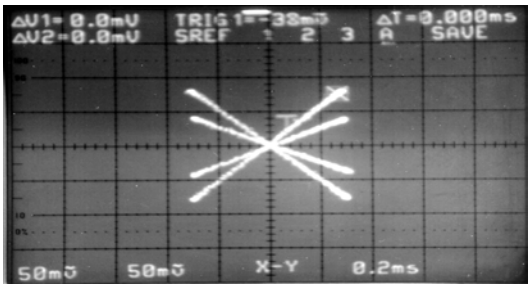


Fig. 4 Measured DC transfer curves with V_3–V_4= ± 0.15V for R_L=1kΩ.

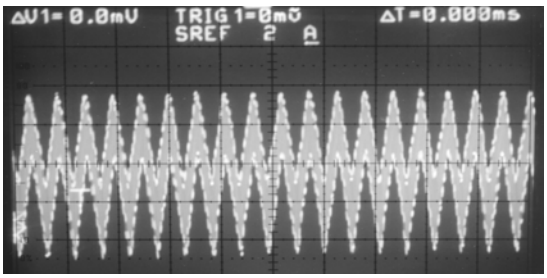


Fig. 5. Offset-induced partial amplitude modulation output signal due to DC offsets in both 2.5kHz triangular and 150kHz sinusoidal signals.

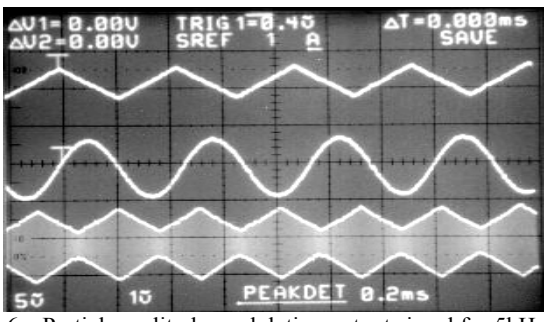


Fig. 6 Partial amplitude modulation output signal for 5kHz triangular and 100kHz sinusoidal input signals.