

ACM SIGDA Publications on CDROM

ISLPED'02

The Monterey Beach Hotel Resort

Monterey, California

August 12-14, 2002

Copyright © 2002 by the Association for Computing Machinery, Inc. (ACM). Permission to make digital or hard copies of portions of this work for personal or classroom use is granted without fee provided that copies are not made or distributed for profit or commercial advantage and that copies bear this notice and the full citation on the first page. Copyright for components of this work owned by others than ACM must be honored. Abstracting with credit is permitted. To copy otherwise, to republish, to post on servers or to redistribute to lists, requires prior specific permission and/or a fee. Request permission to republish from: Publications Dept., ACM, Inc. Fax +1 (212) 869-0481 or <permissions@acm.org>.

For other copying of articles that carry a code at the bottom of the first or last page, copying is permitted provided that the per-copy fee indicated in the code is paid through the Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

ISBN # 1-58113-595-5

ACM Order is 477026.

Click on the text below to go to:

Table of Contents

Front Matter

Author Index

Cover Page

CD-ROM produced by ACM SIGDA CD-ROM Project.

ISLPED'02

Proceedings of the
2002
**International Symposium
on Low Power Electronics
and Design**

**Monterey Beach Hotel Resort
Monterey, California, USA
August 12-14, 2002**

Sponsored by

ACM SIGDA and IEEE Circuits and Systems Society

with technical co-sponsorship from

the IEEE Solid-State Circuits Society

and

the IEEE Electron Devices Society



Title page not received in time for publication

**The Association for Computing Machinery
1515 Broadway
New York, New York 10036**

Copyright © 2002 by the Association for Computing Machinery, Inc. (ACM). Permission to make digital or hard copies of portions of this work for personal or classroom use is granted without fee provided that copies are not made or distributed for profit or commercial advantage and that copies bear this notice and the full citation on the first page. Copyright for components of this work owned by others than ACM must be honored. Abstracting with credit is permitted. To copy otherwise, to republish, to post on servers or to redistribute to lists, requires prior specific permission and/or a fee. Request permission to republish from: Publications Dept., ACM, Inc. Fax +1 (212) 869-0481 or <permissions@acm.org>.

For other copying of articles that carry a code at the bottom of the first or last page, copying is permitted provided that the per-copy fee indicated in the code is paid through the Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923.

Notice to Past Authors of ACM-Published Articles

ACM intends to create a complete electronic archive of all articles and/or other material previously published by ACM. If you have written a work that has been previously published by ACM in any journal or conference proceedings prior to 1978, or any SIG Newsletter at any time, and you do NOT want this work to appear in the ACM Digital Library, please inform permissions@acm.org, stating the title of the work, the author(s), and where and when published.

ACM ISBN: 1-58113-475-4

Additional copies may be ordered prepaid from:

ACM Order Department
PO Box 11405
New York, NY 10286-1405

Phone: 1-800-342-6626
(US and Canada)
+1-212-626-0500
(all other countries)
Fax: +1-212-944-1318
E-mail: acmhelp@acm.org

ACM Order Number 477024
Printed in the USA

Foreword ISLPED Proceedings

Future Perspectives

Charles F. Kettering, American Inventor

"My interest is in the future, because I am going to spend the rest of my life there"

After the well-known speed and area constraints, the ISLPED main focus on low power design, is certainly the new challenge in the design of integrated circuits. The design of nearly one billion transistor chips, down to 0.10 μm and below, supplied at less than 1 Volt but working at some GHz, is a very challenging task, certainly considered as an impossible task only some years ago. The design of such chips seem miraculous, but, as pointed out by:

Thomas Edison, LIFE, 1932

"Genius is one percent inspiration and ninety-nine percent perspiration"

The microelectronic revolution is fascinating; 55 years ago, in late 1947, the transistor was invented by William Shockley, John Bardeen and Walter H. Brattain, Bell Telephone Laboratories, which received the Nobel Prize in Physics in 1956. Everybody knows as the story continues: MOS technology, the first microprocessor in 1971, CISC machines, RISC microprocessors in 1981, superscalar and VLIW machines today, with a shift in CMOS technology in 1984-1985 with the 80386 and 68020.

Unknown engineer

"The best way to predict the future is to invent it"

The 2001 SIA Roadmap predicts in 2016 a 0.022 μm CMOS process (probably SOI) with 16 billions of transistors for high-performance chips, 0.4 Volt, 288 watts and 28 GHz as local frequency. As a result, there are today more transistors in the world (10^{17}) than ants (10^{16}).

William Bragg

"The important thing in science is not so much to obtain new facts as to discover new ways of thinking about them"

However, what is the future of microelectronics? Are we close to the end of this marvellous story? Is the future belonging to nanotechnologies that could completely replace microelectronics (although 0.015 μm transistors have a 15 nanometers length)? Nano-devices have been constructed, capable of switching a current or single electrons with a ratio between the on/off current of 1 thousand to 1 million. Such elements could be promising as their sizes of some nanometers and extremely low or no power consumption are very attractive. Carbon nanotubes, quantum dots, single electron devices or molecular switches are the most promising nano-devices. For instance, a carbon nanotube has a diameter of 1 nanometer, and depending on its diameter, is a semiconductor device (otherwise, it is a conductor, not usable as a switch). However, if one over 10 nanotubes is semiconductor, how to select and interconnect the semiconductor ones to provide a useful logic function?

Quantum dots are based on the Coulomb blockade effect and electrons are moved one by one from dots to dots. They have been constructed atom by atom by atomic force microscopes. Due to noise, it is better to construct cellular automata with several dots, and to define a given state of the automat as the logic "0" and another state as "1". Majority gates have been demonstrated,

as well as AND/OR gates. The main problem is still how to interconnect these gates to provide useful functions. Furthermore, it is hard to construct atom by atom a complete chip with several billions of elements.

Design methods could be completely different from today, as nano-devices could be constructed randomly, without any predefined schematic or layout. However, a useful function could emerge from this huge number of nano-devices, or some auto-organization could occur. It is a little bit similar to natural selection for which only the useful functions will survive. But it will be hard to design a predefined and very complex function like a Pentium microprocessor.

Yogi Berra, American Baseball player

"It is very hard to make predictions, especially for the future"

The most probable future is that microelectronics will be used until perhaps 2020. Then it will be probably not replaced by nanoelectronics, but both technologies, i.e. microelectronics and nanoelectronics will co-exist with probably different applications.

Welcome

Welcome to the 2002 International symposium on Low Power Electronics and Design (ISLPED), also known in short as the "low power symposium". ISLPED is unique in the sense that it brings academic and industrial researchers, technology, circuit, architecture, systems and software people together: their common concern being design for low power.

A total of 162 contributed papers were received. Many thanks to all the authors who submitted their manuscripts. We return to the 2,5 days program to give us a little more room to switch between sessions and interact with other participants during the poster sessions. Even with two parallel sessions, we were able to accept only 24 long papers, 16 short papers and 21 poster papers. We will also have one keynote speech, two invited presentations and two embedded tutorials. These invited presentations are again from the wide span of topics in this symposium: a presentation on low voltage memories, one on nanotechnology and one on system integration for wireless communication. The winners of the student design contest have a special session on Tuesday afternoon. The goal of the design contest is to encourage innovation in low power design and to showcase original power-aware designs. An industry sponsored cash award will be presented to each selected design entry. This year, the symposium will once again feature a small exhibits area.

Many thanks to the technical program committee for all the hard work in the paper review, paper selection and session organization. Additional experts have also contributed to the review process and we acknowledge their contribution. The list of the technical program committee members and of the additional reviewers can be found in the following pages. Many thanks to Prof. G. De Micheli and Prof. L. Benini for hosting the technical program committee meeting at Stanford. Thanks also to the invited speakers for graciously donating their time. The symposium has received generous support from Intel, Motorola, ARM, Chipvision, Magma, Sequence Design and BullDast. ISLPED is sponsored by ACM Sigda and the IEEE Circuits and Systems society and receives technical co-sponsorship from the IEEE Electron Devices Society and the IEEE Solid State Circuits Society.

Finally, we would like to thank you, the audience and the reader, for your interest and support of this symposium. We hope that you will find the symposium both stimulating and helpful.

Vivek De and Mary Jane Irwin
General Co-Chairs

Christian Piguet and Ingrid Verbauwhede
Technical Program Co-chairs

Table of Contents

ISLPED'02 Conference Organization	xi
---	----

Keynote Speech

Session Chair: Mary Jane Irwin (*Penn State University*)

- **Low-Voltage Memories for Power-Aware Systems**..... 1
K. Itoh (*Hitachi Ltd.*)

Session 1: Low Power Modeling and Systems

Session Chair: Nestoras Tzartzanis (*CSEM, EPFL, TPC*)

Session Organizer: Bill Athas (*Apple*)

- **Standby Power Management for a 0.18 μ m Microprocessor**..... 7
L. T. Clark, S. Demmons, N. Deutscher, F. Ricci (*Intel Corporation*)
- **Physical Insight into Fractional Power Dependence of Saturation Current on Gate Voltage in Advanced Short Channel MOSFETS (Alpha-Power Law Model)**..... 13
H. Im (*University of Tokyo, Dongguk University*), M. Song (*Dongguk University*),
T. Hiramoto (*University of Tokyo, VLSI Design and Education Center*), T. Sakurai (*University of Tokyo*)
- **Full-chip Sub-threshold Leakage Power Prediction Model for sub-0.18 μ m CMOS**..... 19
S. Narendra (*Massachusetts Institute of Technology, Intel Laboratories*), V. De, S. Borkar (*Intel Laboratories*),
D. Antoniadis, A. Chandrakasan (*Massachusetts Institute of Technology*)
- **Power-Conscious Interconnect Buffer Optimization with Improved Modeling of Driver MOSFET and Its Implications to Bulk and SOI CMOS Technology**..... 24
K. Nose, T. Saikurai (*University of Tokyo*)

Session 2: Energy Efficient Communication

Session Chair: Teresa Meng (*Stanford University*)

Session Organizer: Vijaykrishnan Narayanan (*Penn State University*)

- **E²WFQ: An Energy Efficient Fair Scheduling Policy For Wireless Systems**..... 30
V. Raghunathan, S. Ganeriwal, C. Schurgers, M. Srivastava (*University of California, Los Angeles*)
- **A Framework for Energy-Scalable Communication in High-Density Wireless Networks**..... 36
R. Min, A. Chandrakasan (*Massachusetts Institute of Technology*)
- **Contents Provider-Assisted Dynamic Voltage Scaling for Low Energy Multimedia Applications**..... 42
E.-Y. Chung (*CSL Stanford University*), L. Benini (*University of Bologna*),
G. De Micheli (*CSL Stanford University*)

Poster Session 1: Technology and Circuits

Session Chairs: R. V. Joshi (*IBM*), Lars Svensson (*Chalmers University*)

- **Low-Leakage Asymmetric-Cell SRAM**..... 48
N. Azizi, A. Moshovos, F. N. Najm (*University of Toronto*)
- **Managing Leakage for Transient Data: Decay and Quasi-Static 4T Memory Cells**..... 52
Z. Hu, P. Juang (*Princeton University*), P. Diodato, S. Kaxiras (*Agere Systems*),
K. Skadron (*University of Virginia*), M. Martonosi, D. W. Clark (*Princeton University*)
- **Conditional Pre-Charge Techniques for Power-Efficient Dual-Edge Clocking**..... 56
N. Nedovic, M. Aleksic, V. G. Oklobdzija (*University of California, Davis*)

- **Circuit-Level Techniques to Control Gate Leakage for sub-100nm CMOS** 60
F. Hamzaoglu, M. R. Stan (*University of Virginia*)
- **Modeling and Analysis of Leakage Power Considering Within-Die Process Variations** 64
Srivastava, R. Bai, D. Blaauw, D. Sylvester (*University of Michigan*)

Poster Session 2: System and Software Design

Session Chairs: Vamsi Krishna (*Agilent Technologies*)

- **Low-Power Approach for Decoding Convolutional Codes with Adaptive Viterbi Algorithm Approximations** 68
R. Henning, C. Chakrabarti (*Arizona State University*)
- **Power-aware Source Routing Protocol for Mobile Ad Hoc Networks**..... 72
M. Maleki, K. Dantu, M. Pedram (*University of Southern California*)
- **Analyzing Energy Friendly Steady State Phases of Dynamic Application Execution in Terms of Sparse Data Structures** 76
E. G. Daylight (*IMEC vzw, Katholieke University Leuven*), S. Wuytack, C. Ykman-Couvreur (*IMEC vzw*), F. Catthoor (*IMEC vzw, Katholieke University Leuven*)
- **Odd/Even Bus Invert with Two-Phase Transfer for Buses with Coupling**..... 80
Y. Zhang, J. Lach, K. Skadron, M. R. Stan (*University of Virginia*)
- **An Intra-Task Dynamic Voltage Scaling Method for SoC Design with Hierarchical FSM and Synchronous Dataflow Model**..... 84
S. Lee (*Seoul National University*), S. Yoo (*TIMA Lab*), K. Choi (*Seoul National University*)
- **Reducing Access Energy of On-Chip Data Memory Considering Active Data Bitwidth**..... 88
T. Okuma, Y. Cao, M. Muroyama, H. Yasuura (*Kyushu University*)

Session 3: Low Power Circuit Techniques

Session Chair: Ram Krishnamurthy (*Intel*)

Session Organizer: Kaushik Roy (*Purdue University*)

- **Energy Recovering Static Memory** 92
J. Kim, C. H. Ziesler, M. C. Papaefthymiou (*University of Michigan*)
- **Low Power Integrated Scan-Retention Mechanism**..... 98
V. Zyuban, S. V. Kosonocky (*IBM T. J. Watson Research Center*)
- **Closed-Loop Adaptive Voltage Scaling Controller for Standard-Cell ASICs**..... 103
S. Dhar, D. Maksimović (*University of Colorado*), B. Kranzen (*National Semiconductor*)
- **Design of a Branch-Based 64-bit Carry-Select Adder in 0.18 μ m Partially Depleted SOI CMOS** 108
A. Nève, D. Flandre (*Université Catholique de Louvain*),
H. Schettler, T. Ludwig, G. Hellner (*IBM Entwicklung GmbH*)

Session 4: Energy Efficient System Design

Session Chair: N. Ranganathan (*University of S. Florida, Tampa, FL*)

Session Organizer: Mahmut Kandemir (*Penn State University*)

- **Low -Power Color TFT LCD Display for Hand-Held Embedded Systems**..... 112
I. Choi, H. Shim, N. Chang (*Seoul National University*)

- **Discharge Current Steering for Battery Lifetime Optimization**..... 118
L. Benini (*Università di Bologna*), A. Macii, E. Macii (*Politecnico di Torino*),
M. Poncino (*Università di Verona*)
- **Towards Energy-Aware Software-Based Fault Tolerance in Real-Time Systems** 124
O. S. Unsal, I. Koren, C. M. Krishna (*University of Massachusetts, Amherst*)

Session 5: Memory Subsystem

Session Chair: Lawrence Clark (*Intel*)

Session Organizer: Peter Kogge (*University of Notre Dame*)

- **Fine-Grain CAM-Tag Cache Resizing Using Miss Tags**..... 130
M. Zhang, K. Asanović (*MIT Laboratory for Computer Science*)
- **An Adaptive Serial-Parallel CAM Architecture for Low-Power Cache Blocks** 136
A. Efthymiou, J. D. Garside (*University of Manchester*)
- **Reducing Energy Consumption of Video Memory by Bit-Width Compression** 142
V. G. Moshnyaga, K. Inoue, M. Fukagawa (*Fukuoka University*)
- **A History-Based I-Cache for Low-Energy Multimedia Applications** 148
K. Inoue, V. G. Moshnyaga (*Fukuoka University*), K. Murakami (*Kyushu University*)

Session 6: Modeling and Design Issues

Session Chair: Anand Raghunathan (*NEC*)

Session Organizer: Joerg Henkel (*NEC*)

- **Battery Lifetime Prediction for Energy-Aware Computing** 154
D. Rakhmatov, S. Vruthula (*University of Arizona*),
D. A. Wallach (*Hewlett-Packard Western Research Laboratory*)
- **Early Evaluation Techniques for Low Power Binding** 160
E. Kursun, A. Srivastava, S. O. Memik, M. Sarrafzadeh (*University of California, Los Angeles*)
- **Unified Methodology for Resolving Power-Performance Tradeoffs at the Microarchitectural and Circuit Levels**..... 166
V. Zyuban, P. Strenski (*IBM T.J. Watson Research Center*)

Invited Talk

Session Chair: Ingrid Verbauwhede (*UCLA*)

- **Is Nanoelectronics the Future of Microelectronics?**..... 172
M. Lundstrom (*Purdue University*)

Session 7: Microarchitecture Techniques

Session Chair: David Brooks (*IBM T.J. Watson*)

Session Organizer: Lea Hwang Lee (*Motorola*)

- **Saving Energy with Just In Time Instruction Delivery**..... 178
T. Karkhanis, J. E. Smith (*University of Wisconsin-Madison*), P. Bose (*IBM T.J. Watson Research Center*)
- **Tradeoffs in Power-Efficient Issue Queue Design** 184
A. Buyuktosunoglu, D. H. Albonesi (*University of Rochester*),
P. Bose, P. W. Cook, S. E. Schuster (*IBM T. J. Watson Research Center*)
- **Reducing Transitions on Memory Buses Using Sector-based Encoding Technique**..... 190
Y. Aghaghiri (*University of Southern California*), F. Fallah (*Fujitsu Laboratories of America*),
M. Pedram (*University of Southern California*)
- **Energy-Efficient Hybrid Wakeup Logic** 196
M. Huang, J. Renau, J. Torrellas (*University of Illinois at Urbana-Champaign*)

Session 8: Technology-Driven Power Optimization

Session Chair: Unni Narayanan (*Intel*)

Session Organizer: G. Stamoulis (*Technical University of Crete*)

- **Automated Selective Multi-Threshold Design For Ultra-Low Standby Applications** 202
K. Usami, N. Kawabe, M. Koizumi, K. Seta (*Toshiba Corporation Semiconductor Company*),
T. Furusawa (*Toshiba Microelectronics Corporation*)
- **HA²TSD: Hierarchical Time Slack Distribution for Ultra-Low Power CMOS VLSI**..... 207
K.-w. Choi, A. Chatterjee (*Georgia Institute of Technology*)
- **Runtime Mechanism for Leakage Current Reduction in CMOS VLSI Circuits**..... 213
A. Abdollahi (*University of Southern California*), F. Fallah (*Fujitsu Laboratories of America*),
M. Pedram (*University of Southern California*)

Embedded Tutorial 1

Session Chair: Chritian Piguet (*CSEM&EPFL, Switzerland*)

- **Future Directions in Clocking Multi-Ghz Systems**..... 219
V. G. Oklobdzija (*University of California*), J. Sparsø (*Technical University of Denmark*)

Embedded Tutorial 2

Session Chair: Mary Jane Irwin (*Penn State University*)

- **Compilers for Power and Energy Management**..... 220
U. Kremer (*Rutgers University*)

Session 9: Analog Electronic

Session Chair: Paul Hurst (*UC Davis*)

Session Organizer: Satyen Mukherjee (*Philips*)

- **Oversampled Gain-Boosting** 221
O. Oliaei (*Motorola Labs*)
- **$\pm 0.5V \sim \pm 1.5V$ VHF CMOS LV/LP Four-Quadrant Analog Multiplier
in Modified Bridged-Triode Scheme**..... 227
S. C. Li, J. C. Cha (*National Yunlin University of Science and Technology*)
- **A Power and Resolution Adaptive Flash Analog-to-Digital Converter** 233
J. Yoo, D. Lee, K. Choi, J. Kim (*Pennsylvania State University*)
- **Design Techniques for Low Power High Bandwidth Upconversion in CMOS**..... 237
C. De Ranter, M. Steyaert (*Katholieke Universiteit Leuven*)

Session 10: Design Contest Presentation

Session Chair: Vivek Tiwari (*Intel*)

Poster Session 3: Logic and Micro Architecture

Session Chairs: Vojin G. Oklobdzija (*UC Davis*)

- **TLB and Snoop Energy-Reduction using Virtual Caches
in Low-Power Chip-Multiprocessors** 243
M. Ekman (*Chalmers University of Technology*), F. Dahlgren (*Ericsson Mobile Platforms*),
P. Stenström (*Chalmers University of Technology*)
- **A Preactivating Mechanism for a VT-CMOS Cache using Address Prediction** 247
R. Fujioka, K. Katayama, R. Kobayashi, H. Ando, T. Shimada (*Nagoya University*)

- **Dynamic Vt SRAM: A Leakage Tolerant Cache Memory for Low Voltage Microprocessors**..... 251
C. H. Kim, K. Roy (*Purdue University*)
- **Asymmetric-Frequency Clustering: A Power-Aware Back-End for High-Performance Processors**..... 255
A. Baniasadi (*Northwestern University*), A. Moshovos (*University of Toronto*)

Poster Session 4: Analysis, Estimation and Optimization

Session Chairs: Ed Cheng (*Synopsys*)

- **Power Analysis Techniques for SoC with Improved Wiring Models**..... 259
T. Sakamoto, T. Yamada, M. Mukuno, Y. Matsushita, Y. Harada (*Sanyo Electric*),
H. Yasuura (*Kyushu University*)
- **A Microarchitectural-Level Step-Power Analysis Tool**..... 263
W. El-Essawy, D. H. Albonesi (*University of Rochester*), B. Sinharoy (*IBM Corporation*)
- **Power Estimation of Sequential Circuits using Hierarchical Colored Hardware Petri Net Modeling**..... 267
A. K. Murugavel, N. Ranganathan (*University of South Florida*)
- **High-Level Area Estimation**..... 271
K. M. Büyükkahin (*University of Illinois at Urbana-Champaign*), F. N. Najm (*University of Toronto*)
- **Retiming-Based Logic Synthesis for Low-Power** 275
Y.-L. Hsu, S.-J. Wang (*National Chung-Hsing University*)
- **Activity-Sensitive Clock Tree Construction for Low Power**..... 279
C. Chen, C. Kang (*University of Windsor*), M. Sarrafzadeh (*University of California at Los Angeles*)

Invited Talk

Session Chair: Vivek De (*Intel*)

Session 11: Signal Processing

Session Chair: Wanda Gass (*Texas Instruments*)

Session Organizer: Sanjive Agarwala (*Texas Instruments*)

- **Low-Power VLSI Decoder Architectures for LDPC Codes**..... 284
M. M. Mansour, N. R. Shanbhag (*University of Illinois at Urbana-Champaign*)
- **A Low Power Normalized-LMS Decision Feedback Equalizer for a Wireless Packet Modem**..... 290
D. Garrett, C. Nicol (*Lucent Technologies*), A. Blanksby, C. Howland (*Agere Systems*)
- **High-Performance and Low Power FIR Filter Design Based on Sharing Multiplication**..... 295
J. Park, W. Jeong, H. Choo, H. Mahmoodi-Meimand, Y. Wang, K. Roy (*Purdue University*)
- **A Low-Power Digital Matched Filter for Spread-Spectrum Systems** 301
S. Goto, T. Yamada, N. Takayama, Y. Matsushita, Y. Harada (*Sanyo Electric, Co., Ltd.*),
H. Yasuura (*Kyushu University*)

Session 12: Simulation and Estimation Techniques

Session Chair: Pai Chou (*UCI*)

Session Organizer: Wolfgang Nebel (*OFFIS, Oldenburg University*)

- **Parametric Timing and Power Macromodels for High Level Simulation of Low-Swing Interconnects**..... 307
D. Bertozzi, L. Benini, B. Ricco (*University of Bologna*)
 - **Compact Models for Estimating Microprocessor Frequency and Power**..... 313
W. Athas, L. Youngs (*Apple Computer*), A. Reinhart (*Motorola Labs*)
 - **Efficient Estimation of Signal Transition Activity in MAC Architectures** 319
A. García, L. D. Kabulepa, M. Glesner (*Darmstadt University of Technology*)
 - **Novel Modeling Techniques for RTL Power Estimation**..... 323
M. Eiermann, W. Stechele (*Technical University of Munich*)
- Author Index** 329

Committee page not received in time for publication

Author Index

Abdollahi, A.	213	Efthymiou, A.	136
Aghaghiri, Y.	190	Eiermann, M.	323
Albonesi, D. H.	184, 263	Ekman, M.	243
Aleksic, M.	56	El-Essawy, W.	263
Ando, H.	247	Fallah, F.	190, 213
Antoniadis, D.	19	Flandre, D.	108
Asanović, K.	130	Fujioka, R.	247
Athas, W.	313	Fukagawa, M.	142
Azizi, N.	48	Furusawa, T.	202
Bai, R.	64	Ganeriwal, S.	30
Baniasadi, A.	255	García, A.	319
Benini, L.	42, 118, 307	Garrett, D.	290
Bertozzi, D.	307	Garside, J. D.	136
Blaauw, D.	64	Glesner, M.	319
Blanksby, A.	290	Goto, S.	301
Bose, P.	178, 184	Hamzaoglu, F.	60
Büyükaşahin, K. M.	271	Harada, Y.	259, 301
Buyuktosunoglu, A.	184	Hellner, G.	108
Cao, Y.	88	Henning, R.	68
Catthoor, F.	76	Hiramoto, T.	13
Cha, J. C.	227	Howland, C.	290
Chakrabarti, C.	68	Hsu Y.-L.	275
Chandrakasan, A.	19, 36	Hu, Z.	52
Chang, N.	112	Huang, M.	196
Chatterjee, A.	207	Im, H.	13
Chen, C.	279	Inoue, K.	142, 148
Choi, I.	112	Itoh, K.	1
Choi, K.	84, 233	Jeong, W.	295
Choi, K.-w.	207	Juang, P.	52
Choo, H.	295	Kabulepa, L. D.	319
Chung, E.-Y.	42	Kang, C.	279
Clark, D. W.	52	Karkhanis, T.	178
Clark, L. T.	7	Katayama, K.	247
Cook, P. W.	184	Kawabe, N.	202
Dahlgren, F.	243	Kaxiras, S.	52
Dantu, K.	72	Kim, C. H.	251
Daylight, E. G.	76	Kim, J.	92, 233
De Micheli, G.	42	Kobayashi, R.	247
De Ranter, C.	237	Koizumi, M.	202
De, V.	19	Koren, I.	124
Demmons, S.	7	Kosonocky, S. V.	98
Deutscher, N.	7	Kranzen, B.	103
Dhar, S.	103	Kremer, U.	220
Diodato, P.	52	Krishna, C. M.	124

Kursun, E.	160	Roy, K.	251, 295
Lach, J.	80	Sakamoto, T.	259
Lee, D.	233	Sakurai, T.	13, 24
Lee, S.	84	Sarrafzadeh, M.	160, 279
Li, S. C.	227	Schettler, H.	108
Ludwig, T.	108	Schurgers, C.	30
Lundstrom, M.	172	Schuster, S. E.	184
Macii, A.	118	Seta, K.	202
Macii, E.	118	Shanbhag, N. R.	284
Mahmoodi-Meimand, H.	295	Shim, H.	112
Maksimović, D.	103	Shimada, T.	247
Maleki, M.	72	Sinharoy, B.	263
Mansour, M. M.	284	Skadron, K.	52, 80
Martonosi, M.	52	Smith, J. E.	178
Matsushita, Y.	259, 301	Song, M.	13
Memik, S. O.	160	Sparsø, J.	219
Min, R.	36	Srivastava, A.	64, 160
Moshnyaga, V. G.	142, 148	Srivastava, M.	30
Moshovos, A.	48, 255	Stan, M. R.	60, 80
Mukuno, M.	259	Stechele, W.	323
Murakami, K.	148	Stenström, P.	243
Muroyama, M.	88	Steyaert, M.	237
Murugavel, A. K.	267	Strenski, P.	166
Najm, F. N.	48, 271	Sylvester, D.	64
Narendra, S.	19	Takayama, N.	301
Nedovic, N.	56	Torrellas, J.	196
Nève, A.	108	Unsal, O. S.	124
Nicol, C.	290	Usami, K.	202
Nose, K.	24	Vrudhula, S.	154
Oklobdzija, V. G.	219	Wallach, D. A.	154
Oklobzija, V. G.	56	Wang, S.-J.	275
Okuma, T.	88	Wang, Y.	295
Oliaei, O.	221	Wuytack, S.	76
Papaefthymiou, M. C.	92	Yamada, T.	259, 301
Park, J.	295	Yasuura, H.	88, 259, 301
Pedram, M.	72, 190, 213	Ykman-Couvrer, C.	76
Poncino, M.	118	Yoo, J.	233
Raghunathan, V.	30	Yoo, S.	84
Rakhmatov, D.	154	Youngs, L.	313
Ranganathan, N.	267	Zhang, M.	130
Reinhart, A.	313	Zhang, Y.	80
Renau, J.	196	Ziesler, C. H.	92
Ricci, F.	7	Zyuban, V.	98, 166
Ricco, B.	307		