TUTORIAL 4

PLACEMENT - THE KEY PROBLEM IN PHYSICAL DESIGN

Speakers:

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Background: Placement is one of the main tasks in physical layout. The quality of the placement becomes more and more important with shrinking feature sizes for several reasons: routability is harder to achieve; the wireload has an increasing impact on the timing behavior; and minimizing power consumption (which depends on the overall wire capacitance, and thus on the placement) is an increasingly important objective. However, even for the classical (and still useful) problem formulations, many questions have remained open. An additional challenge is posed by increasing complexities of chips, where placement has to deal with several million movable components.

The target audience includes design engineers, academic researchers, and anyone interested in physical design.

Description: This tutorial starts with a description of an automated design flow from a designer's viewpoint. The design objectives are discussed, and the key role of the placement problem, in interaction with other tasks like routing, timing optimization, logic changes and clocktree design, is stressed. Examples of current production parts and future trends highlight the design complexities that need to be supported. The first part ends with addressing the question of hierarchical versus flat design and illuminating some pros and cons.

The second part discusses hierarchy, and, in particular, floorplanning. We will discuss the two approaches to hierarchical physical implementation: one, the top-down floorplanning approach and two, the bottom-up partitioning approach. Key technologies that enable both approaches will be enumerated. We will discuss a few floorplan representations and talk about algorithms used by current block placers. We will also talk about pin assignment techniques, and timing budgeting for hierarchical implementation.

Basic placement algorithms are subject of the third part of this tutorial. Classical formulations of the placement problem, though still useful, are far from being well-solved in spite of intensive research for decades. We will summarize what is known in theory, review the most successful placement approaches, and discuss their pros and cons. Stability and robustness is essential for achieving design closure when integrating other tools (like timing optimization) and objectives into the placement flow. While the classical and most common objective in global placement is minimization of some weighted netlength estimation, the goal in detailed placement (legalization) is usually rather to minimize the weighted total movement. We discuss both problems, their objectives, constraints, and solution techniques in theory and practice.

The effects of placement on the timing and routability properties of a circuit are paramount. The fourth part of this tutorial will give an overview of the state of knowledge in this area and will discuss potential future directions. Timing related topics will include performance models, path-based versus net-based timing optimization and implications of post-placement optimizations such as buffer insertion. In the routability area, congestion modeling and validation including constructive versus statistical models will be discussed. A discussion of global and detailed routability optimization techniques is also planned.