

Noise Propagation and Failure Criteria for VLSI Designs

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Abstract

Noise analysis has become a critical concern in advanced chip designs. Traditional methods suffer from two common issues. First, noise that is propagated through the driver of a net is combined with noise injected by capacitively coupled aggressor nets using linear summation. Since this ignores the non-linear behavior of the driver gate the noise that develops on a net can be significantly underestimated. We therefore propose a new linear model that accurately combines propagated and injected noise on a net and which maintains the efficiency of linear simulation. After the propagated and injected noise are correctly combined on a victim net, it is necessary to determine if the noise can result in a functional failure. This is the second issue that we discuss in this paper. Traditionally, noise failure criteria have been based on unity gain points of the DC or AC transfer curves. However, we will show that for digital designs, these approaches can result in a pessimistic analysis in some cases, while in other cases, they allow circuit operation that is extremely close to regions that are unstable and do not allow sufficient margin for error in the analysis. In this paper, we compare the effectiveness of the discussed noise failure criteria and also present a propagation based method, which is intended to overcome these drawbacks. The proposed methods were implemented in a noise analysis tool and we demonstrate results on industrial circuits.

1 Introduction

Process scaling has led to a significant increase in capacitive [1][2] and inductive coupling [3] in VLSI interconnects, resulting in large noise injection from neighboring nets and making noise analysis a critical concern in today's chip design. In noise analysis, the net under consideration is referred to as the *victim* net, and the neighboring nets that inject noise on the victim net are referred to as *aggressor* nets. Noise is broadly classified into two types. *Functional noise* [1] occurs when a victim net is intended to be at a stable state and results in an unwanted noise pulse on the net. If this noise pulse is of sufficient magnitude and is able to propagate to a memory element, such as a latch or dynamic gate, it can change the state of the memory element and cause a functional failure. *Delay noise* [4] occurs when noise is injected on a net when it transitions, and results in a change in the delay of the net. In this paper, we consider the problem of functional noise.

Noise analysis is a difficult problem since a number of different sources of noise must be considered and since noise along a circuit path combines in a non-linear manner as it propagates through the gates of a path. Also, since noise is an AC pulse, both the height, width and shape of a noise pulse are significant and must be considered in the analysis. In order to ensure that no noise errors in the design escape the analysis, it is necessary to perform a conservative analysis which errs on the side of pessimism. However, with the dramatic increase of noise in digital design, it is necessary that the analysis is not overly pessimistic. Otherwise, an inordinate number of false noise failures could result that would be difficult to fix and would require excessive chip resources and performance sacrifices. To this end, a number of methods have been proposed to account for logic and timing correlations that constrain the manner in which noise source can combine [5][6][7][8].

During noise analysis, noise injected by aggressor nets combines with noise propagated from the input of the victim driver gate, as illustrated in Figure 1. The victim receiver gate is then examined to determine if the combined noise constitutes a failure. In order to ensure an

accurate analysis, it is necessary to correctly model the propagation and addition of noise along a circuit path and to identify which noise pulses at the receiver gates cause a circuit failure. It is these two key issues that we address in this paper.

The propagation of noise through a circuit is complicated by the non-linear behavior of the gates through which the noise propagates. To efficiently compute the *injected* noise, analysis tools typically use linear models for the victim and aggressor driver gates. The victim driver is modeled with a grounded resistance which is computed using small signal analysis of the driver with both driver input and output biased at stable supply voltages. The use of such a linear model has two advantages.

- The entire interconnect circuit can be analyzed using efficient linear methods, such as reduced order modeling methods [9].
- Superposition can be used to sum the noise injected from each individual aggressor, making it simple to align the noise pulse peaks from each aggressor.

To compute the *propagated* noise, analysis tools typically store the results of non-linear simulations in pre-characterized tables for a number of different input noise pulse widths and heights. During noise analysis, the propagated noise and the injected noise from aggressor nets are then added linearly. Hence, they can be computed independently and their worst-case alignment is easily determined. This allows for a very efficient and simple analysis which has resulted in wide spread use of this method.

However, this approach is based on the underlying assumption that the victim driver gate is linear and the approach is similar to noise analysis in analog circuits, where noise sources are small and devices exhibit relatively linear behavior. In digital circuit, on the other hand, noise can be quite large (due to its inherent robustness), and the devices are constructed to have a very high gain and exhibit highly non-linear behavior. Therefore, the linear addition of propagated and injected noise is not valid and can result in a significant error in the computed noise. To illustrate the magnitude of this problem, Figure 2 shows the simulation of a typical noise cluster from an industrial 0.13 micron design. Computed separately, the propagated noise pulse has a height of 70mV and the injected noise pulse a height of 453mV and their linear combination results in a noise height of 523mV. However, non-linear simulation of simultaneous injected and propagated noise results in a combined noise pulse with a height of 900mV, which is 72% higher.

This large error is due to the fact that the holding resistance of the victim driver is not constant during the noise propagation, even though the propagated noise is small (70mV). In fact, it is possible that the input

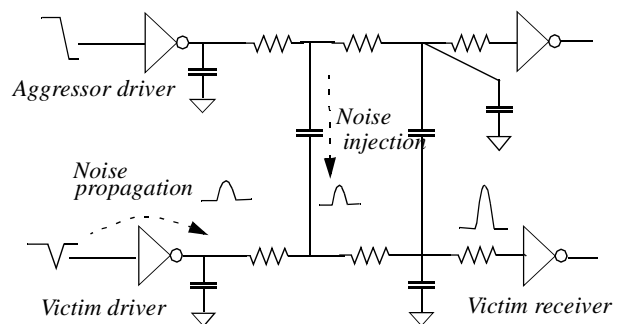


Figure 1. Noise due to propagation and injection

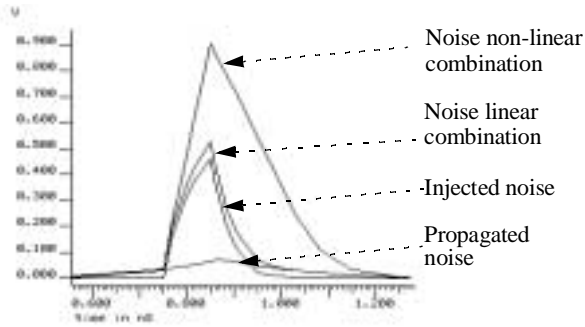


Figure 2. Computation of propagated and injected noise.

noise at the victim driver is sufficiently small such that it does not yield any propagated noise, while still significantly modulating the holding resistance and increasing the injected noise on the victim net. The non-linearity of the driver therefor greatly complicates the noise analysis and results in a dependence between the propagated and injected noise.

It is clear that the linear combination of the propagated noise and injected noise, commonly used noise analysis tools, can result in a significant underestimation of the actual noise, making it possible for real noise failures to go undetected. The straightforward solution to this problem is to perform non-linear simulation of the entire coupled interconnect and driver network. However, even though the linear portion of the network can be represented with a reduced order model, non-linear simulation is too slow for analysis of large, cell-based designs which require analysis of several hundreds of thousands of global nets. Also, determining the worst-case alignment between the propagated noise and the injected noise is difficult in non-linear simulation. In this paper, we therefore propose a new *linear* model that allows injected and propagated noise to be accurately combined for a net while allowing the use of efficient linear analysis and superposition techniques. The approach lends itself well for pre-characterized cell-based analysis approaches and is demonstrated on industrial circuits.

After the propagated and injected noise are correctly combined, it is necessary to determine if the noise can result in a functional failure. This is the second issue that we address in this paper. A noise failure criteria must meet two requirements: 1) It must ensure that the present noise level cannot change the state of a memory element in the design. 2) It must ensure that a small increase in the noise at a particular point in the circuit, due to process variation or simulation error, does not result in a disproportional increase of noise at the latch element. Historically, noise analysis has been based on DC noise margins, defined as NM_L and NM_H in Figure 3(a) and any noise pulse with a height that exceeds the DC noise

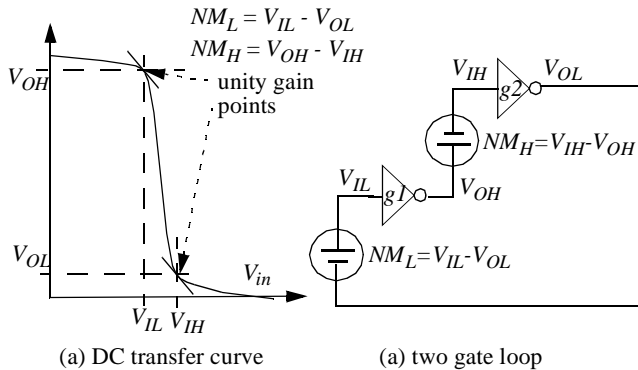


Figure 3. DC noise margins in two gate feedback loop

margin of the receiver gate is flagged as a noise failure. However, this criterion ignores the width of the noise pulse and since digital

noise often exhibits narrow pulse widths, a purely DC analysis is very conservative.

An AC extensions of the DC noise margin was therefore proposed in [1][2][10], based on the unity gain points of the AC transfer curve. In this method, the gain in the receiver output noise voltage at all points in time is computed with respect to a DC offset added to the noise pulse at the receiver gate input. If this gain exceeds (becomes more negative than) -1 at any point in time, the noise is considered to cause a functional failure. As explained in more detail in Section 2, an issue of this approach is that it may over or underestimate the sensitivity of the peak noise pulse height to the DC offset if the DC offset influences the receiver delay. As one of the noise failure criteria studied in this paper, we therefore propose an alternate AC gain measure that addresses this problem.

In a second AC failure criterion method [11], the noise pulse at the input of the receiver is first propagated through the receiver gate and the resulting noise pulse height at the *output* of the receiver gate is compared against the unity gain output voltage V_{OL} or V_{OH} on the DC transfer curve. This approach simplifies the analysis in that it does not require the computation of AC sensitivities, while still allowing for narrow noise pulses to be substantially attenuated by the low pass properties of the receiver gate.

Both proposed criteria share in common that they are based on the unity gain point of either DC or AC transfer curves of the receiver gate. Below, we list three motivations for using the unity gain point as a failure criteria, as well as some of their limitations for noise analysis in digital circuits.

1. The DC transfer curve is very steep between the two unity gain points and constraining the noise to be less than the unity gain points avoids this region, where a small change in input noise height results in a large change in output noise. However, as illustrated in Figure 3(a), the unity gain point can lie only a few millivolt from this steep region in CMOS gates, while the expected uncertainty in the noise pulse height due to errors in the parasitic extraction and simulation can be substantially larger. Limiting the noise to the unity gain point therefore may not allow for a sufficient safety margin for stable operation.
2. The differential gain of a circuit loop is less than one if all gates in the loop have a differential gain less than 1 (i.e. they operate below their unity gain point). However, we will show this is only true under very specific conditions. If the width of a noise pulse is larger than the loop delay, or if multiple nodes in the current loop are simultaneously affected by an error in the noise computation, the differential loop gain may in fact significantly exceed one.
3. Limiting the noise at each stage to the unity gain point provides a method of budgeting the allowed noise at each stage along a path such that the *sum* of the noise margins for two identical gates connected in series is maximized. However, when the circuit consists of non-identical gates or when the injected noise varies strongly from stage to stage, such a noise “budget” for each stage can be overly constraining and can result in a pessimistic analysis results.

Noise failure criteria based on the unity gain points therefore can result in a pessimistic analysis in some cases, while in other cases, they can allow circuit operation extremely close to regions that are unsafe without allowing sufficient margin of error. The purpose of this paper is to compare the two discussed unity gain failure criteria and study the effectiveness of such criteria for digital circuits. To this end, we also discuss a third, non-unity gain based method referred to as the *latch transition criterion* which propagates and combines noise along circuit paths and then checks if the resulting noise pulse at the input of a latch or memory element is able to cause a change in its state. In order to ensure that a noise does not result in operation close to the unsafe regions of operation where the transfer curves are very steep, an error margin

is added to the noise at each stage along a path. This margin is set to be larger than the expected error in the computed noise height at a stage due to uncertainties in extraction and simulation. No noise budget is imposed on the noise levels along a circuit path preceding a memory element, thereby allowing a stage with high noise to be attenuated by several subsequent stages with small noise. Since the change of the memory state is ultimately the mechanism through which noise causes a functional failure in the device, directly checking for this condition was found to result in a significantly less pessimistic analysis.

One of the difficulties in the latch transition criterion is to correctly model the non-linear behavior of the driver gate when combining propagated and injected noise, as addresses in this paper. A second difficulty is to efficiently determine if a particular noise pulse can change the state of a latch, since the final state of the latch depends not only on the noise pulse height and width but also on its alignment with the clock edge. The exact solution to this problem requires finding the worst-case alignment of the noise pulse and clock signal, which can require many transient simulations. In this paper, we therefore also propose an efficient and conservative method that addresses this problem with only two transient simulations.

The proposed methods were implemented in an industrial noise analysis tool and were tested on industrial circuits. We demonstrate the accuracy of the proposed method for combining propagated and injected noise on a number of industrial interconnects. We then compare the effectiveness of the two existing noise failure criteria as well as the non-unity gain base latch transition criterion. For a large microprocessor with over 250,000 global interconnects we show that unity gain based noise failure criteria have a high degree of pessimism, reporting numerous failures. On the other hand, the latch transition criterion reports no failures, which is consistent with the fact that the chip was successfully tested in silicon without any noise problems.

The remainder of this paper is organized as follows. In Section 2, we discuss the three noise failure criteria. In Section 3, we present the proposed method for combining injected and propagated noise. In Section 4, we present the results and in Section 5, we draw our conclusions.

2 Noise Failure Criteria

Existing noise failure criteria are AC extensions of the traditional DC noise margins, which is based on the unity gain points of the DC transfer curve. In this Section, we will examine the rationale for using the unity gain points and its limitations as applied to current digital design. Although we discuss DC unity gain points, the same arguments apply to their AC extensions as well. In Sections 2.1 through 2.5, we then discuss the existing and proposed noise failure criteria.

DC noise margins were developed to address the need for design rules that specify the maximum allowable noise at the input of a particular gate. Since these noise margins are computed before the context of the gate is known, the AC characteristics of the noise at the gate input can not be predicted, and hence DC noise is assumed to ensure a conservative analysis. Similarly, the type of gates in subsequent stages of the design and their susceptibility to noise is also not known, and therefore, a gate is assumed to drive an identical gate as fanout arranged in a two gate loop, as shown in Figure 3(b). In this loop, the input of gate g_1 is at a nominal low voltage and the input of gate g_2 is at a nominal high voltage. The maximum (minimum) allowed input voltage of gate g_1 (g_2) is defined as V_{IL} (V_{IH}), resulting in a maximum voltage at the gate output of $V_{OH} = H(V_{IL})$ ($V_{OL} = H(V_{IH})$), where H is the DC transfer function. The maximum allowed noise voltages or noise margins are represented

by the two voltage sources NM_L and NM_H , as shown in Figure 3(b). In order to ensure stable operation, two criteria must be satisfied:

1. When the maximum allowed noise voltages NM_L and NM_H are applied in the feedback loop, the overall system must remain stable and must not switch to the opposite state.
2. When all gates are biased at their maximum allowed input voltage, the differential gain of the loop must remain less than one, meaning that the sensitivities of the node voltages to the noise voltages are less than one. This ensures that the system is well behaved in the presence of a small error in the computed noise voltage.

Given a specified maximum valid input voltages V_{IL} and V_{IH} , criterion one is satisfied by defining the noise margins as $NM_L = V_{IL} - H(V_{IH})$ and $NM_H = H(V_{IL}) - V_{IH}$, as shown in Figure 3. Naturally, V_{IL} and V_{IH} must be selected such that both noise margins are positive and are maximized. Reducing V_{IL} and/or V_{IH} increases the high noise margin NM_H at the cost of a smaller low noise margin NM_L and vice versa. Selecting V_{IL} and V_{IH} therefore “budgets” the allowable noise in the loop between NM_L and NM_H . In order to maximize the sum of the two noise margins, $NM_L + NM_H = V_{IL} + H(V_{IL}) - V_{IH} - H(V_{IH})$, it is easy to derive through differentiation that the valid input voltages must be set at their unity gain point: $V_{IL} = -dH(V_{IL})/d(V_{IL})$ and $V_{IH} = -dH(V_{IH})/d(V_{IH})$.

Maximizing the sum of the noise margins is a reasonable objective for developing design rules when no specific information about the distribution of the noise among the nets in the circuit is known. However, during chip-level noise analysis, the exact amount of inject noise among nets is known. Apriori restricting the noise on a net base on the unity gain points therefore results in an unnecessarily pessimistic analysis.

The second stability criterion requires that the differential gain of the loop is less than 1, when each gate is biased at its worst valid input voltage V_{IL} or V_{IH} . We define the differential gain of an individual gate at its worst valid bias point as $p = dH(V_{out})/d(V_{in})$ and the open loop gain coefficient $k = p_1 * p_2$, as the differential gain of the circuit when the feedback is disconnected. If each gate operates at its unity gain point, $k=1$. To determine the differential gain l of the loop with closed feedback, we consider two cases. First, if the noise pulse present on the nodes is short compared to the delay of the loop, an increase in the pulse height of a single noise source will not accumulate on itself along the feedback loop and $l=k$. In this case, criterion 2 is satisfied when each gate operates at its unity gain point.

However, a noise pulse is often wide compared to the delay of the loop, for instance for the feedback of latches, or for wide noise pulses, such as power supply noise. In this second case, the differential loop gain can be shown to be $l = k/(1-k)$ [13], and will be infinite if each gate operates at its unity gain point. This can be easily understood from Figure 3(a). If each gate is operating at its unity gain point, $p = 1$, and a small increase in the voltage NM_L will result in an equal increase in V_{OH} and V_{OL} . This increase in V_{OL} will sum with the initial increase of NM_L , resulting a larger change of V_{IL} and therefore a greater increase in V_{OH} , etc.

It is also useful to examine the total differential gain of an infinite chain of gates with respect to a simultaneous increase in the noise at *each* node. For digital designs, this situation is, in fact, more realistic than the case where only one noise source is increased, since an error in the computed noise due to extraction and simulation error will affect *all* noise sources simultaneously. It can be easily shown that in this case, the differential gain of the chain will be $p/(1-p)$, meaning that it can be of any value even if every gate operates below its unity gain point.

Finally, it is important to point out that the second criterion ensures stability only for very small errors in noise, since the slope of the transfer curve increases rapidly past the unity gain point. Even a small error in the computed noise would be sufficient to cause the gate to operate at a gain point significantly exceeding 1. To address this issue in the proposed method discussed in Section 2.3, we therefore add a substantial margin to the computed noise at each stage to increase the tolerated margin of error in the analysis. At the same time, noise is only checked at the latch or memory element in this approach, thereby removing the inherent budgeting that occurs when noise margins are enforced at each gate. This allows larger noise at one stage to be attenuated by subsequent stages in the design which have less injected noise or are less susceptible to noise.

In the following three Sections, we present the implementation of the three different noise failure criteria.

2.1 Static gain failure criterion.

In the *static gain failure criterion*, the noise pulse at the input of the receiver gate is propagated across the gate and if the maximum receiver output noise voltage exceeds the output voltage at the unity gain point of its DC transfer curve (V_{OL} or V_{OH}), the noise is flagged as failing. The advantage of this approach is its simplicity since it does not require any computation of dynamic (transient) sensitivities. It has the same properties and limitations as checking the noise pulse height at the input of the receiver against the unity gain input voltage (V_{IL} or V_{IH}), as discussed in the previous Section. However, it has the added advantage that it is less pessimistic since the low pass filter properties of the receiver gate will filter out noise with short pulse widths.

We consider two variations of this approach. In the first one, the total noise on a net is computed as the combination of the injected noise and the noise propagated from the inputs of the victim driver gate. This requires that all gates are processed in topological order and requires iterations in the presence of feedback in the circuit. In the second version, the total noise on a net is computed as the combination of the injected noise and the maximum allowable noise at the driver output (V_{OL} or V_{OH}). This technique has the advantage that the amount of propagated noise is known apriori for each driver gate and the analysis of each net is independent, thereby simplifying the analysis at the cost of increased pessimism.

2.2 Dynamic gain failure criterion

An analysis approach based on the unity gain point of the AC transfer curve was first proposed in [2][10]. The AC noise sensitivity in this approach is taken to be:

$$S(t) = \left. \frac{dV_{out}(t)}{dV_{in,DC}} \right|_{V_{in,DC} = 0} \quad (\text{EQ 1})$$

where $V_{out}(t)$ is the propagated noise pulse voltage, and $V_{in,DC}$ is a DC voltage source in series with the noise pulse at the gate input. This sensitivity expresses the sensitivity of each point of the propagated noise with respect to a DC platform added to the input noise. If the magnitude of $S(t)$ is less than -1 at any point in time, a noise failure is flagged. However, error may be introduced if the delay of the gate is impacted by the added DC platform. In this case, it is possible that $S(t)$ is high, simply because the delay of the propagated noise pulse is changed while its magnitude is unchanged as shown in Figure 4.

To overcome this problem, we propose an alternate dynamic gain criterion. The objective is to find the differential gain dV_{out}/dV_{in} , where V_{out} is the propagated noise, V_{in} is the input noise and the gain is variation of output noise with respect to the input noise. The difficulty is in how to define the input noise pulse

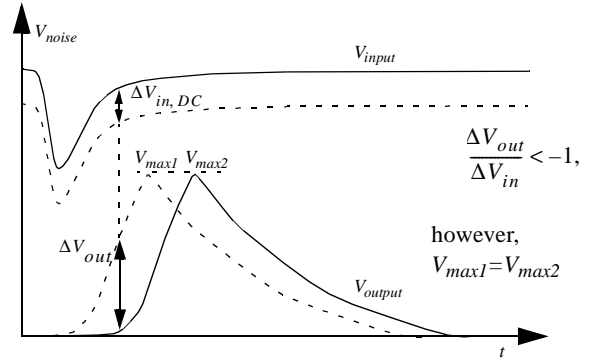


Figure 4. Error in sensitivity due to delay change.

variation and how to measure output noise variation. Both noise height and noise width are important for noise failure analysis. We therefore vary the input noise by adding an envelope to the noise as shown in Figure 5. This approach has the advantage that it increases both the input noise height and its width. For measuring the output noise, we measure the maximum pulse height, regardless of the point in time where it occurs and is therefore insensitive to changes in delay. However, it does not account for widening of the output noise pulse, which can worsen the impact of the noise. This could be accounted for by adding a weighted term for the noise width. In general, the failure criterion also has the same limitations as those discussed in Section 2, since it is based on a unity gain point.

The computation of the proposed failure criterion requires either a transient simulator able to compute transient sensitivities or performing two transient simulations. In our experiments we used the second option.

2.3 Latch transition failure criterion.

The fundamental way in which noise causes a functional failure is by changing the state of a memory element, such as a latch or dynamic gate. In the third approach, we therefore propagate noise, combining the propagated noise with injected noise at each circuit net, apply the propagated noise to a memory element and check if its state can be changed. To allow for a margin of error in the computed noise, we add additional noise at each stage to account for unexpected temperature or voltage fluctuation, and for error in the extraction and simulation. This safety margin will also ensure that each gate is not operating very close to the steep part of its transfer curve. One difficulty in this approach is correctly modeling the non-linear behavior of the driver gate when combining the propagated and injected noise, as discussed in Section 3. A second, diffi-

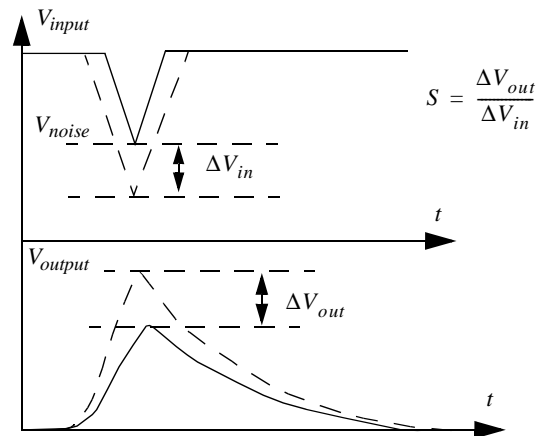


Figure 5. Dynamic gain criterion

culty is efficiently detecting the fact that a particular noise pulse can or can not be latched, as addressed in Section 2.4. The overall analysis process is outlined below:

- The circuit nets are sorted topologically to facilitate noise propagation from circuit inputs to its latches or outputs
- Each net is processed in topological order starting from circuit inputs so that at the time of processing net N connected to the output of a gate, we have computed the noise for each of its gate inputs.
- From all the gate inputs we select the one which will cause the worst propagated noise and combined it with the injected noise. We currently assume that noise coming from different inputs does not combine with each other, although the proposed method could be extended to simultaneous propagation of noise at multiple gate inputs.
- When noise is propagated to a latch, we check if it changes state.

One difficulty in noise propagation is analysis of long feedback loops, as shown in Figure 6. When the propagated noise on net B is calculated, the total amount of noise on net A is not known since it comes from a feedback loop. In this case, we initially propagate only the known input nodes (net $in1$ in Figure 6). When the noise on net A is subsequently computed, we need to propagate it to net B . If the propagate noise from net A does not exceed the propagated noise previously computed at net B , the analysis can be safely terminated. Otherwise, additional iterations of the analysis are necessary.

A noise pulse varies significantly while propagating from circuit input to a latch. It could be large at some point and then be attenuated by the subsequent gates especially if these nets have small injected noise. We report a noise failure only if we detect that the noise can be latched. Unfortunately, detecting a noise failure does not provide enough information for fixing the noise problem. For example, the failure can be fixed by reducing the injected noise at any of several nets along the noise propagation path. On the other hand it is possible that fixing a noise failure requires a reduction in the injected noise for several nets simultaneously. Therefore, for circuit designers, it is desirable to identify nets that contribute the most noise in the path. This problem can be addressed by identifying nets on the problematic path with high injected noise or with high dynamic gain. The information about ratio between injected and propagated noise at each net can also be helpful.

2.4 Detecting noise latching

An important problem in the proposed latch failure criterion is detecting when a propagated noise pulse at the input of a storage element changes its state. There are two types of storage elements: non-clocked (asynchronous) and clocked. For asynchronous storage element, such as an RS flop-flop, this problem can be solved by simple transient simulation while applying the noise pulse at its input. For clocked storage elements, such as the transparent latch shown in Figure 7(a), a more complex analysis is needed since the final state of the latch depends not only on the noise pulse height and width but also on the alignment of the noise pulse with the clock edge, as shown in Figure 7(b). The exact solution of this problem requires finding the worst-case alignment of the noise

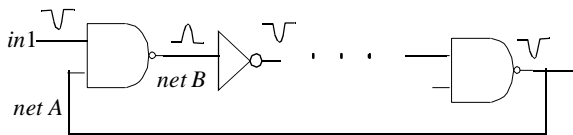


Figure 6. Circuit with feedback

pulse and clock signal, which can require a search involving many transient simulations.

To ensure an efficient analysis, we therefore propose a heuristic approximate technique that can make conservative conclusion about the possibility of latching a particular noise. We assume that the latch to be analyzed has a general structure with a feedback and input circuit, and that either or both of them are clocked.

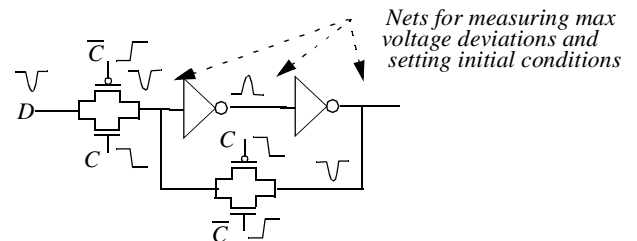
Our technique consists of the following steps:

1. Perform transient simulation of the latch in its transparent state with the noise pulse applied at its data input and register the maximal voltage deviations at each net of the latch feedback (Figure 7(a)). Note that the recorded voltages may occur at different points in time.
2. Set the latch to its non-transparent state and set the initial conditions for all internal latch nodes in its feedback equal to the maximal deviations recorded in the previous simulation.
3. Perform transient simulation of the latch. If the final state of the latch is the same as without noise it means that the noise cannot be latched at any possible alignment the clock signal.

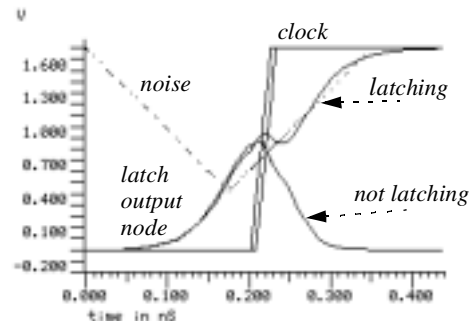
This technique is conservative meaning that it never predicts that noise cannot be latched when in reality it can. This follows from the fact that if we consider the waveforms at feedback nodes for any particular clock alignment (including the worst-case one) then the voltage levels of these signals at the time of the clock edge never deviate more from their stable values than the initial conditions that we used in step 2. Of course, this technique is pessimistic and could predict the noise is latched when in fact, it cannot. However, as shown in Figure 8(a) the error is small in practice.

2.5 Comparison of failure criteria

The results in Figure 8(b) show so-called *noise rejection curves* of the critical noise height as function of noise pulse widths. The static and dynamic unity gain based failure criteria are well correlated with each other and are more pessimistic than the noise latching criterion for short noise pulses while it is more optimistic for long ones. This is due to the fact that for short noise pulses the gate transfer curve is not very steep and we can exceed the unity gain point without causing a stability problem while for very wide noise pulses the transfer curve is very steep and even very small additional noise makes the circuit fail.



(a) Example of transparent latch with noise



(b) Noise latching and not latching due to clock alignment

Figure 7. Noise latching

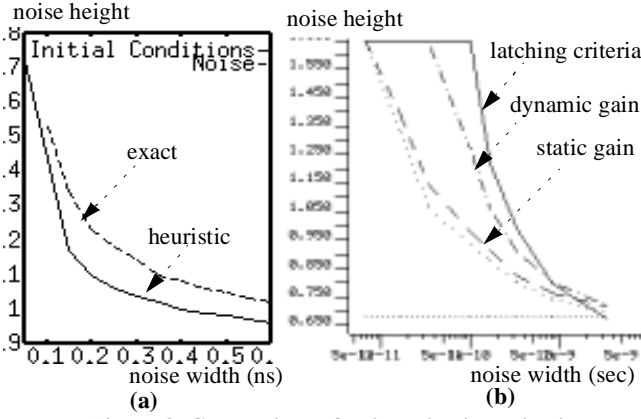


Figure 8. Comparison of noise rejection criteria

3 Combined injected and propagated noise

Noise injected by aggressor nets combines with noise propagated from the input of the victim driver gate, as illustrated in Figure 1. To efficiently compute the combined noise, analysis tools typically use linear models for the victim and aggressor driver gates. However, these linear models result in a significant underestimation of the actual noise. The straightforward approach to solving this problem is to perform non-linear simulation of the entire coupled interconnect and driver network. However, this approach is too slow and makes it difficult to determine the worst-case alignment between the propagated injected noise.

We therefore propose a new linear model, for accurate computation of the combined injected and propagated noise. In this model, the victim driver is represented with a Thevenin model consisting of a pulsed voltage source V_{ThP} and resistance R_H , as shown in Figure 9(b). These model parameters depend on the victim driver input noise v_{in} , as well as the total combined output noise v_{out} , in order to capture non-linearity of the victim driver. We assume that a linear aggressor driver model is computed using traditional methods [12] and the victim and aggressor receivers are modelled by simple grounded capacitances. For simplicity, we also assume that noise is applied to one input of the victim driver although the proposed technique can be generalized for noise propagated from several inputs as well.

3.1 Noise computation algorithm

After transforming the Thevenin models of the aggressor drivers into Norton equivalents, the nodal equations for the noise cluster can be written as

$$\left(C \cdot \frac{d}{dt} + G \right) \cdot V = J, \quad (\text{EQ } 2)$$

where C is the capacitance matrix, G is the conductance matrix, V is the vector of nodal voltages, and J is the vector of current sources. All the equations are linear except the one with the victim driver output current i_{out} which is non-linear and time dependent. The victim driver output current is expressed as a function of the victim input and output voltages, v_{in} and v_{out} where the victim input voltage $v_{in}(t)$ is a function of time t :

$$i_{out} = f_{load}(v_{in}, v_{out}) \quad (\text{EQ } 3)$$

$$v_{in} = f_{noise}(t) \quad (\text{EQ } 4)$$

Since solving (EQ3) and (EQ4) simultaneously as a non-linear system is very expensive and takes away the benefits of the linear models such as superposition and model order reduction, we propose to solve (EQ3) and (EQ4) separately and iteratively improve

the solution. We construct a parametrized victim driver Thevenin model $M_{Victim}(p_1, p_2, \dots)$ and add the equations describing this model to (EQ3) to make it linear and definite. The resulting system describes the linear model of combined noise where victim driver is represented with its Thevenin model shown in Figure 9(b). The parameters of this model can be, for example, Thevenin resistance, propagated noise height, etc. The resulting linear circuit can be solved using reduced order model techniques and the superposition principle. Exploiting its linearity we can easily find the worst noise alignment. Its solution is a linear estimation of the victim output voltage $v_{lin}(t)$ and current $i_{lin}(t)$. Substituting the estimation $v_{lin}(t)$ into (EQ4), we compute the non-linear estimates of the victim output current $i_{nonlin}(t)$. Comparing the linear and non-linear victim output current estimates, we then correct the parameters p_1, p_2, \dots of the victim model to improve current estimation. The discrepancy between the linear and non linear estimates of the output victim current is computed as the integral of their squared difference:

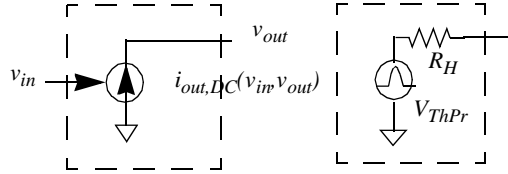
$$\int_0^T (i_{lin}(t) - i_{nonlin}(t))^2 dt \quad (\text{EQ } 5)$$

The corrected values of model parameters p_1, p_2, \dots, p_n are computed by minimizing this integral as their function $F(p_1, p_2, \dots, p_n)$. We find them by equating the partial derivatives of the function F to 0 and solving the resulting system of equations. With these refined parameters we repeat our iteration till convergence. It is obvious that if the linear and non-linear current estimates converge to be equal, they provide the exact solution of the original system of equations. Simultaneously, we find the parameters of the victim driver linear model. The overall algorithm is given below.

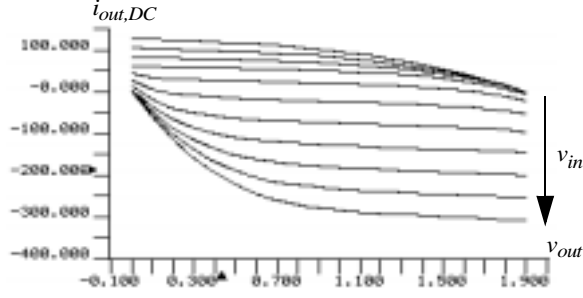
1. Compute initial values of victim model parameters p_1, p_2, \dots
2. Build linear system by combining equations (EQ3) and victim model equations.
3. Find linear estimations of the victim output voltage $v_{out}(t)$ and current $i_{lin}(t)$ by solving the built system using the worst alignment.
4. From nonlinear victim model (EQ4) find nonlinear estimations of the victim output current $i_{nonlin}(t)$.
5. Find the values of the victim model parameters p_1, p_2, \dots providing the minimum of the criterion $F(p_1, p_2, \dots, p_n)$.
6. If the value of the criterion $F(p_1, p_2, \dots, p_n)$ is more than desired accuracy and the number iterations done is less than the limit, repeat step 2.

3.2 Simplified non-linear victim driver model

In the above approach, we need to compute the victim output current $i_{out}(t)$ as a function of time. For the sake of efficiency, we model the victim driver as a non-linear current source (Figure 9 (a)). Its current $i_{out,DC}$ depends on both its input and output voltages: $i_{out,DC} = f_{load}(v_{in}, v_{out})$. Graphically this dependence is represented by a family of driver load curves (Figure 9(c)). For our noise computations, victim driver output current $i_{out,DC} = f_{load}(v_{in}, v_{out})$ is represented by a two dimensional table. Also, we use the DC victim driver voltage transfer characteristics expressing its output voltage as a function of the input voltage: $v_{out} = v_{out}(v_{in})$ (Figure 3(a)). This is given in a one dimensional table. The family of load curves and the transfer curve are computed only once during cell precharacterization by DC simulations sweeping input and output voltages and do not need to be recomputed at the time of noise analysis. Using input and output noise waveforms $v_{in}(t)$, $v_{out}(t)$ and the DC characteristics of the victim driver, we compute $i_{out}(t)$.



(a) non-linear victim driver model (b) linear victim driver model



(c) family of load curves

Figure 9. Victim driver models

3.3 Linear victim driver model

The best trade-off between accuracy and computational complexity was obtained by adjusting both propagated noise pulse height and width and assuming that the victim holding resistance R_H is constant. The Thevenin propagated noise pulse V_{ThPr} is rep-

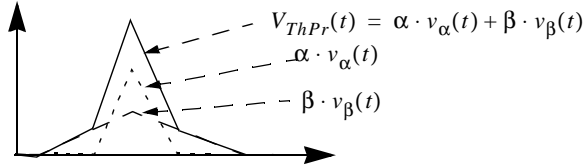


Figure 10. Propagated noise pulse for victim models

resented as a combination of two pulses of different width. Their heights α and β are considered as model parameters. The total propagated noise pulse is $V_{ThPr}(t) = \alpha \cdot v_\alpha(t) + \beta \cdot v_\beta(t)$, as shown in Figure 10. Substituting this expression into our error criterion, we obtain the function to minimize:

$$\text{Minimize} \int_0^T \left(\frac{v_{out} - \alpha \cdot v_\alpha - \beta \cdot v_\beta}{R_H} - i_{nonlin}(t) \right)^2 dt \quad (\text{EQ } 6)$$

The victim output noise voltage v_{out} can be represented as a sum of total injected and propagated noise $v_{out} = v_{inj} + v_{prop}$. As our circuit for noise propagation is linear, we express the propagated noise as $v_{out} = \alpha \cdot v_{prop,\alpha} + \beta \cdot v_{prop,\beta}$, where $v_{prop,\alpha}$ and $v_{prop,\beta}$ are the solutions of the linear model for noise propagation when the Thevenin propagated noise pulse is $v_\alpha(t)$ and $v_\beta(t)$ respectively. Substituting this into (EQ6) and solving for the values of α and β we obtain the equation shown in Figure 11. The proposed technique requires an initial estimation of the victim driver holding resistance R_H , which we compute from gate load curves using input voltage bias equal to 0.5 of the maximum propagated noise pulse. In order to avoid convergence problem we change the adjusted parameters at each iteration by not more than 20% because in computing new values of parameters we partly ignore the dependence of victim current on parameters variation.

4 Results

The proposed methods were implemented in a noise analysis

$$\alpha = \frac{\int_0^T \Delta v_\alpha \cdot \Delta v_i dt \cdot \int_0^T \Delta v_\beta^2 dt - \int_0^T \Delta v_\beta \cdot \Delta v_i dt \cdot \int_0^T \Delta v_\alpha \cdot \Delta v_\beta dt}{\int_0^T \Delta v_\alpha^2 dt \cdot \int_0^T \Delta v_\beta^2 dt - \left(\int_0^T \Delta v_\alpha \cdot \Delta v_\beta dt \right)^2}$$

$$\beta = \frac{\int_0^T \Delta v_\beta \cdot \Delta v_i dt \cdot \int_0^T \Delta v_\alpha^2 dt - \int_0^T \Delta v_\alpha \cdot \Delta v_i dt \cdot \int_0^T \Delta v_\alpha \cdot \Delta v_\beta dt}{\int_0^T \Delta v_\alpha^2 dt \cdot \int_0^T \Delta v_\beta^2 dt - \left(\int_0^T \Delta v_\alpha \cdot \Delta v_\beta dt \right)^2}$$

where: $\Delta v_\alpha = v_\alpha - v_{prop,\alpha}$, $\Delta v_\beta = v_\beta - v_{prop,\beta}$ and $\Delta v_i = v_{inj} - R_H \cdot i_{nonlin}$.

Figure 11. Computation of linear victim driver model

tool and were tested on industrial circuits. To test the accuracy of the linear models for combining propagated and injected noise, experiments were performed on net clusters from a high performance microprocessor, implemented in a 0.13 micron process as shown in Table 1. The net clusters rang in size from 122 to 236 elements. Each noise cluster was analyzed with three different input

Net	#Input noise height	Output noise				Error(%) (height/width)
		New approach		SPICE		
		height	width	height	width	
1	0.38	0.34	0.39	0.40	0.44	9.5/6.3
	0.76	0.37	0.43	0.41	0.55	9.7/21
	1.14	0.48	0.48	0.51	0.60	6.3/20.
2	0.38	0.32	0.35	0.31	0.45	3.2/20.6
	0.76	0.32	0.35	0.33	0.47	2.5/25.
	1.14	0.392	0.36	0.399	0.48	1.7/25
3	0.38	0.12	0.45	0.13	0.46	2.1/2.4
	0.76	0.13	0.46	0.14	0.50	3.6/8.2
	1.14	0.23	0.45	0.24	0.49	4.8/8.3
4	0.38	0.14	0.27	0.13	0.26	7.6/2.2
	0.76	0.16	0.28	0.17	0.31	7.1/9.3
	1.14	0.32	0.30	0.39	0.32	17.8/6.2

Table 1. Results of combined noise calculation

noise pulse heights at the victim driver input. The proposed approach provides good accuracy for both small and very high input and output noise. It also demonstrates that the accuracy of the noise height is higher than that of the noise width. This results from the fact that our integral criterion is only computed up to the peak of the noise pulse. Increasing the integration time improves the accuracy of noise width estimation at the expense of the noise height accuracy.

To compare the three discussed noise failure criteria, Table 2 shows the number of nets that failed in the noise analysis and their average noise slack (allowed noise height - actual noise height) on two industrial designs. *Block-1* is a large circuit block and *Chip-1* is a complete high performance microprocessor. Row 1 (static gain - no propagation) is the static gain failure criterion when the worst-case output noise is propagated. Row 2 (static gain - propagation) is the static gain failure criterion where the actual noise at the

receiver output is propagated. Row 3 (dynamic gain) corresponds to the dynamic gain failure criterion. Row 4 (latch criterion) is the latch transition failure criterion.

As can be seen, the number of failing nets decreases while average slack increases as we go from static - no propagation, to static-propagation, to dynamic noise failure criterion, as suggested earlier. On the other hand, when we propagate noise up to a latch and check for failure at the latch (latch criterion), no failures have been reported for both designs, which is consistent with the fact that both these chips were fabricated and tested in silicon with no noise related failures.

Noise criterion	#of failing nets/average slack	
	Block-1 31,489 nets	Chip-1 254,356 nets
Static gain - no propagation	82 / 285mV	2074 / 82mV
Static gain - propagation	14 / 405mV	341 / 260mV
Dynamic gain criterion	1 / 712mV	130 / 409mV
Latch criterion	0 / 1259mV	0 / 1103mV

Table 2. Results of use of different noise analysis criteria

Figure 12 compares the amount of slack obtained using four different noise failure criteria for 7500 nets of Chip-2 that could not be filtered out and were analyzed with detailed simulation. Each + sign corresponds to a net, whereas the solid line is a 45 degree line. The X-axis corresponds to the noise slack of the net using the static gain failure criteria without propagation, while the Y-axis corresponds to the noise slack of the net using one of the three other discussed noise failure criteria. A noise failure is reported when slack is negative. These plots confirm the data shown in Table 2 and also shed more light on the relative conservativeness of the noise failure criteria shown. As can be seen, the proposed latch transition failure criterion is significantly less conservative than unity gain based approaches.

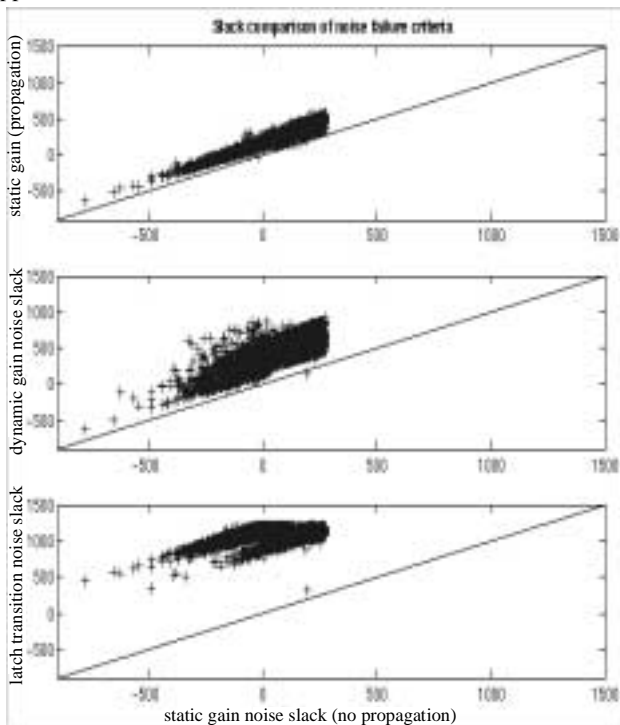


Figure 12. Comparison of noise failure criteria

5 Conclusions

In this paper we discussed to issues in noise analysis. First, we showed that using linear summation of the noise that is propagated through the driver of a net with the noise injected by capacitively coupled aggressor nets will significantly underestimate the actual noise on a net. We therefore propose a new linear model that accurately combines propagated and injected noise on a net, while maintaining the efficiency of linear simulation. The second issue addresses to how to determine if a noise pulse on a net can result in a functional failure. Traditional noise failure criteria are AC extensions of DC noise margins. We showed that these approaches can, in some cases, result in a pessimistic analysis, while in other cases, they allow circuit operation that is extremely close to regions that are unstable and do not provide sufficient margin of error. We compared the effectiveness of the discussed noise failure criteria and also discussed a method called the latch transition criteria, which addresses the drawback of the existing methods. The proposed methods were implemented in a noise analysis tool. We demonstrated that the proposed linear model for combining propagated and injected noise gives high accuracy compared with SPICE simulations. It was also demonstrated that the proposed latch transition failure criteria is significantly less conservative than the other noise failure criteria and that it was the only method that correctly identified zero noise failures for a design that successfully passed silicon testing without noise related problems.

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