Comprehensive Frequency-Dependent Substrate Noise Analysis Using Boundary Element Methods

Hongmei Li, Jorge Carballido, Harry H. Yu, Vladimir I. Okhmatovski, Elyse Rosenbaum, and Andreas C. Cangellaris University of Illinois at Urbana-Champaign, Urbana, IL 61801 Email: hli4@uiuc.edu

Abstract

We present a comprehensive methodology for the electrodynamic modeling of substrate noise coupling. A new and efficient method is introduced for the calculation of the Green's function that can accommodate arbitrary substrate doping profiles and thus facilitate substrate noise analysis using boundary element methods. In addition to a discussion of the application of the method and its validation in the context of substrate transfer resistance extraction, preliminary results from its application to frequency-dependent substrate noise modeling are presented also.

1. Introduction

System-on-a-chip, and mixed-signal circuits in general, promise great cost savings for both manufacturer and consumer, but they present new challenges for the chip designer, a significant one being noise coupling from digital blocks to analog blocks through the common silicon substrate. The physical picture is one of current injection into the substrate; as the carriers travel toward the substrate contacts for collection, they induce potential variations across the substrate. This, in turn, causes fluctuations in the threshold voltage of MOS devices whose bodies lie in the substrate, as well as displacement current flow into circuit nodes. Design guidelines for minimization of substrate noise coupling have been formulated [1]. For example, since switching noise on the ground bus can be severe, the substrate is directly contacted using a quiet ground. Digital circuits that are known to inject a large substrate current, such as output buffers, are surrounded by guard rings. Triple-well technology can be employed for shielding of sensitive analog circuitry. Digital blocks with a large switching activity are placed far away from analog circuitry. All of these practices have an associated cost in terms of area, and the efficacy is highly dependent on the substrate doping and noise signal frequency. In order to provide sufficient isolation with minimum area penalty. and in order to learn how to provide isolation given that the dominant noise frequency components are increasing, simulation tools are needed.

Noise-sensitive circuit blocks are generally the analog or RF blocks; these tend to be small and thus it's feasible to simulate them using a detailed, SPICE-type, circuit simulator. Our proposal is to place current-controlled voltage sources (CCVS) at critical nodes in the netlist of these blocks in order to capture the effect of noise injection through the substrate. The CCVS coefficient is set equal to the transfer impedance between the noise injector and the noise sensor [2]. This paper presents a

methodology for extracting transfer impedances given a chip layout and description of the technology. Our method is novel in its ability to handle arbitrary substrate doping profiles without sacrificing computational efficiency.

For convenience, we assume p-type substrate throughout the rest of the paper. Although noise may be injected into the substrate from an n+ diffusion or an n-well via capacitive coupling, once the current is in the p-substrate it travels primarily through p-type regions (the substrate, channel stops, p⁺ buried layers) because, at low and moderate frequencies, these provide the lowest impedance path. Thus in our initial analysis, we treat certain features which lay between the noise injector and noise sensor, such as n-wells and trench isolation, as open circuits. Furthermore, for sufficiently low noise signal frequencies, we can model the substrate using transfer resistances, as opposed to transfer impedances. Consider for example, a sinusoidal signal of frequency f; the corresponding current density in the substrate is given by $\vec{J} = (s + j2p fe)\vec{E}$, where σ is the conductivity of the silicon substrate, ε is the permittivity and \vec{E} is the electric field. For sufficiently low signal frequencies, the substrate behaves resistively, i.e., $\vec{J} \approx s\vec{E}$. An RF circuit might be fabricated on a lightly doped substrate in which $\sigma = 20 \Omega$ -cm [3]; in this case, the displacement current would exceed the conduction current for f > 7.6 GHz and at which point the substrate could not be well modeled using transfer resistances. Most ICs are built on more heavily doped substrates. Therefore, the first part of this paper will focus primarily on extraction of a transfer resistance model of the substrate.

Substrate noise modeling presents two interrelated challenges. The first one is development of an efficient methodology for extraction of the transfer resistances. The second one is how to contain the complexity of the substrate topography; this challenge is compounded by the fact that the substrate features are of dimensions on the order of microns, while the distances over which transfer impedances need to be extracted are on the order of 10s and 100s of microns. Clearly, the modeling methodology needs to address this complexity [4], [5]. While finite-difference based methods (e.g. [1]-[3], [6]-[7]) provide superior modeling versatility, they are hindered by the need to discretize the entire volume of the substrate, thus becoming prohibitively large when dealing with realistic problems. Integral equation methods, on the other hand, utilize a smaller number of unknowns, since only the surfaces of substrate taps, wells, and other boundaries between substrate features of different electrical properties need to be discretized for the

numerical solution. Among the various boundary element methods proposed to date for the solution of the integral equation statement of the transfer resistance extraction problem, the fast multipole method [8], the pre-corrected FFT method [9], [10], and the singular value decomposition (SVD)-accelerated scheme of [11], are the ones best suited to handle the computational complexity of the problem.

Of particular importance in the efficient implementation of boundary element methods is the ability to use in the integral equation a Green's function that accounts for the layered (i.e. non-uniformly doped) nature of the substrate. In Section 3, we present a very systematic and efficient method for construction of Green's functions for layered substrates. This methodology has several important attributes that set it apart from other commonly used approaches for the calculation of Green's function in layered media, two of which are the following. First, the Green's function is obtained in a closed-form expression, irrespective of the complexity (i.e., number of layers or doping profile variation with depth). Second, its extension to the general electrodynamic case, which may be needed for proper prediction of substratecoupled noise at multi-GHz frequencies, can be affected with only slight modifications. These attributes of the proposed Green's function construction and their impact on enhancing layered substrate modeling versatility and solution efficiency have been discussed in detail in [12], [13] and [14].

The presentation in this paper begins with the description of the layout extractor, the output of which are input decks for the transfer impedance extractor and the circuit simulator; this is described in Section 2. Section 3 provides the details of the development of the field solver for transfer resistance extraction. The need for a frequency-dependent field solver and a brief overview of the methodology for its development are presented in Section 5.

Despite its computational efficiency and modeling versatility, the proposed field solver is still limited in its ability to do fullchip analysis for large ICs where thousands or tens of thousands of substrate contacts may be involved. Roadblocks include the time and storage requirements for full-chip layout extraction. One may address this by performing a series of small-scale studies to develop heuristics for systematic substrate complexity reduction through several means, such as the thresholding of low-sensitivity interactions and the lumping of multiple noise sources when dealing with interactions between distance blocks. Some preliminary results from such studies are presented in Section 4. Following layout extraction, complexity may be further reduced by exploiting ways in which the quantification of the sensitivity of a given "victim" contact to another "aggressor" contact may be utilized to sparsify the resistance/impedance matrix [4].

2. Layout Extraction

The inputs to the layout extractor are the layout description in GDS-II format and a technology file. The technology file allows the extractor to map the layout description into a 3-D description of the substrate: conductivity at any point (x, y, z). The extractor also constructs the netlist.

2.1 Technology File

Substrate features, such as p-wells or n⁺ buried layers, are defined as combinations of layout layers; the combinations are

made using the Boolean operators AND (·), OR (|) and NOT (!), and the additional operators DON'T CARE (&*) and CONDITIONAL DON'T CARE (&+). The latter operator is used for the specific case in which a feature is defined as the Boolean combination of specific layers plus the condition that one layer of any type besides those explicitly cited must also be present. Each substrate feature defined using this algebra is further described in the technology file by its starting and its stopping z-coordinates, given that the surface of the Si substrate is located at z=0. The conductivity (i.e., doping) is also listed as a function of z. Sample lines from a technology file are shown in Fig. 1.

```
% Comment lines start with %
% Substrate Features Description Example- BiCMOS
% Substrate Definition
% P-type substrate. layout layer number = 0.
\% Z dimensions from \dot{0} to 200 microns, non - uniform doping
SUB_LAYER P_TYPE 0 Z=0 Z=200u P [1.2u 5e16] [200u 1e16]
% Substrate Tap Definition
% P-Diffusion layer = 44, N-well layer = 42
SUB TAP 44 !42 &* Z=0 Z=0.2u
% N-well Definition
% Uniform doping 3e16
NWELL 42 &* Z=0 Z=2u 3e16
% P-well Definition
% This technology does not have p-well
% Buried N Laver
% Uniform doping 1e19
B_N_LAYER 42 &* Z=2u Z=3.5u 1e19
% Buried P Laver
% Uniform doping 3e19
B P LAYER 45 &* Z=1.2u Z=3.2u 3e19
% Substrate Tap Contact Definition
% Active layer = 43
CONTACT 44 43 !42 &*
% Interconnection Layer
% Metal 1 layer = 49, sheet resistance = 0.15
INTERCONNECT 49 0.15
```

Fig. 1. Technology file example. The last two commands, CONTACT and INTERCONNECT, are needed for interconnect resistance extraction between substrate taps.

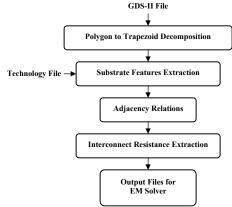


Fig. 2. Flowchart of the substrate extractor. It has two input files: layout description (GDS-II file) and substrate features description (technology file).

2.2 Substrate Extractor

A flowchart of the substrate extractor is shown in Fig. 2. The extractor's first procedure parses the layout area into multi-layer trapezoids. The second procedure extracts features matching a description in the technology file. All features extracted are rectangles as required by our field solver. The third procedure adds the third dimension to the extracted features. Adjacency relations among the extracted features are identified. For each feature, i.e. parallelepiped, there are six arrays corresponding to its six faces. Each of the elements in these arrays is a data structure that stores the type of neighbor feature and the coordinates that limit the shared surface. Since non-overlapping of the features is assumed, redundancy of information is avoided by not storing the common coordinates between two neighbors. These data are passed to the field solver, along with the interconnect resistance between substrate taps.

Noise sources and sensors are identified by the user. They are given to the extractor as pairs of (x, y) coordinates, which can be easily obtained from a layout editor such as Virtuoso Layout Editor from Cadence by just positioning the mouse over the desired region. Source and sensor locations are passed by the extractor to the field solver with the appropriate z coordinate added. The depth coordinate is obtained by considering what features are present at (x, y) to ensure any source or sensor lies in the pure substrate.

As noted previously, a finite amount of computer memory can make full-chip extraction infeasible. Therefore, the extractor can do a limited extraction of user-specified cells. The cells are placed relative to one another at the correct distance, and the correct substrate doping profile is used everywhere, but substrate features (wells, taps, trenches, etc) located outside the cells are lost. In many cases, this has very little impact on the extracted transfer resistance.

2.3 Interconnect Resistance Extraction

Ideally, all substrate taps would be at the same potential. But in reality, there may be unequal ohmic drops from the pad to the various substrate taps. To enhance the accuracy of the transfer resistance extraction, the user may choose not to tie each substrate tap to a fixed potential (usually Ground) but, instead, have the solver find transfer resistances with a resistive network placed between the pad voltage and the substrate taps. The layout extractor provides values for these resistances [15].

2.4 Netlist Extraction

Devices are identified based on the layer composition of each node of the device and its adjacency relations to other nodes. For example, an NMOS is identified by the layer composition of the gate (G), the drain (D) and the source (S), and their adjacencies given by the pairs (G, D) and (G, S). Further details about the algorithm can be found in [16]. Although conventional layout extractors do not include the well-substrate capacitances in the netlist, this extractor can do so. These capacitances need to be considered during circuit simulation if they are the points at which noise is coupled into and out of the substrate. The netlist for circuit simulation must also contain current-controlled voltage sources, where the source coefficients are the transfer resistances. These sources are automatically inserted in the netlist following transfer resistance extraction. To do this, a mapping from the (x, y) coordinates of a noise source or sensor to a netlist node is made. This task is achieved by a simple matching of the

physical location of a source or sensor to the area covered by one of the nodes from the extracted devices.

3. Transfer Resistance Solver

As noted in the introduction, the transfer resistance solver uses the layout information and substrate doping profile from the layout extractor as input, solves the integral Poisson's equation using the boundary element method (BEM), and outputs the transfer resistances between the source points and the sensor points. A fast BEM solver requires derivation of an appropriate Green's function that takes into account the (possible) non-uniform conductivity of the substrate. A systematic methodology for the development of such a Green's function is presented next.

3.1 Green's Function Derivation

The development of a layered-medium Green's function is a very well addressed problem in applied electromagnetics, and the final form is in terms of either a slowly converging double infinite summation or in terms of a semi-infinite integral. Both of these are very expensive to compute. To overcome this difficulty, different techniques have been derived, such as [6][11][17]. These methods are either restricted in the number of substrate layers, or become computationally inefficient for large lateralsized substrates due to the lack of closed-form expressions for the Green's function. One commonly used approach to tackling the computational complexity of the layered Green's function calculation is a pre-calculation of the Green's function followed by a table-lookup. This reduces significantly the overhead associated with the online calculation of the Green's function; however, the amount of time required for the generation of the tables can be on the order of several hours, depending on the complexity of the substrate. Next, we will introduce an accurate closed-form Green function for layered media, which can be used to reduce dramatically this pre-processing time. Furthermore, it also may be used for on-the-fly calculation of the Green's function for the BEM solver.

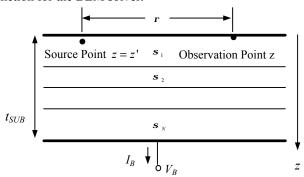


Fig. 3. Illustration of the layered substrate for calculating the Green's function. **s** is the conductivity which varies for each layer, t is the thickness of the substrate, and z is the vertical axis. The source is located at z', the observation point is located at z, and the horizontal distance between the source point and the observation point is **r**. The backside of the substrate is either grounded $(V_B = 0)$ or floating $(I_B = 0)$.

The geometry of the layered substrate for which the Green's function is obtained is shown in Fig. 3. The proposed methodology was first presented in [12] in the context of the solution of Poisson's equation in layered dielectrics for the purposes of capacitance extraction. The derivation assumes that the noise source is located at a depth z', the sensor point is

located at a depth z, and the separation between the source point and the sensor point in the x-y plane is \mathbf{r} . The Green's function denoted by $g(\mathbf{r}, z, z')$ is the solution to the generalized form of Poisson's equation subject to appropriate boundary conditions at material interfaces,

$$\nabla \cdot (\mathbf{s}(z)\nabla g(\mathbf{r}, z, z')) = -\frac{\mathbf{d}(\mathbf{r})}{2\mathbf{p}\mathbf{r}}\mathbf{d}(z-z'). \tag{3.1}$$

The spectral domain form of (3.1) is constructed by applying the discrete approximation of the Fourier-Bessel transform, and is given by

$$\frac{d}{dz}\left(\mathbf{s}(z)\frac{dG(\mathbf{I},z,z')}{dz}\right) - \mathbf{I}^{2}\mathbf{s}(z)G(\mathbf{I},z,z') = -\frac{1}{2\mathbf{p}}\mathbf{d}(z-z'). \quad (3.2)$$

Its numerical solution using the method of finite differences yields the matrix equation,

$$([A] - \mathbf{I}^2[I]) \cdot [G] = [F] \cdot [U]. \tag{3.3}$$

It is noted that since a finite difference method is used to solve (3.2), arbitrary variation in doping profiles can be handled, contrary to traditional layered media Green's function construction methods that rely on the analytic solution of (3.2). In (3.3), [A] is a tri-diagonal matrix, [I] is the identity matrix, [U] is a unit vector with one at the source plane and zeroes elsewhere, and [F] is a diagonal matrix. The dimension of the linear system in (3.3) is N, equal to the number of points in the finite-difference grid. As explained in [12], the solution of (3.3) utilizes the eigen-decomposition of the matrix [A], $[A] = [P][S][P]^{-1}$. Thus, the result for the spectral form of the Green's function is cast in a pole-residue form that enables the calculation of its inverse Fourier-Bessel transform in closed form,

$$g(\mathbf{r}, z_i, z_j') = -\sum_{k=1}^{N} P_{ik} \mathcal{Q}_{kj} K_0\left(\sqrt{|S_k|}\mathbf{r}\right), \qquad (3.4)$$

where $[Q]=[P]^{-1}[F]$ and K_0 is the modified Bessel function of order 0. Since [P], [Q] and [S] in (3.4) describe the properties of the substrate and they need only be computed once for a given substrate, the closed-form Green's function can be calculated efficiently for any arbitrary doping profile. Such a closed-form expression for the Green's function in layered media facilitates significantly the development of fast solvers for complicated, layered substrates. For example, considering the common practice of the development of a hash table for the fast on-the-fly calculation of the Green's function in a fast integral equation solution methodology such as the Pre-Corrected FFT method [9]. such a table can be developed quickly and with ease, irrespective of the complexity of the substrate.

In order to verify the numerical implementation of the proposed methodology and to examine the accuracy of the generated Green's function, use was made of the fact that the Green's function describes the transfer resistance for the case of a point source and a substrate that is uniform in the x and y directions (i.e., no diffusions, wells, trenches, etc.). For this simple geometry and for a variety of substrate doping profiles, we calculated the transfer resistance using the 3D finitedifference (FD) method [2][18] and compared the value with that given by the newly derived Green's function. Furthermore, an analytic Green's function may be derived for the case of a uniformly doped substrate by using image theory.

Table 1 compares the various Green's functions for five different cases. Results for both uniformly doped and nonuniformly doped substrates are presented. The difference between the newly derived Green's function and the analytic Green's function is less than 0.35%. The difference between the new Green's function and the transfer resistance from the FD method is less than 6%, and we attribute this spread to inaccuracy of the FD calculations - the number of grid points was limited in order to save time and memory. Indeed, the FD calculations had an error of 5% compared to the analytical Green's function. In Fig. 4, the newly derived Green's function is compared with the analytic Green's function over a large range of r. The two curves are indistinguishable.

Case	Derived Analytic GF GF		Transfer resistance from FD	
1	1443.84	1436.5	N/A	
2	132.40	132.51	125.53	
3	0.1319	N/A	0.1250	
4	16.36	N/A	16.68	
5	54.33	N/A	52.36	

Table 1. Comparison of the derived Green's function (GF) given by (3.4), the analytic GF given by image theory, and the transfer resistance calculated using the FD method, for five different cases ($t_{SUB} = 200$ mm for all cases).

Case 1:
$$I_B = 0$$
, $\mathbf{r} = 100 \,\mu\text{m}$, $N_{SUB} = 10^{15} \text{cm}^{-3}$,
Case 2: $V_B = 0$, $\mathbf{r} = 100 \,\mu\text{m}$, $N_{SUB} = 10^{15} \text{cm}^{-3}$,

Case 3:
$$V_B = 0$$
, $\mathbf{r} = 100 \ \mu\text{m}$, $N_{SUB} = \begin{cases} 10^{15} \ \text{cm}^{-3}, \ 0 \le z < 2 \, \text{mm} \\ 10^{19} \ \text{cm}^{-3}, \ 2 \le z \le 200 \, \text{mm} \end{cases}$

Case 4:
$$V_B = 0$$
, $\mathbf{r} = 100 \, \mu \text{m}$, $N_{SUB} = 10^{(17 - Z/50 \mu \text{m})} \text{cm}^{-3}$,

Case 5: $V_B = 0$, $\mathbf{r} = 100 \,\mu\text{m}$, $N_{SUB} = 10^{(16 - Z/100 \mu\text{m})} \text{cm}^{-3}$

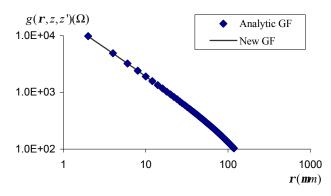


Fig. 4. Comparison between newly-derived and analytic Green's functions (GF) for a uniformly doped substrate. Substrate doping is 10^{15} cm⁻³, thickness of the substrate is 200mm, and $V_B = 0$.

The implementation of the Green's function in an integral equation solver requires availability of the derivatives of the Green's function. Radial derivatives are calculated analytically using the results:

$$\frac{\partial g}{\partial x}(\mathbf{r}, z_i, z_j') = \frac{x - x'}{\mathbf{r}} \sum_{k=1}^{N} P_{ik} Q_{kj} \sqrt{|S_k|} K_1 \left(\sqrt{|S_k|} \mathbf{r} \right), \quad (3.5a)$$

$$\frac{\partial g}{\partial y}(\mathbf{r}, z_i, z_j') = \frac{y - y'}{\mathbf{r}} \sum_{k=1}^{N} P_{ik} Q_{kj} \sqrt{|S_k|} K_1 \left(\sqrt{|S_k|} \mathbf{r} \right), \quad (3.5b)$$

where K_1 is the modified Bessel function of order 1. The vertical derivatives are calculated numerically using the finite difference approximation

$$\frac{\partial g}{\partial z} \left(\mathbf{r}, z_i, z_j' \right) \bigg|_{z_i} = \frac{g \left(\mathbf{r}, z_i, z_j' \right) - g \left(\mathbf{r}, z_{i+1}, z_j' \right)}{z_i - z_{i+1}}.$$
 (3.6)

The accuracy of the derivatives of the Green's function were verified by comparing them with those of the analytic solution, obtained for the case of a uniform substrate. The comparison is depicted in Fig. 5. Excellent agreement is observed with the difference remaining below 1%.

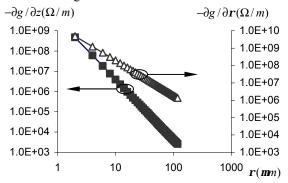


Fig. 5. Verification of $\P g/\P z$ and $\P g/\P r$. Data points are for the analytic Green's function, while solid lines are those for the derived one. $N_{SUB}=10^{15}\,\mathrm{cm}^{-3},\,t_{SUB}=200\,\mathrm{mm},\,\mathrm{and}\,V_B=0.$

3.2 Boundary Element Method

The boundary element method we implement is well known. It is based on the integral form of Poisson's equation

$$\mathbf{a}\Phi(\vec{r}) = \int_{S} \mathbf{s} \left(\vec{r}'\right) \left(\frac{\partial \Phi(\vec{r}')}{\partial n} g(\vec{r}, \vec{r}') - \frac{\partial g(\vec{r}, \vec{r}')}{\partial n} \Phi(\vec{r}') \right) dS', \quad (3.7)$$

where α =1 for observation points inside the volume of interest, α =0 for observation points exterior to the volume of interest, and α =1/2 for points on the boundary S. If the Green's function satisfies the conditions of potential and normal current density continuity at layer interfaces, the only surface boundaries present in the integral equation are those associated with the contact areas, trench isolations and the wells. Consequently, the potential and its normal derivative on these surfaces are the only quantities relevant to the development of the desired transfer resistance matrix.

Substrate taps or guard rings (p+ diffusions)

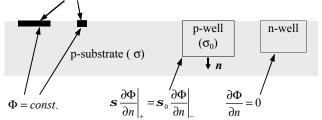


Fig. 6. Illustration of the boundary conditions for the BEM. s is the conductivity of the substrate which varies for each layer. The substrate taps and guard rings are equipotential surfaces. A p-well has a current continuity boundary condition, and an n-well is treated as an open circuit in this static analysis.

Fig. 6 depicts the various types of boundary conditions pertinent to semiconductor substrate modeling. The noise source may be modeled in four different ways: (1) a point source with current I, (2) evenly distributed current density on the boundary, (3) some known distribution of current density on the boundary, (4) an equipotential surface. The substrate taps and guard rings are set to potential 0 if the interconnect resistance is negligible, and are modeled as equipotential surfaces otherwise. A p-well

has a current continuity boundary condition, and an n-well is treated as an open circuit in this static analysis. Trench isolation is also modeled as an open circuit for the static problem.

The numerical approximation of (3.7) using the method of moments is well known and will not be discussed here. Table 2 compares results for the transfer resistances extracted using this BEM solver with those obtained using a 3D FD solver. The test structure under study is shown in Fig. 7. Transfer resistances obtained from the BEM solver agree well with those calculated using the finite difference method. Furthermore, Table 3 demonstrates the superior computational efficiency of a BEM over a finite difference solver. As already mentioned in the Introduction, one of the primary reasons for the enhanced efficiency is that the number of unknowns in the BEM method scales with the surface area of substrate taps, guard rings, and wells, while for the finite difference method, this number scales with the volume of the substrate block that is being modeled. Furthermore, even though the BEM matrix is dense, the implementation of a fast iterative solution process similar to the pre-corrected FFT method of [9] enables efficient storage complexity and CPU solution time management, both of which scale as $O(N\log N)$ where N is the number of unknowns.

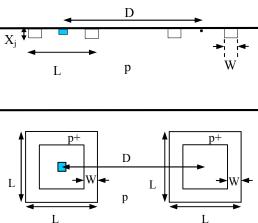


Fig. 7. Cross-sectional and top view of the example test structure. It has one source of 4 mm by 4 mm and a sensor placed D (mm) away from the source. A guard ring is placed around the source, or the sensor, or both. The guard ring width is W and its length is L. The depth of the guard ring is X_i .

4. Case Studies

Case studies have been performed to validate the static field solver, to develop layout guidelines, and to develop heuristics for simplifying the complexity of the IC representation being analyzed. A few of the interesting findings are presented in this section

A guard ring placed around either the sensor or the injector typically reduces the transfer resistance (i.e, noise coupling) by a factor of 10, assuming a bulk substrate is used. Lower returns are provided by addition of a guard ring around the second element; transfer resistance is reduced by another factor of 4 or so. The guard ring structure simulated was illustrated in Fig. 7. The area versus isolation trade-offs for one case are summarized in Table 4. Increasing the guard ring width has a direct impact on the isolation (Table 5); transfer resistance decreases as the guard ring area increases. Decreasing the guard ring length (L) has surprisingly little effect on transfer resistance, for bulk substrates

(Table 2). As the guard ring is made smaller, it lies closer to the source/sensor, which tends to reduce the transfer resistance. At the same time, its surface area decreases, which tends to increase the transfer resistance. The two effects mostly cancel each other out. For epi substrates, the result is quite different; transfer resistance increases significantly as the guard ring length is made smaller, until its separation from the source/sensor is on the order of the epi layer thickness; in other words, the area effect is more important than the proximity effect.

L (mm)	Method	Source Ring Only	Sensor Ring Only	Both Rings
60	FD	151.9	155.6	28.7
00	BEM	146.7	146.7	26.6
80	FD	151.2	151.5	33.8
80	BEM	147.7	147.7	33.6
100	FD	135.7	134.8	37.5
100	BEM	141.1	141.1	39.5

Table 2. Calculated transfer resistance for three different test cases. $N_{\rm SUB}=10^{15}~{\rm cm}^{-3}$, $t_{SUB}=200~{\rm mm}$, $I_B=0$, $D=120~{\rm mm}$, $W=10~{\rm mm}$, and $X_j=0.2~{\rm mm}$. Transfer resistances obtained from the BEM solver agree well with those calculated using the FD method. The data also show that by placing dual rings around source/sensor, the coupling can be significantly reduced.

Case	FD	BEM
Sensor ring	10281 s	19 s
Source ring	10281 s	19 s
Both rings	10281 s	78 s

Table 3 Computation time comparisons show that our BEM solver is significantly faster than a FD solver. This FD solver implements a fast sparse solver in an adaptive gridding sense [2].

Structure	Area Penalty (nm²)	Transfer Resistance (W)	
No isolation	0	1491	
Single ring	1500	147.7	
Dual ring	3000	33.6	

Table 4. Area vs isolation. Single ring refers to the placement of one guard ring around either the sensor or the source; dual ring means that two guard rings are present, one around the source and another around the sensor. ($D=120\,\mathrm{mm}$, $W=10\,\mathrm{mm}$, $L=80\,\mathrm{mm}$, $N_{SUB}=10^{15}\mathrm{cm}^{-3}$). Grounded substrate taps were placed outside the guard rings in these simulations.

Ring Width W (mm)	Transfer Resistance Rt (W)		
10	33.6		
20	12.1		
30	2.4		

Table 5. Transfer resistance decreases as guard ring width increases for a dual ring scheme. (D=120mm, L=80mm, $N_{SUR}=10^{15}$ cm⁻³).

In a given design, the primary noise sources may be few in number and easily identifiable, for example, output drivers. Or, a digital block with a large activity factor may be the noise source. In this case, the number of nodes from which current is injected can be large. Rather than providing a transfer resistance between each of these nodes and each noise-sensitive node, and then needing to perform detailed circuit simulation of both the noisy block and the noise-sensitive block, it may be preferable to precharacterize the substrate current injection from the digital block and then represent it as one noise source [19]. Preliminary case studies indicate that if the noise sources are not surrounded

by guard rings (or if they all lie within a single guard ring), it is usually acceptable to lump the multiple sources into one equivalent source located away from the sensor at a distance equal to the average spacing between all the sources and the sensor (Table 6).

	D ₁ (mm)	D ₂ (mm)	D ₃ (1111 11)	R _t (W)	D _{eq}	R _{teq} (W)	Error
ĺ	120	120	N/A	1494	120	1494	0%
	120	600	N/A	1400	360	1356	3.1%
	120	1440	N/A	1356	780	1279	5.7%
	120	120	120	1494	120	1494	0%
	120	90	600	1450	270	1386	4.4%

Table 6. Transfer resistances of multi-source structures versus lumped source structures. No guard rings surround the sources or the sensor, $N_{SUB}=10^{15} {\rm cm}^{-3}$. D_1 , D_2 , and D_3 represent the distances from source1, source2 and source3 to the sensor, respectively. $D_{\rm eq}$ represents the distance from equivalent source to sensor. $R_{\rm t}$ and $R_{\rm teq}$ are the transfer resistances of original structure and the equivalent structure, respectively.

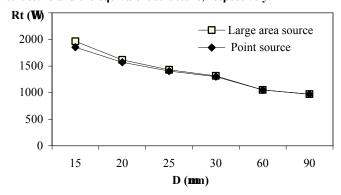


Fig. 8. Transfer resistance of a large area source and a point source. The large noise source has an area of 25mm x 25mm, the sensor is a point sensor at a varying distance D away from the source and there is a 4mm x 4mm substrate tap 10mm behind the sensor. P-type bulk substrate $(N_{SUB} = 10^{15} \text{ cm}^{-3})$.

Relative to a point source, a distributed noise source will increase the computational time by increasing the number of Green's functions that need to be calculated. Therefore, it is desirable to model it as an equivalent point source whenever possible. Fig. 8 compares the transfer resistance of a distributed source with that of a point source, as the separation between the source and sensor increases, for the case of a lightly doped bulk substrate. The transfer resistance of a distributed source is similar to that of a point source located at its center. The same result is found for heavily doped bulk substrates. For epitaxial substrates, the point source approximation is only valid when D/P > 1.2, where D is the distance from the center of the source to the sensor and P is the dimension of the (square) distributed source.

If guard rings surround the noise source(s) and sensor, there is usually negligible loss of accuracy and considerable speed-up if the chip regions outside the rings are modeled as feature-free p-substrate. Even for the (realistic) case that only the noise sensor has a guard ring, substrate taps (and presumably other features) outside this ring can often be ignored unless they lie very close to the source ($S \le 3/5 \cdot (D - L/2)$, D and L are defined in Fig. 7, S is the separation from the center of the noise source to the substrate tap), or they lie directly on the line between source and sensor. The preliminary results suggest that limiting the

region of detailed extraction to just a few cells will provide sufficient accuracy.

5. Transfer Impedance Solver

As noted in the introduction, high resistivity substrates are often used for RF circuits and, in this case, it is important to take into account electrodynamic effects. High performance digital circuits are usually built on low resistivity (e.g., 0.05 Ω -cm) substrates to avoid latch-up, and the active devices are fabricated in a relatively lightly doped layer epitaxially grown on the wafer top surface. Even though for such substrates the effect of displacement current is insignificant beyond 100 GHz, another electrodynamic effect, the skin effect, may be important and must be modeled for accurate transfer impedance calculation.

To illustrate the importance of properly modeling the electromagnetic behavior of the semiconductor substrate, we simulated the effective surface impedance $Z_S(f)$ for two different cases of layered substrates. The effective surface impedance [20] provides a first-order approximation of the impedance seen by a voltage source connected between two square electrodes of width w and placed at distance d from each other, provided that d is small compared to the wavelength. This impedance may be approximated by

$$Z(f) = Z_S(f) \frac{d}{w}.$$
 (5.1)

The first substrate considered, Substrate A, is a three-layer, low-resistivity substrate with layer resistivities and thicknesses (from top to bottom) as follows: (1.25 Ω -cm, 1.2 μm), (12.5 Ω -cm, 0.8 μm), (0.01 Ω -cm, 198 μm). Substrate B is a two-layer, higher resistivity substrate, with layer resistivities and thicknesses (from top to bottom) as follows: (20 Ω -cm, 2 μm), (5 Ω -cm, 198 μm). Simulation results are shown in Fig. 9. Note that for the case of the higher resistivity substrate (Substrate B) the effective surface impedance exhibits an increasing capacitive component as signal frequencies become high. For the case of the lower resistivity Substrate A, it is the skin effect that becomes dominant at higher frequencies and the effective surface impedance exhibits an increasing inductive part.

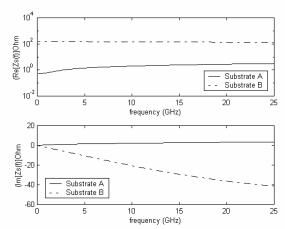


Fig. 9. Resistive and reactive parts of the effective surface impedance of a low-resistivity (Substrate A) and a high-resistivity (Substrate B) multi-layered Si substrate.

Clearly, unless a comprehensive electromagnetic model is put forth with electromagnetic induction and displacement current effects taken into account, semiconductor substrate noise coupling cannot be done properly for the multi-GHz, mixedsignal VLSI designs of the near future. The development of electromagnetic models for substrate coupling is currently in its infancy.

The development of a numerical model for the quantification of frequency-dependent substrate noise coupling is based on the integral equation formulation of the Maxwellian system in terms of the magnetic vector potential \vec{A} and the electric scalar potential Φ . In terms of these potentials, the electric field intensity vector is written as [20]

$$\vec{E}(\vec{r}) = -j \vec{w} \vec{A}(\vec{r}) - \nabla \Phi(\vec{r}). \tag{5.2}$$

The two potentials are obtained as integrals of the surface electric current and charge densities on substrate taps, guard rings, and, in general, all boundaries between substrate features of different electrical properties. The only boundaries that are not discretized are planar boundaries that may be assumed to be of infinite extent. The electromagnetic field discontinuities at these interfaces are handled implicitly through the construction of appropriate Green's functions for the aforementioned potentials in layered media. As demonstrated in [13], [14], the methodology used for the fast, closed-form calculation of stratified-media Green's functions for Poisson's equation can be extended to the electrodynamic case in a rather straightforward fashion.

As a preliminary application of our electrodynamic substrate coupling extractor, we provide the following example of substrate-induced noise coupling. At this point it is appropriate to mention that for proper modeling of noise coupling in the electrodynamic case, attention needs to be paid to the use of proper models for both the source of the noise and the way noise is quantified at the sensor (victim circuit). To elaborate, in this example, the noise source considered is noise current injected into the substrate from an n⁺ diffusion or an n-well via capacitive coupling. Instead of a detailed model of the noise source region, a simpler electrodynamic model, namely, that of an electric dipole of dipole moment $I(f) \cdot h$ (in A·m) may be used to describe the current source. $I(f) = C \cdot (i2\pi f V(f))$ is the injected noise current, with C denoting the capacitance of the junction, while h is the effective thickness of the junction. It is important to define induced noise voltages at the sensor using the closest ground contact as reference because, in the electrodynamic case, a unique definition of the potential difference between points at distances other than small fractions of the wavelength is impossible. Therefore in this example, the induced noise voltage is calculated as the line integral of the calculated electric field between the victim contact and a ground contact in its immediate proximity. The substrate used in this example is the same threelayer substrate (Substrate A) used earlier in this section. At the top layer of resistivity 1.25 Ω -cm, the wavelength varies from 35.3 mm at 0.1 GHz to 3.4 mm at 10 GHz. Thus, with the distance between the victim contact and the ground contact taken to be 1 µm, an induced noise voltage may be calculated with confidence.

Fig. 10 depicts the frequency dependence of the real and imaginary parts of the induced noise voltage at a distance of 100 μ m from the aggressor dipole noise source. It is noted that for this plot the frequency dependence of the dipole current is not taken into account. Rather, the dipole moment was set to a value of $1A \cdot \mu$ m. The static solver described in Section 3 predicts an

induced voltage of 47.45 nV, which is in excellent agreement with the value of 48.05 nV obtained from the electrodynamic model at 10 Hz. Furthermore, it is noted from the figure that this value remains essentially unchanged up to a frequency of 10 MHz. Beyond that frequency, the induced voltage starts exhibiting a frequency dependence that the static model is unable to predict. Finally, it is mentioned that, as expected from the frequency dependence of the equivalent surface impedance of this substrate depicted in Fig. 9, the reactive part of the induced voltage is inductive over the calculated frequency range.

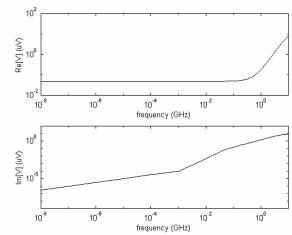


Fig. 10. Frequency dependence of the induced noise voltage across a pair of contacts 1 mm apart, placed at a distance of 100 mm from an aggressor dipole noise source in a three-layer substrate.

6. Conclusions and Future Work

In summary, this paper has presented a comprehensive methodology for the modeling of substrate noise coupling. For those cases where a quasi-static approximation is acceptable and transfer resistances may be used to quantify substrate coupling, a new and efficient method has been introduced for the calculation of the Green's function for multi-layered substrates that can accommodate arbitrary substrate doping profiles. This new methodology, combined with a systematic layout extraction procedure and the development of heuristics for reduction of semiconductor substrate complexity for those cases where large portions of the substrate must be modeled, enables a systematic and comprehensive approach to substrate noise coupling modeling under quasi-static conditions.

In addition, the need for the extension of this methodology to the frequency-dependent case, where electromagnetic effects such as displacement current and skin effect cannot be assumed negligible, has been argued and demonstrated in this paper. Toward this objective, a boundary element method is currently under development, based on a rigorous electromagnetic model for multi-layered semiconductor substrates. The preliminary study presented here from the application of such a dynamic model also argues the need for a more careful consideration of the modeling of both the various mechanisms of noise injection in the substrate and the quantification and definition of substrate-induced noise signals. These issues will be addressed in detail in a forthcoming paper.

7. Acknowledgements

H. Li is sponsored by the Motorola University Partnership in Research program. This work is partly supported by the SRC. The authors would also like to thank Mr. Jason Morsey for his contributions to the frequency-dependent Green's function calculations.

References:

- N. Verghese, T. Schmerbeck and D. Allstot, Simulation Techniques and Solutions for Mixed-Signal Coupling in Integrated Circuits, Kluwer, 1995.
- [2] T. Li, C-H Tsai, E. Rosenbaum, S-M Kang, "Substrate Resistance Modeling and Circuit-Level Simulation of Parasitic Device Coupling Effects for CMOS I/O Circuits under ESD Stress," *Electrical Overstress/Electrostatic Discharge Symposium Proceedings*, 1998.
- [3] M. Pfost, H.-M. Rein and T. Holzwarth, "Modeling substrate effects in the design of high-speed Si-bipolar IC's," *IEEE J. Solid-State Circuits*, vol. 31, no. 10, pp. 1493-1501, 1996.
- [4] J. Kanapka and J. White, "Highly accurate fast methods for extraction and sparsification of substrate coupling based on low-rank approximation," *Proc.* ICCAD 2001, San Jose, CA, Nov. 2001.
- [5] J. R. Phillips and L. M. Silveira, "Simulation approaches for strongly coupled interconnect systems," *Proc. ICCAD 2001*, San Jose, CA, Nov. 2001.
- [6] T. Smedes, N. P. van der Meijs, and A. J. van Genderen, "Boundary element methods for 3D capacitance and substrate resistance calculations in inhomogeneous media in a VLSI layout verification package," *Advances in Engineering Software*, vol. 20, no. 1, pp. 19 27, 1994.
- [7] I. L. Wemple and A. T. Yang, "Integrated circuit substrate coupling models based on Voronoi tessellation," *IEEE Trans. Computer-Aided Design*, vol. 14, no. 12, pp. 1459 – 1469, Dec. 1995.
- [8] K. Nabors, S. Kim and J. White, "Fast capacitance extraction of general three-dimensional structures," *IEEE Trans. Microwave Theory Tech.*, vol. 40, no. 7, pp. 1496-1507, July 1992.
- [9] J. R. Phillips and J. K. White, "A precorrected-FFT method for electrostatic analysis of complicated 3D structures," *IEEE Trans. On Computer-Aided Design*, pp. 1059-1072, 1997.
- [10] J. Phillips, J. Kanapka, and J. White, "Fast methods for extraction and sparsification of substrate coupling," *Proc.* 37th Design Automation Conference, pp. 738-743, 2000.
- [11] J. Zhao, S. Kapur, D. E. Long, and W. W.-M. Dai, "Efficient three-dimensional extraction based on static and full-wave layered Green's functions," *Proc.* 35th Design Automation Conference, Jun. 1998.
- [12] A.Cangellaris, "A new methodology for the direct generation of closed-form electrostatic Green's functions in layered dielectrics," Proc. Of The Applied Computational Electromagnetics Society (ACES) Symposium, Monterey, CA, March 2000.
- [13] A. C. Cangellaris and V. I. Okhmatovski, "New closed-form Green's function in shielded planar layered media," *IEEE Trans. Microwave Theory Tech.*, vol. 48, pp. 2225-2232, Dec. 2000.
- [14] V. I. Okhmatovski and A. C. Cangellaris, "A new technique for the derivation of closed-form Green's functions for unbounded planar layered media," *IEEE Trans. Antennas & Propagation*, May 2002, (in press).
- [15] L. Ladage and R. Leupers, "Resistance extraction using a routing algorithm," 30th Design Automation Conference, 1993, pp. 38-42.
- [16] Q. Li, "Layout extraction including substrate parasities for ESD protection circuits and design rule checking," Ph.D. dissertation, University of Illinois at Urbana-Champaign, Champaign, 2001.
- [17] A. M. Niknejad, et al, "Numerically stable Green function for modeling and analysis of substrate coupling in integrated circuits," IEEE Trans. Computer-Aided Design, vol 17, no. 4, pp.305-315, April 1998.
- [18] J. Katzenstein, et al, "iSREX Version 1.0 user's manual," Coordinated Science Lab, *University of Illinois*, Urbana, IL, 1999.
- [19] E. Charbon, et al, "Modeling digital substrate noise injection in mixed-signal IC's," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems*, vol. 18, no. 3, 1999, pp. 301-310.
- [20] J. R. Wait, Electromagnetic Wave Theory, Harper & Row, New York, 1985.