Minimizing Resources in a Repeating Schedule for a Split-Node Data-Flow Graph

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ABSTRACT

Many computation-intensive or recursive applications commonly found in digital signal processing and image processing applications can be represented by data-flow graphs (DFGs). In our previous work, we proposed a new technique, extended retiming, which can be combined with minimal unfolding to transform a DFG into one which is rate-optimal. The result, however, is a DFG with split nodes, a concise representation for pipelined schedules. This model and the extraction of the pipelined schedule it represents have heretofore not been explored. In this paper, we demonstrate one scheduling algorithm for such graphs, and then discuss a way to reduce the hardware requirements of the resulting schedule. In the process, we state and prove a tight upper bound on the minimum number of processors required to execute the static schedule produced by our algorithms. Finally, we demonstrate our methods on a specific example.

Categories and Subject Descriptors
J.6 [Computer-Aided Engineering]: Computer-Aided Design (CAD)

General Terms
Algorithms, Design, Performance, Theory

1. INTRODUCTION

Because the most time-critical parts of real-time or computation-intensive applications are loops, we must explore the parallelism embedded in the repetitive pattern of a loop. A loop can be modeled as a data-flow graph (DFG). The nodes of a DFG represent tasks, while edges between nodes represent data dependencies among tasks. Each edge may contain a number of delays (i.e. loop-carried dependencies). This model is widely used in many fields.

In our previous work [6–9], we proposed an efficient algorithm, extended retiming, which transforms a DFG into an equivalent graph with maximum parallelism. Indeed, we have demonstrated that extended retiming, when combined with minimum unfolding, achieves rate optimality, the first method we are aware of that this can be said about. However, the result of extended retiming is a graph containing split nodes. Indeed, it is a particular type of split-node graph which can be scheduled rate optimally. This is not to say that we are physically altering the DFG by placing registers inside of functional units. Rather, we are describing an abstraction for a graph which provides a feasible schedule with loop pipelining. While the split-node graph is the most compact means for expressing this schedule, the properties of such graphs and the means by which they can be manipulated and this pipelined schedule drawn out have not been explored in the literature. We take the first step in this exploration in this paper, exhibiting one method for scheduling the system represented by a split-node graph and optimizing it to execute on a minimal number of processors.

In [6] we demonstrated the effectiveness of our extended retiming transformation via several experiments. In all cases, we were able to achieve better results by using extended retiming, getting an optimal clock period while requiring less unfolding. The usefulness of this new transformation is clear, but interpreting the split-node graph that results from its application still presents a problem. Many scheduling algorithms for standard data-flow graphs exist throughout the literature [1, 2]. There are even many techniques for reducing such schedules so that they require a minimal number of processors [3–5]. The problem is not new but the model is. In using a split-node DFG to represent a situation, we are conveying not only that a schedule is to be pipelined, but we are giving specific clues as to how it is to be pipelined. Even after we produce a schedule which obeys the additional rules regarding pipelining that the split-node graph dictates, most of the existing scheduling methods assume unlimited available processors, an unrealistic situation. We not only demonstrate a scheduling method for our new model, we then optimize the results of our method to require minimal hardware.

In this paper, we formally define a split-node data-flow graph and redefine the terminology of scheduling to fit this new paradigm. We demonstrate a scheduling algorithm for split-node graphs, and then discuss a way to reduce the hardware requirements of the resulting schedule. In the process, we state and prove a tight upper bound on the minimum number of processors required to execute our static schedule. Finally, we demonstrate our methods on a specific example.

2. BACKGROUND

Before proceeding to our primary results, we first introduce our basic models. We then review previously established results pertinent to our task.

In our previous work [6, 8], we defined extended retiming, a graph transformation technique which minimizes the iteration period of a DFG by redistributing delays among the edges and inside of the nodes. One method for constructing the extended retiming function based on a DFG’s static schedule was proposed in [7, 9]. We begin with the schedule defined in [1], based on the DFG’s...
scheduling graph. (We will refer to this algorithm as DFG scheduling and will describe it in more detail later.) We now find the last node of the first iteration to be scheduled and cut the schedule at this point. We then read the retiming immediately by counting the occurrences of the nodes to the left of the cut.

For example, consider the DFG of Figure 1(a). Adopting a clock period of 7 and unfolding factor of 2, followed by the application of DFG scheduling, results in the schedule of Figure 1(b). C is the last node of the first iteration to be scheduled at time step 12, so we cut our diagram at this point as shown. To the left of the cut we see one complete copy of A, plus partial copies having times 1, 5 and 8. When we now retie node A, we pass one delay entirely through the node, while the remaining delays get stuck at these designated positions within A. The result is the split-node graph of Figure 1(c).

An iteration is simply an execution of all nodes in a data-flow graph (DFG) once. The average computation time of an iteration is called the iteration period of the DFG. If a DFG G contains a loop, then this iteration period is bounded from below by the iteration bound of G, which is denoted B(G) and is the maximum time-to-delay ratio of all cycles in G. For example, there are two loops in Figure 1(a): the outer A → B → C → A loop with total computation time 14 and delay count 4; and the B → C → B loop with time 4 and delay count 2. The larger of these ratios comes from the outer loop, and so B(G) = 7 in this case. In fact, the schedule of Figure 1(b) achieves this minimal iteration period, with 4 iterations being scheduled every 14 time steps. When the iteration period of the schedule equals the iteration bound of the DFG (as happens here), we say that the schedule is rate-optimal. Clearly, if we have a legal schedule for G with cycle period c and unfolding factor f, its iteration period is fΔ, and since B(G) is a lower bound for the iteration period, we must have B(G) ≤ fΔ.

We can now define a split-node data-flow graph (SDG) with splitting degree δ to be a finite, directed, weighted graph G = (V, E, d, t) where:

1. V is a vertex set;
2. E ⊆ V × V is the edge set, representing precedence relations among the nodes;
3. d : E → Z is a function with d(e) the delay count for edge e;
4. t : V → Z+ is a function with the δ-tuple t(v) representing the computation times of v’s pieces.

Broadly speaking, δ is the maximum number of pieces any node of G is split into. If a node v is not split t(v) is an integer rather than a δ-tuple. For example, in the SDG of Figure 1(c), t(A) = (1, 4, 3, 2) while t(B) = t(C) = 2. We will use the notation T(u) to refer to the sum of the elements of u’s δ-tuple if u is split and to t(u) otherwise. In this example, T(A) = 10 and T(B) = T(C) = 2.

In our model, delays may be contained either along an edge or within a node. Delays contained along an edge represent precedence relations across iterations; for example, the one-delay edge between B and C in Figure 1(c) indicates that the execution of B in the current iteration must terminate before C can begin in the next iteration. On the other hand, delays within a node convey information regarding the pipelined execution of a node. For example, the three delays inside of A tell us that up to 4 copies of the node may be executing simultaneously in a pipelined schedule of tasks. Furthermore, the position of the delays inside of a node indicate the form of the schedule of tasks for a graph. For example, one schedule for the SDG of Figure 1(c) appears in Figure 2. As we can see, the first iteration contains the beginning of A’s first copy; the next iteration includes only the part of this copy taking 4 time units to execute; the next iteration lasts only 3 time units to match the next part of the copy; and the next iteration includes the remaining piece of A’s first copy. After that, we schedule the copies of B and C as best we can around the borders of the iterations, making sure that the copy of B in this iteration precedes the copy of C in the next iteration, and that the current copy of A starts upon termination of the current copy of C.

Given an edge e = (u, v) in a SDG G, we will use the traditional notation d(e) to refer to the number of delays on the edge not including delays within end nodes. We will use d(u → v) to denote the total number of delays along an edge, including delays contained within the end nodes. We will further define d+(u → v) as d(e) plus the number of delays within the source node u, and d−(u → v) as d(e) plus the number of delays within the sink node v. Referring to Figure 1(c), we observe that d+(A → B) = d(A → B) = 3 while d−(A → B) = d(e) = 0 for e = (A, B). It is easy to see that d(u → v) = d+(u → v) + d−(u → v) − d(e) for any edge e = (u, v).

An integral time schedule or integral schedule is a function s : V × N → Z where the starting time of node v in the i-th iteration is given by s(v, i). It is a legal schedule if s(u, i) + T(u) ≤ s(v, i + d+(u → v)) for all edges e = (u, v) and iterations i, while a legal schedule is a repeating schedule for cycle period c.

Figure 1: (a) A sample DFG; (b) The DFG schedule for Figure 1(a); (c) Figure 1(a) retimed.

Figure 2: One schedule for Figure 1(c).
and unfolding factor $f$ if $s(v, i + f) = s(v, i) + c$ for all nodes $v$ and iterations $i$. Such a schedule can be represented by its first $f$ iterations, since a new occurrence of this partial schedule can be started at the beginning of every interval of $c$ clock ticks to form the complete legal schedule.

Given a DFG $G$ without split nodes, a clock period $c$ and an unfolding factor $f$, we construct the scheduling graph $G^* = (V, E, w, t)$ by reweighting each edge $e = (u, v)$ according to the formula $w(e) = d(e) - \frac{f}{c} \cdot t(u)$. We then further alter $G^*$ by adding a node $v_0$ and zero-weight directed edges from $v_0$ to every other node in $G$. We then let $sh(v)$ be the length of the shortest path from $v_0$ to $v$ in $G^*$ for every node $v$. It was demonstrated in [1] that, if $B(G) \leq \frac{f}{c}$ for a given cycle period $c$ and unfolding factor $f$, then the function $S(v, i) = \left[ \frac{f}{c}(i - sh(v)) \right]$ for all nodes $v$ and positive integers $i$ is a legal, integral, repeating schedule. In fact, this is the method used to construct the schedule in Figure 1(b).

Given a set of processors $L$, a processor assignment or assignment is a function $p : V \times N \rightarrow L$ where node $v$ in iteration $i$ is executed using processor $p(v, i)$. An assignment with unfolding factor $f$ is static (with its corresponding time schedule a static schedule) if $p(v, i + f) = p(v, i)$ for every iteration $i$. Finally, we can implement a static schedule using one of two design styles. If two copies of a node cannot be in execution simultaneously, the schedule follows a non-pipelined implementation. This creates an implicit precedence relation between consecutive copies of the same node, insuring that the first copy stops before the succeeding copy begins. If no such restriction is placed on the schedule, it is said to follow a pipelined implementation. As eluded to earlier, we will assume the use of pipelining throughout this paper.

### 3. RESOURCE MINIMIZATION

Having outlined a method by which the nodes of a SDG may be scheduled, we now explore the problem of assigning them to processors for execution. The simplest method is to statically assign dedicated processors, where a functional unit executes iterations of one and only one node from the schedule. Due to pipelining, it is necessary to assign multiple processors to a single node in order to handle overlapping iterations. We may then ask exactly how many processors are required under these rules:

**Theorem 3.1.** Let $G = (V, E, d, t)$ be a data-flow graph. Given the static repeating integral schedule $S$ from above having clock period $c$ and unfolding factor $f$, execution of all iterations of node $v$ may be completed using $\left[ \frac{f}{c} \cdot T(v) \right]$ dedicated processors for each $v \in V$.

**Proof.** Iterations $i$ and $i + k$ of node $v$ can share one processor if and only if $S(v, i) + T(v) \leq S(v, i + k)$, which by definition occurs if and only if

$$\left[ \frac{f}{c}(i - sh(v)) \right] + T(v) \leq \left[ \frac{f}{c}(i + k - sh(v)) \right].$$

Since $T(v)$ is integral, this is equivalent to

$$\left[ \frac{f}{c}(i - sh(v)) \right] + T(v) \geq \left[ \frac{f}{c}(i + k - sh(v)) \right] - \left[ \frac{f}{c}(i - sh(v)) \right] + T(v) \geq 0,$$

which happens if and only if $\frac{f}{c} - T(v) > -1$ and $k > \frac{f}{c}(T(v) - 1)$.

We now have two cases. First suppose that $\frac{f}{c}(T(v) - 1)$ is integral. Clearly $\frac{f}{c}(T(v) - 1) < \frac{f}{c} \cdot T(v) \leq \left[ \frac{f}{c} \cdot T(v) \right]$. On the other hand, $\left[ \frac{f}{c} \cdot T(v) \right] = \left[ \frac{f}{c}(T(v) - 1) + 1 \right] \leq \frac{f}{c}(T(v) - 1) + 1$ since $0 < f < c$ by assumption. Therefore $\left[ \frac{f}{c} \cdot T(v) \right]$ is the smallest integer strictly greater than $\frac{f}{c}(T(v) - 1)$ and is so the minimum number of processors required to execute all iterations of $v$. Otherwise $\frac{f}{c}(T(v) - 1)$ is not integral and we need at least $\left[ \frac{f}{c}(T(v) - 1) \right]$ processors, which is also bounded above by $\left[ \frac{f}{c} \cdot T(v) \right]$.

In any case, if $n = \left[ \frac{f}{c} \cdot T(v) \right]$, we have demonstrated above that one processor is adequate for executing $v_0$, $v_n$, $v_{2n}$, and so on; the same processor can be assigned to $v_1$, $v_{2n+1}$, $v_{2n+2}$, etc.; and one processor for $v_{2n+1}$, $v_{2n+2}$, $v_{2n+3}$, and so forth. Thus all iterations of node $v$ may be executed using only $n$ processors.

For instance, consider the example of Figure 1(c) again with clock period 7 and unfolding factor 2. By this result, we require $\left[ \frac{f}{c} \right] = 3$ dedicated processors for $A$ and $\left[ \frac{f}{c} \right] = 1$ dedicated processor for each of $B$ and $C$. In fact, our schedule for Figure 1(c) reserved 5 processors for execution, one for each “row” of the schedule. However, this may be an overestimate. For example, in the schedule of Figure 2, there is no compelling reason why some iterations of $B$ and $C$ cannot share a processor, thus possibly reducing the hardware cost needed to implement our final schedule. We are now ready to explore this question of systematically studying a given static schedule in an attempt to produce a processor assignment using undedicated processors and requiring minimal hardware.

Our processor assignment method is based on the ideas from [3], although we improve on their idea by considering rational as well as integral iteration periods and fill certain logical gaps. Given a clock period $c$, we first divide time into segments, each containing $c$ clock ticks. Segment 1 lasts from time step 0 until time step $c$, segment 1 from $c$ to $2c$, and in general segment $k$ lasts from time step $(k-1)c$ until time step $kc$. We then unfold nodes, dividing the first $f$ copies of each node in our schedule so that the pieces are small enough to fit into one segment, where $f$ is our given unfolding factor. We use an unfolding method similar to that of [4, 5], simplifying their calculations by assuming that all nodes begin execution at least once during the first segment of our schedule. In general we have two cases:

1. If a node $v$ is small enough to begin and complete execution of its zeroth iteration during the first segment of the schedule, it remains in one piece. We simply pass its starting and computation times to the next stage of our method as $\sigma(v)$ and $\tau(v)$, respectively. We also mark it as having no preceding piece (.$p(v)$ = NIL).

2. Otherwise the node overlaps segments and must be divided into parts. The first part, the head, is assigned at the end of the segment and includes the first part of the node which executes until the end of the first segment. (It thus inherits its starting time from the original node and has a computation time of the clock period minus the start time.) Next are the body sections which span entire subsequent segments. Finally, the tail is assigned at the beginning of a segment and completes execution of the original node following all body sections. In all cases, we assign $i(u)$ to identify what type of node piece $u$ is. We also assign the identity of the preceding piece to $p(u)$.

Since the pieces we are creating must refer back to their matching node from the original schedule, we use $org(u)$ and $copy(u)$ to identify the source and iteration, respectively, in the case of HEAD or whole nodes. This entire procedure appears as Algorithm 1.

As an example, consider the schedule from Figure 2. The first two iterations of both $B$ and $C$ begin and complete execution within the first 7 time steps, so are passed on to the next stage of our
Algorithm 1 Folding the vertices of a split-node graph

**Input:** A SDG \( G = (V, E, d, t) \), a schedule \( S \) for \( G \) having clock period \( c \) and unfolding factor \( f \)

**Output:** A set of folded vertices \( W \)

\( W = \emptyset \)

\( \text{for } i = 0 \text{ to } f-1 \text{ do} \)

\( m = f(v_i) \text{ for } v_i \in V \)

\( W = W \cup \{ v_i, v_{i+1}, \ldots, v_{i+m-1} \} \)

\( \text{if } m = 1 \text{ then} \)

\( \tau(v_0) = T(v) \)

\( \rho(v_0) = T(v) \text{ if } v_0 \in E \)

\( \sigma(v_0) = \emptyset \)

\( \nu(v_0) = \emptyset \)

\( \phi(v_0) = v \)

\( \text{cop}(v_0) = \text{NIL} \)

\( \text{end if} \)

\( \text{for } i = 1 \text{ to } m-2 \text{ do} \)

\( \tau(v_{i-1}) = \rho(v_i) \)

\( \rho(v_{i-1}) = \rho(v_i) \text{ if } v_{i-1} \in E \)

\( \sigma(v_{i-1}) = \emptyset \)

\( \nu(v_{i-1}) = \emptyset \)

\( \phi(v_{i-1}) = \emptyset \)

\( \text{cop}(v_{i-1}) = \emptyset \)

\( \text{end for} \)

\( \tau(v_{m-1}) = \rho(v_m) - c \cdot (m-2) \)

\( \rho(v_{m-1}) = 0 \)

\( \sigma(v_{m-1}) = v_0 \text{ if } v_{m-1} \in E \)

\( \nu(v_{m-1}) = \emptyset \)

\( \phi(v_{m-1}) = \emptyset \)

\( \text{cop}(v_{m-1}) = \emptyset \)

\( \text{end if} \)

\( \text{end for} \)

Algorithm 2 Create independent lists from folded nodes

**Input:** A set of folded nodes \( W \) and clock period \( c \)

**Output:** Independent lists of folded vertices

\( Q = \emptyset \)

\( \text{for } v \in W \text{ do} \)

\( \text{if } \nu(v) = \text{NIL} \text{ and } \text{cop}(v) = \text{NIL} \text{ then} \)

\( Q = Q \cup \{ v \} \)

\( \text{end if} \)

\( \text{end for} \)

\( \text{for } i = 1 \text{ to } f \text{ do} \)

\( w = \text{the } i\text{-th element of } Q \)

\( \text{if } \nu(w) = 0 \text{ then} \)

\( \text{if } c = 0 \text{ then} \)

\( \text{if } \phi(w) = \text{NIL} \text{ and } \nu(w) = \text{NIL} \text{ then} \)

\( \text{end if} \)

\( \text{push list } \{ w \} \text{ onto list } \{ v \} \)

\( \text{end if} \)

\( \text{end if} \)

\( \text{end for} \)

Table 1: Results from Algorithm 1 for the schedule of Figure 2.

<table>
<thead>
<tr>
<th>( v )</th>
<th>( T(v) )</th>
<th>( i )</th>
<th>( S(v,i) )</th>
<th>( m )</th>
<th>( \rho )</th>
<th>( \sigma )</th>
<th>( \nu )</th>
<th>( \phi )</th>
<th>( \text{cop} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( A )</td>
<td>10</td>
<td>0</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>A00</td>
<td>2</td>
<td>NIL</td>
<td>HEAD</td>
</tr>
<tr>
<td>( A00 )</td>
<td>0</td>
<td>5</td>
<td>A00</td>
<td>TAIL</td>
<td>NIL</td>
<td>NIL</td>
<td>NIL</td>
<td>NIL</td>
<td>NIL</td>
</tr>
<tr>
<td>( A1 )</td>
<td>5</td>
<td>3</td>
<td>A10</td>
<td>2</td>
<td>2</td>
<td>A10</td>
<td>2</td>
<td>NIL</td>
<td>HEAD</td>
</tr>
<tr>
<td>( A10 )</td>
<td>0</td>
<td>5</td>
<td>A10</td>
<td>TAIL</td>
<td>NIL</td>
<td>NIL</td>
<td>NIL</td>
<td>NIL</td>
<td>NIL</td>
</tr>
<tr>
<td>( B )</td>
<td>2</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>B00</td>
<td>2</td>
<td>NIL</td>
<td>NIL</td>
</tr>
<tr>
<td>( B00 )</td>
<td>1</td>
<td>2</td>
<td>B00</td>
<td>2</td>
<td>2</td>
<td>B00</td>
<td>2</td>
<td>NIL</td>
<td>NIL</td>
</tr>
<tr>
<td>( C )</td>
<td>2</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>C00</td>
<td>2</td>
<td>NIL</td>
<td>NIL</td>
<td>C</td>
</tr>
<tr>
<td>( C00 )</td>
<td>0</td>
<td>5</td>
<td>C00</td>
<td>TAIL</td>
<td>NIL</td>
<td>NIL</td>
<td>NIL</td>
<td>NIL</td>
<td>NIL</td>
</tr>
</tbody>
</table>

We next identify pieces that can be scheduled back-to-back on the same processor by creating independent lists of folded node pieces. We first sort our nodes, using starting time as the first key and "subscript" as the second. (In other words, if starting times are all equal, the HEAD of a node has higher priority than any of the BODY pieces, all of which have higher priority than the TAIL.) If a node drawn from this sorted list has starting time zero, a new list is created which contains only this node. In this case, we also mark its preceding piece with the number of the current list so that lists containing pieces from the same original node can be placed in proper order later. (In our algorithm, this step is accomplished by assigning a \( \psi \) value to any node which is discovered to be the \( \rho \) value of a piece we are assigning to a list.) On the other hand, if a node from the list has a non-zero starting time, we examine all of our previous lists to see if one is unoccupied at the given starting time. If such a list is found, we add the current node to it. Otherwise, we must start a new list to accommodate this node. At the end, we examine all independent lists. If the last node added to a list has a non-NIL \( \psi \) value, we set the \( su\)cc value of the list equal to this, thus identifying the list which must follow the current one when assigning lists to a processor. We also record whether the current list contains HEAD, BODY or TAIL pieces for use in the next step of our method. All of this is accomplished by Algorithm 2 below.

We resume our example with the data in Table 1, which yields a priority queue of \( A_{01}, A_{11}, A_{12}, C_{01}, B_{01}, A_{00}, C_{10}, A_{10}, B_{10} \). The first four items are assigned to list [1] through list [4], respectively, with notes made that list [1] is available past time step 5, list [3] past step 1 and list [4] past step 2. In the process, we discover three of the nodes (\( A_{01}, A_{11} \) and \( A_{12} \)) with non-NIL \( \rho \) values, so must set the appropriate \( \psi \) values. In this case, \( \psi(A_{01}) = 1 \) since \( \rho(A_{01}) = A_{00} \) and \( A_{01} \) was added to list [1], while \( \psi(A_{11}) = 2 \) and \( \psi(A_{12}) = 3 \) for similar reasons. When we pop \( B_{01} \) from the queue and discover it has starting time 1, we add it to list [3] rather than begin a new list because of our note regarding that list. We continue in this fashion, eventually arriving at the list assignments pictured in Figure 3(a). We next review the four lists and assign non-NIL \( su\)cc values to list [1], list [2] and list [4] since these lists contain the nodes with non-NIL \( \psi \) values. Finally, we note whether any list contains HEAD, BODY or TAIL nodes. These values that we have derived are summarized in Figure 3(b).
Algorithm 3 Use independent lists to assign processors

**Input:** Set of $\ell$ independent lists

**Output:** A processor assignment for iteration zero

```plaintext
Q := Ø  (* Sorted list of unproc. lists w/o body or tail *)
R := Ø  (* Sorted list of all other unproc. lists *)
```

for $i = 1$ to $\ell$
do

$p := 0$
while TRUE do

if $Q \neq Ø$ or $R \neq Ø$ then

$p := p + 1$
else

stop

end if

end while

if $Q = Ø$ then

$l :=$ first element of $Q$

else

$l :=$ first element of $R$

end if

current_nodes := Ø

while proc($l$, $Q$) = TRUE do

current_nodes := current_nodes $\cup \{l\}$

for all $v \in \text{tail}(l)$
do

if $\text{head}(v) = \text{NIL or } \text{tail}(v) = \text{HEAD then}$

$\text{unproc}(v) := p$

else

$f := f + 1$

end if

end while

if $\text{head}(l)$ = TRUE or $\text{body}(l)$ = TRUE then

$t := l$

else

$t := \text{proc}(l)$

end if

if $\text{body}(v) = \text{TRUE or } \text{proc}(v) = \text{TRUE}$ then

if $t \in Q$ then remove $t$ from $Q$ and if

else

if $t \in Q$ then remove $t$ from $Q$ end if

end if

end if

if $f = f + 1$

end if

end while

end for

```

Figure 3: Results of Algorithm 2 applied to the data from Table 1: (a) the independent lists; (b) the lists’ values.

We next take our independent lists and use them to make an initial processor assignment. We first split the lists into two groups, those which contain BODY or TAIL pieces and those that do not. If possible, we select a list without such pieces and assign it to the first available processor. If this list contains a HEAD or BODY node, we know that there is another list which must be assigned to the same processor immediately following our current list, so we find this new list and add it to the current group. Simultaneously, we increment our unfolding factor to account for pipelining. We have assumed that the zeroth iteration of all nodes begins execution during the first clock segment. Therefore, if our first contact with a node in this part of our procedure takes place during a subsequent clock segment, we know that the node represents a later iteration. This incremented unfolding factor helps us keep track of which copy of a node we are actually placing. Finally, after completing a group of lists, we increment the processor count by the unfolding factor to account for pipelining, so that the next group may be assigned to the correct new processor. This procedure appears as Algorithm 3 below.

For example, apply this method to the data from Figures 3(a) and 3(b). Our queue of lists without BODY or TAIL sections is $\{4\}$, while all other lists are in the other queue. With no other choice, we begin by assigning list[4] to the first processor. Thus the zeroth iterations of $C_0$ and $A_0$ are scheduled to execute here. The `succ` of this list is 1, so we remove this list from our other queue, increment the unfolding factor to 1, and schedule the new list’s execution on processor one during the second time segment. This list contains the HEAD of $A_1$, so we schedule the first iteration (due to the unfolding factor) of this node to execute on our processor. We proceed as before, incrementing the unfolding factor (to 2) and loading the successor to list[1], namely list[2]. Since this new list contains only the BODY of $A_1$, no values are altered. Finally, we increment the unfolding factor and process this list’s successor, list[3]. This new list contains the only copies of $B_0$, $C_1$ and $B_1$, so these nodes are scheduled for processor one during their third iteration (which correspond to nodes $B_0$, $C_7$ and $B_7$, respectively, of the original schedule). The queues are now both empty and every node in our graph has been scheduled to execute on the same processor at varying points in time. We finish by assigning all nodes an `unfold` value of 3, leaving us with the values for each node listed in Table 2.

Finally, we must propagate this initial processor assignment throughout the remaining iterations of our nodes. In Algorithm 3, we assigned a processor for a designated iteration of each node. We also recorded an unfolding factor, telling us that `unfold`(u) + 1 copies of this particular node u are in the pipeline simultaneously. It is now a simple task to assign the `unfold`(u) + 1 copies of node u to the processors we reserved for these tasks, then repeat this assignment statically to infinity, thus completing our processor assignment. This final step is summarized in Algorithm 4.

<table>
<thead>
<tr>
<th>unit</th>
<th>iter</th>
<th>unfold</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0m</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>A1m</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>B0m</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>B1m</td>
<td>1</td>
<td>3</td>
</tr>
<tr>
<td>C0m</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>C1m</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Table 2: The output applying Algorithm 3 to the data in Figures 3(a) and 3(b).
We now complete our example, using the values from Figure 2. Due to our unfolding factors, we require 4 processors to complete our schedule. We see from Table 2 that the first iteration of $A_1$ (i.e., $A_0$) is assigned to processor 1. Working backward, this means that the initial iteration of the node ($A_1$) is placed on processor 4. Also, the second iteration $A_3$ is assigned to processor 2, the third to processor 3, the fourth to processor 4, and so on. Similarly, if the third iteration of $B_0$ (really $B_4$) is assigned to the first processor, we work backward to assign the second iteration ($B_1$) to processor 4, the first iteration ($B_2$) to processor 3, and the zeroth iteration to processor 2. We do the exact same thing to assign the iterations of $B_1$ and $C_1$. Finally, the remaining nodes all have their zeroth iterations scheduled for processor 1, so it is easy to work forward and complete our processor assignment. We thus derive the final time- and processor-optimal schedule seen in Figure 4.

5. ACKNOWLEDGEMENTS

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6. REFERENCES