A Complete Phase-Locked Loop Power Consumption Model

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Abstract
A PLL power model that accurately estimates the power consumption during both lock and acquisition states is presented. The model is within 5% of circuit level simulation (SPICE) values. No significant power overhead (+/- 5% of the power consumed at the final frequency) is incurred during the acquisition process.

1. The PLL dynamic behavior

The PLL can be described as a 2nd order continuous time system. For a step of magnitude $A_{step}$ in the input frequency, the time response is given by:

$$f_s(t) = A_{step}N\left[\frac{e^{-j\omega_c t}}{N} \cos(\omega_c \sqrt{1-\xi^2} t + \sin^{-1}(\xi \omega_c))\right]$$

$$\xi = \frac{R}{2} \left[\frac{1}{N}\right] k_v I_{\text{ref}} C$$

If the frequency step takes the VCO frequency beyond the lock range, then a capture (pull-in) process takes place initially. Otherwise, only a lock process occurs, which is defined by $t_{\text{lock}}$. These times can be expressed as:

$$t_{\text{lock}} = \frac{1}{\xi \omega_c}$$

$$t_{\text{capture}} = \left| f_s(t_{\text{capture}}) - f_s(0) \right| \frac{2C}{k_v I_{\text{ref}}}$$

For the VCO gain $K_v$ (Hz/V), we need to calculate:

$$K_v = \frac{df}{dV_c} = \frac{k(V_c)}{2nV_c C_{\text{vco}}}$$

Various differential and single-ended VCOs with different values of $n$ were implemented using Berkeley’s MAGIC CAD tool in a 0.35um technology, operating with a 2.5V supply voltage. This is the validation framework for all other experiments. The average error for the estimated $K_v$ data was 2.2% and 3.2% for non-differential and differential implementations, respectively.

The resistor ($R_c$) was built as a transmission gate with both devices always on. Since $V_{ds}$ is small and assuming that $V_{gs}$ is on average close to $V_{dd}/2$, thus:

$$R_c = \frac{V_{gs}}{I_n} = \frac{2}{k(V_{ds})} \frac{L}{k_c C_{\text{vco}}(V_{dd}-2V_c)} \left[ \frac{L}{W} \right]$$

The average deviation with respect to the simulated values was 3.77% and 3.2%, for $n$ and $p$ devices respectively. The charge pump current ($I_{\text{pump}}$) and the filter capacitance ($C_f$) are described by equations already available.

2. PLL power model

For an $n$-stage differential and non-differential VCO design, the effective capacitances are:

$$C_{\text{vco-diff}} = 2n^2kC_{\text{cell}}$$

$$C_{\text{vco-nondiff}} = 2nC_{\text{cell}}$$

$$C_{\text{eff-diff}} = \frac{W_p}{k_{\text{eff}}} (C_{\text{gate}} + C_{\text{drain}})$$

$$C_{\text{eff-nondiff}} = \frac{W_n}{k_{\text{eff}}} (C_{\text{gate}} + C_{\text{drain}})$$

Where $k$ defines the voltage swing of each cell ($V_{ds}=kV_{dd}$) and $W_p$ and $W_n$ the normalized width of the $n$ and $p$ devices. For the PFD:

$$\text{C}_{\text{eff-PFD}} = \text{N}_{\text{pfd}} \times \text{G}_{\text{pfd}} \times \text{C}_{\text{tech}}$$

Where, $\text{N}_{\text{pfd}} = 146$, $\text{G}_{\text{pfd-lock}} = 0.74$ (during acquisition, $\text{G}_{\text{pfd-acq}} = 0.83$) and $\text{C}_{\text{tech}} = \text{C}_{\text{gate}} + \text{C}_{\text{drain}}$. A similar equation can be applied to the FDIV, using $\text{N}_{\text{fdiv}} = 104$ and $\text{G}_{\text{fdiv}} = 0.78$.

For the charge pump, the total energy delivered is expressed as a function of the total variation of the capacitor voltage ($\Delta V$) during the capture process. Thus:

$$P_{\text{pump}} = \frac{(\Delta V)^2 \times C_{\text{pump}}}{2} + \frac{I_{\text{pump}}^2 \times R}{4}$$

We calculate the contribution of the bias circuitry as proportional to $I_{\text{ch}}$. During lock, the total PLL power is:

$$P_{\text{PLL-lock}} = \left[ \text{N}_{\text{pfd}} \times \text{G}_{\text{pfd}} + N(2n(\theta)+\text{N}_{\text{fdiv}}) \right] C_{\text{tech}} V_{dd}^2 + I_{\text{lock}} + V_{dd}$$

The average error from the simulated results was 3.5% and 3.4% across all non-differential and differential designs. The power consumption during acquisition:

$$P_{\text{PLL-acq}} = \frac{1}{I_{\text{acq}}} \left( I_{\text{PLL-lock}} - I_{\text{lock}} + P_{\text{PLL-capture}} \right)$$

The PLL power consumption during capture is (for the PFD, $G_{\text{pfd-acq}}$ is used):

$$P_{\text{PLL-capture}} = C_{\text{FDIV}} + C_{\text{VCO}} + C_{\text{pump}} \times \left( f_{\text{capture-acq}} + P_{\text{bias}} + P_{\text{pump}} \right)$$

Where $f_{\text{capture-acq}}$ is the mean value between the start and stop frequencies during the capture process. For the lock process, a similar equation is used but a different $f_{\text{capture-lock}}$ is estimated using the definition of average value. This calculated average was within 1% of the final target frequency. The average deviation from the SPICE readings was 1.7% and 0.7% for all non-differential and differential designs.

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