Panel : Formal Verification Techniques : Industrial Status and Perspectives

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The Panel :

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Abstract :

Research in applied formal verification has become a hot topic in circuit and system design due to rising circuit complexity. Design verification presents the biggest bottleneck in digital hardware design. Major hardware bugs found in ASIC design may cause expensive project delays when they are discovered during system test on the real silicon chip. The consequences are severe, from cost overruns to lost market opportunity. Simulation and emulation tools, which are traditionally used to find bugs in a design, often cannot find the corner cases or hard−to−find bugs that may occur only after hundreds of thousands of cycles, and are well beyond the reach of conventional simulation and emulation technologies. Formal methods have emerged as an alternative approach to ensure the quality and correctness of hardware designs, overcoming some of the limitations of traditional validation techniques such as simulation and testing.

But, the use of formal methods in the industry is still quite limited, due to the difficulty of use of many formal methods available nowadays and the lack of integration between them. In order to provide insight into the scope and limitations of currently available formal verification techniques, this panel will address questions such as the following:

ASIC's have been designed for more than twenty years without formal methods. Are formal methods really necessary? How can the research community convince designers to use formal methods? Is it easy to integrate them into traditional design flow?

Not all domains seem suitable for formal methods. Is it possible to isolate those application domains that are best suited for formal methods?

Formal verification requires specially trained people who understand how to apply the mathematical techniques to verify the design. Is there a re−education requirement for the design community in order to benefit from these tools?

The panel will also examine the use of formal verification in the design of SOC's. The questions here are: can formal methods be very effective for finding errors at high levels of abstraction before a large design time is invested in implementing a flawed system architecture? are verification tools ready for System−on−Chip design verification? are they mature enough to give IP credibility and robustness?