Analog Circuit Sizing using Adaptive Worst-Case Parameter Sets

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Abstract

In this paper, a method for nominal design of analog integrated circuits is presented that includes process variations and operating ranges by worst-case parameter sets. These sets are calculated adaptively during the sizing process based on sensitivity analyses. The method leads to robust designs with high parametric yield, while being much more efficient than design centering methods.

1 Introduction

In integrated circuit technologies with ever shrinking feature sizes and growing performance requirements, the influence of process variations on the behavior and yield of analog circuits cannot be neglected. In order to be able to design robust circuits, random process fluctuations and also variations of the operating conditions (e.g. temperature and supply voltage) must be taken into account as early as possible in the design cycle. Furthermore a high degree of automation is needed for analog circuit design in order to cope with the demand of an ever shorter time-to-market [9].

Powerful tools for nominal design, e.g. [5, 14, 15], were developed and some are commercially available. Nominal design usually does not consider process fluctuations and variations of the operating conditions. Therefore, nominal design can only guarantee that the given specifications are fulfilled for the typical process and nominal operating conditions. Due to the growing influence of process fluctuation and changes in the operating conditions, design centering is necessary in addition to nominal design in order to ensure a high production yield.

Many approaches to design centering, based on statistical, e.g. [2, 11], and deterministic methods, e.g. [1, 6, 12], were presented. Usually design centering algorithms are computationally very expensive. Hence the design centering process should be started from a "good" nominal design in order to keep the computational cost small. This can be achieved by introducing *worst-case parameter sets* for process and operating conditions into nominal design [4, 6].

In the digital domain, process fluctuations are being considered by means of slow and fast worst-case parameter sets. These are calculated for a given process and typical circuit performance like delay, but independent from a specific circuit. For digital cell libraries, these parameter sets give a good estimation of the influence of random fluctuations on the relevant digital circuit performances, delay and power. However it is well known that such digital corners cases are not sufficient for analog design [6, 13].

Using digital corner cases for analog circuit design bears a high risk of leaving yield problems undetected until production. For analog design, worst-case parameter sets therefore need to be calculated for each *circuit topology* and each *circuit performance* individually.

Using such performance-specific worst-case parameter sets for circuit sizing faces the problem that they depend on the nominal design parameter set and hence vary during the sizing process.

In this paper, a new efficient sizing algorithm is presented that simultaneously considers process fluctuation and operating conditions. It features:

- calculation of individual worst-case parameter sets for each performance,
- adaptive calculation of worst-case parameter sets in each iteration step of the sizing process based on simple and fast sensitivity analyses.
- efficient trust region optimization algorithm using sizing rules [10].

The paper is structured as follows: The next section formulates worst-case parameter sets. The new sizing algorithm is discussed in Section 3, and the results are presented in Section 4.

2 Worst-case parameter sets and yield

For a given topology, a circuit can be described by its parameters and performances. Three types of parameters can be distinguished:

- *Design parameters* $\mathbf{d} \in \mathbb{R}^{n_d}$ (e.g. nominal transistor widths and lengths) can be adjusted by the circuit designer.
- Process fluctuations for instance at oxide thickness, threshold voltage, or transistor width variation, are modeled by *statistical parameters* $\mathbf{s} \in \mathbb{R}^{n_s}$ and their distribution function. As shown in [7], all practically important parameter distributions can be transformed into a

Gaussian distribution with zero mean value and covariance matrix $\mathbf{C}$: $\mathbf{s} \sim N(\mathbf{0}, \mathbf{C})$. The probability density function $pdf(\mathbf{s})$ is then given by:

$$pdf(\mathbf{s}) = (2\pi)^{-\frac{n_s}{2}} (\det \mathbf{C})^{-\frac{1}{2}} \cdot \exp\left(-\frac{\beta^2(\mathbf{s})}{2}\right) \quad (1)$$

$$\beta^2(\mathbf{s}) = \mathbf{s}^{\mathrm{T}} \mathbf{C}^{-1} \mathbf{s} \ . \quad (2)$$

In integrated circuit design, most statistical parameters appear as transistor model parameters (e.g. tox, or vth0) and cannot be adjusted by the circuit designer if a "frozen", fully qualified production process is assumed.

- *Operating parameters* $\boldsymbol{\theta} \in \mathbb{R}^{n_\theta}$ (e.g. supply voltage, temperature) describe the circuit's operating conditions. The circuit must satisfy its performance specification for a given range $\mathcal{T}_{\boldsymbol{\theta}}$ of the operating parameters, defined by their lower bounds $\boldsymbol{\theta}_{\mathrm{L}}$ and upper bounds $\boldsymbol{\theta}_{\mathrm{U}}$:

$$\mathcal{T}_{\boldsymbol{\theta}} = \{\boldsymbol{\theta} \,|\, \boldsymbol{\theta}_{\mathrm{L}} \le \boldsymbol{\theta} \le \boldsymbol{\theta}_{\mathrm{U}}\} \ . \quad (3)$$

The circuit's *performance values* $\mathbf{f}$ (e.g. gain, delay) can be calculated for a given parameter set using an analog circuit simulator: $(\mathbf{d}, \mathbf{s}, \boldsymbol{\theta}) \mapsto \mathbf{f}$. Depending on the performance, a circuit simulation means solving a system of nonlinear equations (DC- and AC-analysis) or integrating a system of nonlinear algebro-differential equations (transient analysis).

For the circuit performances, lower and/or upper specification bounds $f_{\mathrm{b},i}$, $i = 1, \ldots, n_{\mathrm{b}}$ are defined that have to be met for a correctly operating circuit:

$$\underset{i=1,\ldots,n_{\mathrm{b}}}{\forall} f_i(\mathbf{d}, \mathbf{s}, \boldsymbol{\theta}) \ge f_{\mathrm{b},i} \Leftrightarrow \mathbf{f}(\mathbf{d}, \mathbf{s}, \boldsymbol{\theta}) \ge \mathbf{f}_{\mathrm{b}} \ . \quad (4)$$

Here, upper bounds are included by $-f_i \ge f_{\mathrm{b},i}$ where $f_{\mathrm{b},i} < 0$. Considering variations in the operating conditions, the specification bounds have to be met for the whole operating range:

$$\underset{\boldsymbol{\theta} \in \mathcal{T}_{\boldsymbol{\theta}}}{\forall} \mathbf{f}(\mathbf{d}, \mathbf{s}, \boldsymbol{\theta}) \ge \mathbf{f}_{\mathrm{b}} \ . \quad (5)$$

The parametric yield Y is the percentage of circuits that satisfy (5):

$$Y(\mathbf{d}) = \int\limits_{\{\mathbf{s} \,|\, \underset{\boldsymbol{\theta} \in \mathcal{T}_{\boldsymbol{\theta}}}{\forall} \mathbf{f}(\mathbf{d}, \mathbf{s}, \boldsymbol{\theta}) \ge \mathbf{f}_{\mathrm{b}}\}} pdf(\mathbf{s}) \, d\mathbf{s} \ . \quad (6)$$

During sizing, process and operating variations can be considered by means of *worst-case parameter sets* that represent a certain standard deviation $\beta_{\max}$ of process variations [3]: For each performance specification bound $f_{\mathrm{b},i}$, a worst-case parameter deviation is determined according to

$$\begin{aligned} (\mathbf{s}_{\mathrm{wc},i}, \boldsymbol{\theta}_{\mathrm{wc},i}) &= \underset{\mathbf{s}, \boldsymbol{\theta}}{\operatorname{argmin}} \, f_i(\mathbf{d}, \mathbf{s}, \boldsymbol{\theta}) \\ \text{subject to } \beta^2(\mathbf{s}) &\le \beta_{\max}^2 \text{ and } \boldsymbol{\theta} \in \mathcal{T}_{\boldsymbol{\theta}} \ . \end{aligned} \quad (7)$$

For instance, $\beta_{\max} = 3$ corresponds to a 3σ design. Satisfying (5) at the worst-case parameter sets guarantees a minimum parametric yield

$$Y \ge Y_1^l(n_s) = F_{n_s}(\beta_{\max}^2) \ , \quad (8)$$

Performance	nominal	3σ slow/fast	3σ worst-case
Delay ↑ [ns]	1.35	1.91 (+42%)	1.92 (+42%)
Delay ↓ [ns]	1.43	1.90 (+33%)	1.90 (+33%)
Hysteresis [mV]	612	563 (–8.0%)	441 (–28%)

Table 1: Performance values for a Schmitt trigger compared at slow/fast parameter sets and at worst-case parameter sets according to Eq. (7).

where F_{n_s} is the probability function of a χ^2-distribution with n_s degrees of freedom. If $\mathbf{f}$ is monotonous with regard to $\mathbf{s}$, then another loose lower bound can be given by

$$Y \ge Y_2^l(n_f) = 1 - \Phi(-\beta_{\max}) \cdot n_{\mathrm{b}} \ , \quad (9)$$

where Φ is the probability function of the normal distribution. For example, if $\beta_{\max} = 3$ then

$$Y_2^l(n_f) \approx 100\% - 0.135\% \cdot n_{\mathrm{b}} \ . \quad (10)$$

Since Y_1^l depends on the number n_s of statistical parameters, and Y_2^l depends on the number n_{b} of bounds, either lower bound can be the greater one.

For digital circuits, it turned out that the $\mathbf{s}_{\mathrm{wc},i}$ of delay and power consumption are practically independent from sizing and topology. Therefore it is common practice to calculate a set of slow/fast worst-case parameter sets once for a manufacturing process and then use it for all digital cells. The worst-case operating points $\boldsymbol{\theta}_{\mathrm{wc},i}$ are also practically independent from sizing and topology, but $\mathcal{T}_{\boldsymbol{\theta}}$ is part of the circuit specification, not of the process. Therefore, the $\boldsymbol{\theta}_{\mathrm{wc},i}$ of delay and power are to be determined once for $\mathcal{T}_{\boldsymbol{\theta}}$.

For analog circuits, slow/fast sets are insufficient. First they do not incorporate "non-digital" performances. Tab. 1 compares the performance values of the Schmitt trigger buffer of Fig. 2 at the slow/fast corners of a $0.18\mu m$-process with the performance values at the actual worst-case parameter sets calculated directly for this topology and sizing according to Eq. (7). As can be seen, the slow/fast performance values of the delays conform to the actual worst-case performance values. In contrast to that, the 3σ worst-case value of the third performance "hysteresis" is in fact much worse than indicated by a simulation at the slow or fast parameter set. Using these parameter sets to verify a specification regarding hysteresis will therefore pretend an unrealistically high robustness.

Secondly, worst-case parameter sets depend on the analog circuit's topology. Assume for instance a process consisting of only two random variables, s_{n} that influences solely NMOS transistors and s_{p} for the PMOS transistors. Further given are a current mirror completely built of NMOS transistors and another one completely built of PMOS transistors. It is then obvious, that the first circuit is only affected by s_{n}, whereas the second one is affected only by s_{p}. Hence the 3σ worst-case parameter sets will be orthogonal.

Third, worst-case parameter sets depend on sizing, see Sec. 4.

3 Sizing and adaption of worst-case parameter sets

Worst-case sizing is the task of finding a design parameter vector $\mathbf{d}$ that guarantees a minimum yield according to Eqs. (8, 9). Since the worst-case parameter sets depend on the sizing in a non-linear manner, we propose an iterative numerical optimization. Since the exact calculation of the worst-case parameter sets $(\mathbf{s}_{\mathrm{wc},i}, \boldsymbol{\theta}_{\mathrm{wc},i})$ is computationally expensive, we introduce an approach to relaxed calculation of worst-case parameter sets based on linear approximations. An update of the approximated worst-case parameter sets is performed at each iteration step.

Beginning with $\mu = 0$, the following actions are performed in each iteration step (μ) of the algorithm, The steps 1 through 6 are performed for each specification $f_{\mathrm{b},i}$ (see Fig. 1).

1. the corresponding performance f_i is linearized with respect to the operating parameters $\boldsymbol{\theta}$ at its respective worst-case parameter set $(\bar{\mathbf{s}}_{\mathrm{wc},i}^{(\mu-1)}, \bar{\boldsymbol{\theta}}_{\mathrm{wc},i}^{(\mu-1)})$ and design parameter set $\mathbf{d}^{(\mu-1)}$ of the previous step :

$$\mathbf{g}_i^{(\mu)} = \nabla_{\boldsymbol{\theta}} f_i \Big|_{\mathbf{d}^{(\mu-1)}, \bar{\mathbf{s}}_{\mathrm{wc},i}^{(\mu-1)}, \bar{\boldsymbol{\theta}}_{\mathrm{wc},i}^{(\mu-1)}} . \tag{11}$$

2. Then, the components j of the worst-case operating parameter set $\bar{\boldsymbol{\theta}}_{\mathrm{wc},i}^{(\mu)}$ are calculated:

$$\left(\bar{\boldsymbol{\theta}}_{\mathrm{wc},i}^{(\mu)}\right)_j = \begin{cases} (\boldsymbol{\theta}_L)_j & \text{if } \left(\mathbf{g}_i^{(\mu)}\right)_j \geq 0 \\ (\boldsymbol{\theta}_U)_j & \text{else} \end{cases} . \tag{12}$$

3. Performance f_i is linearized with respect to the statistical parameters $\mathbf{s}$ at the worst-case parameter set from the previous iteration step $(\bar{\mathbf{s}}_{\mathrm{wc},i}^{(\mu-1)})$ and at the worst-case operating parameter set of the current iteration step $(\bar{\boldsymbol{\theta}}_{\mathrm{wc},i}^{(\mu)})$:

$$\mathbf{h}_i^{(\mu)} = \nabla_{\mathbf{s}} f_i \Big|_{\mathbf{d}^{(\mu-1)}, \bar{\mathbf{s}}_{\mathrm{wc},i}^{(\mu-1)}, \bar{\boldsymbol{\theta}}_{\mathrm{wc},i}^{(\mu)}} . \tag{13}$$

4. Thereafter, $\bar{\mathbf{s}}_{\mathrm{wc},i}^{(\mu)}$ is defined by

$$\bar{\mathbf{s}}_{\mathrm{wc},i}^{(\mu)} = -\frac{\beta_{\max}^2}{\sqrt{{\mathbf{h}_i^{(\mu)}}^{\mathrm{T}} \cdot \mathbf{C} \cdot \mathbf{h}_i^{(\mu)}}} \cdot \mathbf{C} \cdot \mathbf{h}_i^{(\mu)} . \tag{14}$$

5. Performance f_i is then linearized with respect to design parameters $\mathbf{d}$ at the worst-case parameter set of the current iteration step $(\bar{\mathbf{s}}_{\mathrm{wc},i}^{(\mu)}, \bar{\boldsymbol{\theta}}_{\mathrm{wc},i}^{(\mu)})$[1]:

$$\mathbf{k}_i^{(\mu)} = \nabla_{\mathbf{d}} f_i \Big|_{\mathbf{d}^{(\mu-1)}, \bar{\mathbf{s}}_{\mathrm{wc},i}^{(\mu)}, \bar{\boldsymbol{\theta}}_{\mathrm{wc},i}^{(\mu)}} \tag{15}$$

[1] Please note that each iteration step is divided into 3 update steps according to the 3 parameter types. First, the worst-case operating parameter set is updated: $\bar{\boldsymbol{\theta}}_{\mathrm{wc}}^{(\mu-1)} \rightsquigarrow \bar{\boldsymbol{\theta}}_{\mathrm{wc}}^{(\mu)}$. Thereafter this updated worst-case operating parameter set $\bar{\boldsymbol{\theta}}_{\mathrm{wc}}^{(\mu)}$ is already used for the sensitivity calculation that leads to an updated worst-case parameter set $\bar{\mathbf{s}}_{\mathrm{wc}}^{(\mu-1)} \rightsquigarrow \bar{\mathbf{s}}_{\mathrm{wc}}^{(\mu)}$. The updated worst-case parameter set is then used for the sensitivity calculation leading to an updated design parameter set $\mathbf{d}^{(\mu-1)} \rightsquigarrow \mathbf{d}^{(\mu)}$. Using the latest available parameter sets for each update step contributes to the efficiency of the algorithm.

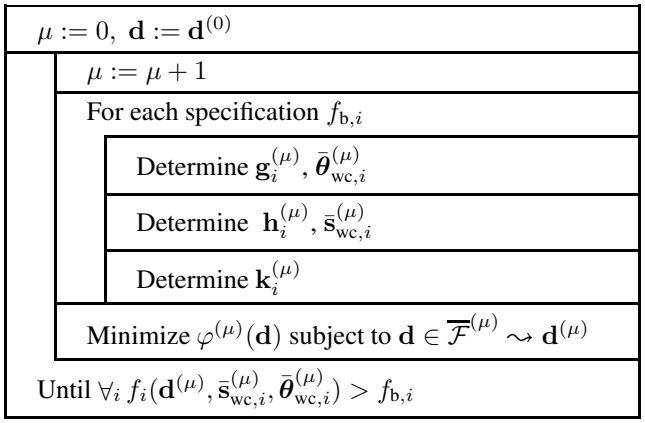

Figure 1: Structure of optimization algorithm.

$$\begin{aligned} \bar{f}_{\mathrm{wc},i}^{(\mu)}(\mathbf{d}) &= f_i(\mathbf{d}^{(\mu-1)}, \bar{\mathbf{s}}_{\mathrm{wc},i}^{(\mu)}, \bar{\boldsymbol{\theta}}_{\mathrm{wc},i}^{(\mu)}) \\ &\quad + {\mathbf{k}_i^{(\mu)}}^{\mathrm{T}} \cdot (\mathbf{d} - \mathbf{d}^{(\mu)}) . \end{aligned} \tag{16}$$

6. The parameter distance function $\alpha_i^{(\mu)}(\mathbf{d})$ [15] is then defined as

$$\alpha_i^{(\mu)}(\mathbf{d}) = \frac{\bar{f}_{\mathrm{wc},i}^{(\mu)}(\mathbf{d}) - f_{\mathrm{b},i}}{\left\|\mathbf{k}_i^{(\mu)}\right\|} . \tag{17}$$

The objective function $\varphi^{(\mu)}(\mathbf{d})$ is calculated based on the parameter distances $\alpha_i^{(\mu)}$ for the specifications $f_{\mathrm{b},i}$, $i = 1, \ldots, n_{\mathrm{b}}$:

$$\varphi^{(\mu)}(\mathbf{d}) = \sum_{i=1}^{n_{\mathrm{b}}} \exp\left(-a \cdot \alpha_i^{(\mu)}(\mathbf{d})\right), \quad a > 0 . \tag{18}$$

The positive constant factor a is a weighting factor. High values of a make the optimizer focus stronger on violated specifications.

7. The objective function $\varphi^{(\mu)}(\mathbf{d})$ is then minimized by means of a trust region method presented in [15]:

$$\mathbf{d}^{(\mu)} = \underset{\mathbf{d}}{\operatorname{argmin}}\, \varphi^{(\mu)}(\mathbf{d}) \quad \text{subject to } \mathbf{d} \in \overline{\mathcal{F}}^{(\mu)}, \tag{19}$$

where $\mathcal{F}$ is the *feasibility region* that guarantees the basic functionality and robustness of a circuit [10]. The constraint $\mathbf{d} \in \mathcal{F}$ ensures that functional constraints like "all transistors must be in saturation" are fulfilled during the sizing.

The feasibility region $\mathcal{F}$ is the subset of the design space where all functional constraints are fulfilled. Considering $\mathcal{F}$ is crucial for automated sizing of circuits:

- The result of the sizing has to be feasible in order to represent a technically correct circuit. Only parameter vectors $\mathbf{d} \in \mathcal{F}$ are technically valid solutions.
- Most performances are only weakly nonlinear in the feasibility region. Therefore, the reduction of the design space to the feasibility region significantly improves the precision of the used linearized performance models.

	Performance	Hysteresis [V]	Delay↑ [ns]	Delay↓ [ns]
	Spec. $f_{\mathrm{b},i}$	> 0.50	< 1.75	< 1.75
Initial	$f_i(\mathbf{d}^{(\mathrm{Initial})}, \mathbf{s}_{\mathrm{wc},i}^{(\mathrm{Initial})})$	0.44↯	1.92↯	1.90↯
	Y_i	2.0%	55.0%	73.5%
	Y_{tot}	2.0%		
Final	$f_i(\mathbf{d}^{(\mathrm{Final})}, \mathbf{s}_{\mathrm{wc},i}^{(\mathrm{Final})})$	0.51	1.75	1.74
	$f_i(\mathbf{d}^{(\mathrm{Final})}, \mathbf{s}_{\mathrm{wc},i}^{(\mathrm{Initial})})$	0.51	1.75	1.74
	Y_i	100.0%	99.5%	100.0%
	Y_{tot}	99.5%		

Table 2: Results for Schmitt trigger, with partial yields Y_i and total yield Y_{tot}.

- The constraints reduce the exploration space for the optimization algorithm and therefore improve the convergence of the algorithm.

During the optimization, a linear approximation $\overline{\mathcal{F}}^{(\mu)}$ is used and is updated in each iteration step.

4 Results

The proposed method was applied to two example circuits using statistical data of an industrial fabrication process. The first circuit, a Schmitt trigger (Fig. 2), is a typical digital circuit from a cell library.

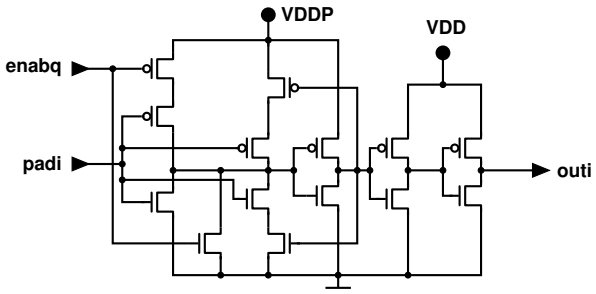

Figure 2: Schematic of a Schmitt trigger.

The yield values listed in this section were all obtained from a 200 sample Monte-Carlo analysis, with consideration of operational parameters according to Eq. (6). Please note, that this Monte-Carlo analysis is not part of the algorithm itself, but only to illustrate the yield improvement obtained with this approach. The results of the optimization are compiled in Table 2. As can be seen, the initial total yield Y_{tot} was insufficient 2.0% for this circuit, mainly due to the low partial yield Y_i of the hysteresis. The row $f_i(\mathbf{d}^{(\mathrm{Initial})}, \mathbf{s}_{\mathrm{wc},i}^{(\mathrm{Initial})})$ unveils that all specifications were violated at their appropriate 3σ worst-case parameter set before the optimization. After only 5 iterations of the worst-case sizing algorithm all specifications could be met at their final worst-case parameter sets $(\mathbf{d}^{(\mathrm{Final})}, \mathbf{s}_{\mathrm{wc},i}^{(\mathrm{Final})})$. This improvement led to a total yield of 99.5%.

In Table 2, the performance values for the final design parameter set $\mathbf{d}^{(\mathrm{Final})}$ have been simulated for both, the initial worst-case parameter sets $\mathbf{s}_{\mathrm{wc},i}^{(\mathrm{Initial})}$ and the final worst-case parameter sets $\mathbf{s}_{\mathrm{wc},i}^{(\mathrm{Final})}$. Obviously, both worst-case parameter sets lead to identical performance values.

Performance	Hysteresis	Delay↑	Delay↓
$\angle(\mathbf{s}_{\mathrm{wc},i}^{(\mathrm{Initial})}, \mathbf{s}_{\mathrm{wc},i}^{(\mathrm{Final})})$	12.4°	5.4°	4.3°

Table 3: Angles between initial and final worst-case parameter sets of the same performance of the Schmitt trigger.

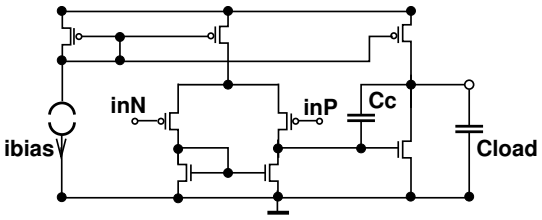

Figure 3: Schematic of a Miller operational amplifier.

In Table 3, the angles between the initial and final worst-case parameter sets are given for each performance. Apparently, the initial and final worst-case parameter sets are very similar for the hysteresis and nearly identical for the two delays.

In Table 4, angles of initial and final worst-case parameter sets are compared between the different performances. The differences between initial and final angles are around 10° comparing the hysteresis with the delays and almost 0° between rising and falling delay.

	Hysteresis	Delay↑	Delay↓
Hysteresis	—	66.4°	60.0°
Delay↑	74.4°	—	10.6°
Delay↓	76.1°	10.5°	—

Table 4: Angles between the worst-case parameter sets of different performances of the Schmitt trigger before the optimization (unshaded upper right triangle) and after the optimization (light gray shaded lower left triangle).

These experiments illustrate, that for digital circuits, worst-case parameter sets are rather independent from the sizing.

The second example, a Miller operational amplifier (Fig. 3), is a typical analog circuit. For the initial sizing all specifications but the one for the power consumption were violated at their 3σ worst-case parameter sets (row $f_i(\mathbf{d}^{(\mathrm{Initial})}, \mathbf{s}_{\mathrm{wc},i}^{(\mathrm{Initial})})$ of Table 5), leading to a total yield of 0.0%. Again after 5 iterations of the sizing algorithm, all specifications could be fulfilled at their worst-case points $(\mathbf{d}^{(\mathrm{Final})}, \mathbf{s}_{\mathrm{wc},i}^{(\mathrm{Final})})$.

Unlike the Schmitt trigger, the worst-case parameter sets of the Miller operational amplifier change significantly with the sizing. Conducting the same experiment as with the Schmitt trigger of transfering the initial worst-case parameter sets $\mathbf{s}_{\mathrm{wc},i}^{(\mathrm{Initial})}$ to the final sizings $\mathbf{d}^{(\mathrm{Final})}$ again, this time leads to considerably different performance values compared to the values at the actual final worst-case parameter sets $(\mathbf{d}^{(\mathrm{Final})}, \mathbf{s}_{\mathrm{wc},i}^{(\mathrm{Final})})$. The same holds for the positions of the initial and final worst-case parameter sets (Table 6 and 7).

Given these variabilities and the spread of the worst-case parameter sets over the space of the statistical parameters (Table 7), it becomes apparent that the worst-case conditions for analog circuits cannot be represented only by pre-

	Performance	A_0 [dB]	f_t [MHz]	Φ_m [°]	SR_p [V/μs]	Power [mW]
	Spec. $f_{b,i}$	> 80	> 1.3	> 60	> 3	< 1.3
Initial	$f_i(\mathbf{d}^{(\text{Initial})}, \mathbf{s}_{wc,i}^{(\text{Initial})})$	64.8↯	0.7↯	9.6↯	0.2↯	0.2
	Y_i	95.5%	0.0%	0.0%	0.0%	100.0%
	Y_{tot}	0.0%				
Final	$f_i(\mathbf{d}^{(\text{Final})}, \mathbf{s}_{wc,i}^{(\text{Final})})$	80.1	2.5	64.2	3.2	1.2
	$f_i(\mathbf{d}^{(\text{Final})}, \mathbf{s}_{wc,i}^{(\text{Initial})})$	85.6	2.5	66.8	4.5	1.1
	Y_i	100.0%	100.0%	100.0%	100.0%	100.0%
	Y_{tot}	100.0%				

Table 5: Results for Miller operational amplifier, with partial yields Y_i and total yield Y_{tot}.

Performance	A_0	f_t	Φ_m	SR_p	Power
$\angle(\mathbf{s}_{wc,i}^{(\text{Initial})}, \mathbf{s}_{wc,i}^{(\text{Final})})$	30.6°	13.0°	93.9°	165.5°	68.2°

Table 6: Angles between initial and final worst-case parameter sets of the same performance of the Miller operational amplifier.

defined digital slow/fast worst-case parameter sets. In consequence one worst-case parameter set has to be determined for each specification at every sizing individually.

Table 8 compiles the computational costs for the sizing of both circuits. The results were obtained on a network of 5 computers (Sun Ultra I for the Schmitt trigger and 500 MHz Pentium III for the Miller operational amplifier), using the Infineon in-house simulator TITAN [8]. One can see that the whole synthesis process takes 385 and 685 simulations respectively (1 simulation includes DC, AC and transient simulation), equivalent to 20 minutes and 5 minutes elapsed time (exclusive computer usage). Hence a complete sizing can be done at the cost of a Monte Carlo analysis.

Conclusion

A method for analog circuit sizing has been presented that performs nominal design at worst-case parameter sets for operating conditions and for manufacturing variations. It has been illustrated that these worst-case parameter sets are dependent on the circuit topology, on the circuit performances and of the design parameter values. The presented method features a relaxed calculation of worst-case parameter sets based on performance linearizations. In this way, sizing of robust analog circuits can be achieved at lower simulation costs than by design centering approaches.

	A_0	f_t	Φ_m	SR_p	Power
A_0	—	13.6°	130.0°	91.1°	164.5°
f_t	28.0°	—	117.2°	79.1°	162.4°
Φ_m	141.1°	125.1°	—	41.5°	54.2°
SR_p	105.1°	79.5°	61.9°	—	88.1°
Power	81.1°	106.2°	112.1°	172.9°	—

Table 7: Angles between the worst-case parameter sets of different performances of the Miller operational amplifier before the optimization (unshaded upper right triangle) and after the optimization (light gray shaded lower left triangle).

Circuit	# Simulations	Wall clock time
Schmitt trigger	385	20 min (5 Sun Ultra I)
Miller	685	5 min (5 Pentium III 500 MHz)

Table 8: Computational costs

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