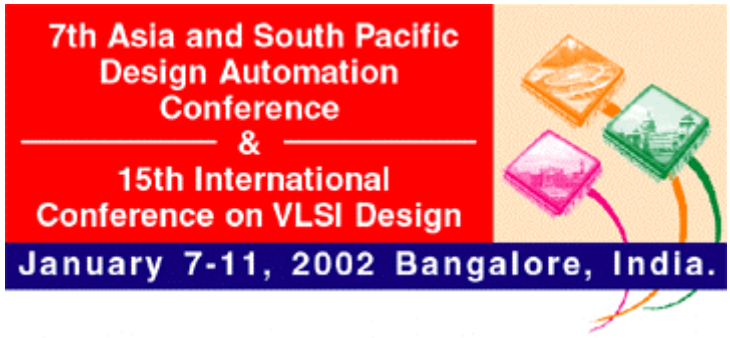

ASP-DAC/VLSI Design 2002

7th Asia and South Pacific Design Automation Conference and 15th International Conference on VLSI Design

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7–11 January 2002

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A landmark of Bangalore, Vidhana Soudha, is an imposing building which houses the Secretariat, the State Legislature, and several other government offices of the State of Karnataka in India. Built in a Neo-Dravidian style of architecture, it is one of India's most magnificent post-independence buildings. The massive four-story structure, with towering columns, ornamental frescoes and carvings, has a total plinth area of over 500,000 square-feet. The Cabinet Room has a spectacular carved door made of pure sandalwood.

The papers in this Proceedings reflect the authors' opinions and are published as presented and without change. Their inclusion in this book does not necessarily constitute endorsement by the ASPDAC/VLSI Design Conference Committee.

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Message from the General Chair

Sunil D. Sherlekar

Welcome to the joint event—The Fifteenth International Conference on VLSI Design and the Seventh Asia and South Pacific Design Automation Conference (ASPDAC). Both these conferences have individually matured into prestigious meetings that VLSI professionals look forward to attending year after year. For the first time, these meetings are being held jointly in order to bring together a larger cross-section of VLSI Design and EDA professionals. We have a five-day program packed with many exciting events ahead of us. I invite you to take full advantage of this unique opportunity to meet people, learn and explore business opportunities.

Allow me to offer you a quick overview of this joint conference. The first two days will feature eight high-quality tutorials that cover all aspects of VLSI. In the next three days, we have keynote speeches, technical paper presentations, embedded tutorials and panel discussions. It is our privilege to have four distinguished keynote speakers this year: Dr. Biswadip (Bobby) Mitra of Texas Instruments from India, Dr. Kazuo Yano of Hitachi from Japan, Dr. Martin Schuurmans of Philips from The Netherlands and Dr. Aart de Geus of Synopsys from U.S.A. The technical program of the conference will feature five embedded tutorials and 109 technical paper presentations. In addition, a special session on "Hot Chips from India" is being organized.

To share the practical experience of chip design, a design contest was organized with the conference, with prizes being awarded to the most innovative designs. This year, 24 designs were submitted for the design contest.

The conference is accompanied by an exhibition featuring a large number of leading VLSI companies from all over the world demonstrating their latest products.

It is my pleasure to acknowledge the effort of the joint conference committee in putting this event together. I thank the Program Co-chairs, Srimat Chakradhar, Takashi Nanya and C.P. Ravikumar, for their excellent work in compiling a high-quality technical program. The technical program is a true reflection of the state-of-the-art in VLSI Design and Electronic Design Automation. My thanks are due to the Tutorials Chair, Rubin Parekhji, for putting together an excellent program of eight full-day tutorials. I would like to thank the Design Contest Co-chairs, Soumitra Nandy and Kazutoshi Kobayashi for the successful design contest. Thanks are due to Srimat Chakradhar for playing the additional role of Publications Chair. He has also maintained the conference website and worked closely with the staff of the IEEE Computer Society Press and ACM SIGDA to bring out the proceedings. The proceedings of this joint conference are

published by the IEEE CS Press in paper form and by ACM SIGDA on CD-ROM. I thank Anne Jacobs of IEEE and Kathy Preas of ACM SIGDA for their cooperation and support.

Obviously, no conference can be organized without money and the support of various companies and organizations goes a long way to minimize the burden of registration fees on the delegates. I am grateful to M. Chandrasekaran, our Exhibits & Sponsorship Chair, for putting together an impressive exhibition and obtaining sponsorship support.

Infrastructure: when good, it is invisible! I thank the Organizing Committee Chair, R. Shankar and his team for making excellent arrangements and ensuring smooth execution of the event. In this task, he was ably assisted by Kenneth Menzies, John Jacob and their team from Adverto and our Audio-Visual Chair, T.V. Varadarajan.

The Publicity Co-chairs, Anand Sudarshan and Samir Kumar have done a creditable job of publicizing the event. I thank Ashok Murugavel for coordinating the foreign registration.

Every event needs someone to take care of last-minute problems and servicing requests from individual delegates. This job was handled remarkably well by our dedicated team of volunteers; my heartfelt thanks to them.

VLSI Design/ASPDAC 2002 is sponsored by the VLSI Society of India, the Ministry of Information Technology (Government of India), the IEEE Circuits & Systems Society and ACM SIGDA. Nikil Dutt, Ellen Yoffa, and A. Prabhakar have played key roles as Liaisons for ACM, IEEE and VLSI Society of India, respectively. The help and encouragement received from G.H. Sarma, Secretary, VLSI Society of India is gratefully acknowledged.

The fellowships program has allowed a number of faculty and students from Indian academic institutions to participate in the conference. In addition, the travel grants from IEEE CAS have permitted a number of researchers from foreign countries to participate in the meeting. I thank the Fellowship Co-chairs, K.S. Gurumurthy and Navakant Bhat for handling the fellowships and the IEEE CAS travel grants.

The ASPDAC Steering Committee Chair, Tatsuo Ohtsuki, and the VLSI Design Conference Steering Committee Chair, Vishwani Agrawal, have offered invaluable help, guidance, moral support and inspiration at all stages.

Finally, I would like to thank the authors who submitted their work to the conference, the tutorial speakers, members of the technical program committee, paper reviewers, members of the local organization committee, exhibitors, panelists and delegates who have all played their important roles in making this event a success.

On behalf of the conference committee, I once again extend you a warm welcome to VLSI Design/ASPDAC 2002. I hope you will benefit from the technical sessions, the exhibits and the informal interactions. I also hope that you will enjoy your stay in Bangalore—variously described as the garden city of India, the air-conditioned city of India and the Silicon Valley of India—and visit places in and around Bangalore of interest to lovers of nature, history, art, architecture and technology.

Sunil D. Sherlekar

Message from the Program Chairs



Srimat Chakradhar **Takashi Nanya** **C.P. Ravikumar**

On behalf of the organizing committee of **VLSI Design-ASPDAC 2002**, it is our pleasure to welcome you to this mega-event. For the first time, the International Conference on VLSI Design is being held jointly with the Asia South Pacific Design Automation Conference. Today, the VLSI Design conference celebrates its 15th birthday while ASPDAC celebrates its 7th birthday. It has been our unique privilege to be associated with this event in the capacity of technical program co-chairs.

Preparations towards the conference technical program started almost a year ago. Continuing the tradition set up last year, we used an Internet-based submission and review process. Each paper was assigned 5 to 8 reviewers in relevant areas. Each paper was also assigned a review manager, who was a member of the technical program committee. We obtained 1123 reviews from 384 reviewers -- about 5 reviews per paper on an average. The program committees met separately in India, USA, and Japan, and converged on a final program.

The final program of the joint conference represents a slice of cutting-edge R&D in VLSI. It includes 4 Keynote addresses, 8 full-day tutorials, 113 technical paper presentations, and 1 panel discussion. We are proud to have Aart De Geus (Synopsys, USA), Bobby Mitra (TI India), Kazuo Yano (Hitachi, Japan), and Martin Schuurmans (Philips, Netherlands) as our distinguished Keynote speakers. We received 22 excellent tutorial proposals, of which we were able to accommodate 8 full-day tutorials. We received a record submission of 269 high-quality technical papers from over 10 different countries this year: India (95), USA (74), China (29), Japan (24), Germany (12), Korea (8), Taiwan (6), The Netherlands (4), Singapore (3), Belgium (3), France (2), Sweden (2), Hong Kong (2), Australia (2), Ireland (1), Italy (1), and Russia (1). Due to space and time limitations, we were only able to include 113 of these submissions in the final program. These papers are organized into

- 4 sessions each on Low Power Design, Synthesis, Testing, Layout, and Interconnects & Technology
- 2 sessions on Embedded Systems, Verification, and VLSI Architecture
- 1 session on Analog Design, and
- 1 special session on "Hot Chips from India"

We hope you will enjoy this technical program as much as we have enjoyed putting it together. We thank all the authors who submitted their work to the conference. We thank all the reviewers

for their timely reviews. The final program is a reflection of the combined opinion of members of the program committee and independent peer reviews. Special thanks to the program committee for a job well done. We thank Rubin Parekhji who put together an excellent Tutorial program, and all the tutorial speakers for their contribution. We thank S. Karthik for organizing the special session. We express our sincere gratitude to the staff at Texas Instruments, India, and Prof. Mike Bushnell and his team at Rutgers University for their invaluable help in hosting the PC meetings. This year, we were fortunate to tap into the expertise of Vishwani Agrawal, Sunil Sherlekar, and Mahesh Mehendale who willingly offered quality help at all times.

We extend you a warm welcome, and invite you to enjoy the proceedings of VLSI Design-ASPDAC 2002.

Srimat Chakradhar

Takashi Nanya

C.P. Ravikumar

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VLSI Design 2001 Conference Awards

Arun Kumar Choudhury Best Paper Award

Estimating Crosstalk from VLSI Layouts

C.P. Ravikumar and V. Shankar Subramanian

Best Student Paper Award

Combinational Test Generation for Acyclic Sequential Circuits Using a Balanced ATPG Model

Yong Chang Kim, Vishwani D. Agrawal, and Kewal K. Saluja

Honorary Mention Award

Observability Register Architecture for Efficient Production Test and Debug of VLSI Circuits

Dilip Bhavsar and Rishan Tan

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Conference History

Meeting Sequence	Place	Dates	Number of Papers	Number of Posters	Number of Tutorials	Proceeding Pages
First	Madras, India	Dec. 26-28, 1985	29	0	1	193
Second	Bangalore, India	Dec. 15-18, 1988	26	21	4	496
Third	Bangalore, India	Jan. 6-9, 1990	30	22	4	390
Fourth	New Delhi, India	Jan. 4-8, 1991	45	16	9	315
Fifth	Bangalore, India	Jan. 4-7, 1992	57	24	4	378
Sixth	Bombay, India	Jan. 3-6, 1993	70	9	6	371
Seventh	Calcutta, India	Jan. 5-8, 1994	87	0	6	448
Eighth	New Delhi, India	Jan. 4-7, 1995	77	6	6	456
Ninth	Bangalore, India	Jan. 3-6, 1996	75	16	6	480
Tenth	Hyderabad, India	Jan. 4-7, 1997	84	18	6	608
Eleventh	Chennai, India	Jan. 4-7, 1998	98	0	6	624
Twelfth	Goa, India	Jan. 7-10, 1999	103	0	6	682
Thirteenth	Calcutta, India	Jan. 3-7, 2000	93	0	6	590
Fourteenth	Bangalore, India	Jan. 3-7, 2001	77	0	9	592
Fifteenth	Bangalore, India	Jan. 7-11, 2002	109	0	8	834

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