Impact of RET on Physical Layouts

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ABSTRACT
In this paper, we briefly describe the lithography developments known as RET (Resolution Enhancement Technologies), which include off-axis illumination in litho tools, Optical and Process Correction (OPC), and phase shifting masks (PSM). All of these techniques are adopted to allow ever smaller features to be reliably manufactured, and are being generally adopted in all manufacturing below 0.25 microns. However, their adoption also places certain restrictions on layouts. We explore these restrictions, and then provide suggestions for layout practices that will facilitate the use of these technologies, especially the generation of a clean "target" layout for use as input layers for photomask preparation, and the use of verification tools that use process simulation.

General Terms
Verification, Design, Standardization, Performance.

Keywords
Lithography, RET, OPC, PSM, phase-shifting, Off-axis illumination, DFM, physical verification, simulation.

1. INTRODUCTION
As the economics of Moore's Law continue to drive ICs to ever higher performance with circuit features with ever smaller sizes [1], optical lithography has been pushed far beyond the range previously thought possible. Excimer lasers with a wavelength of 248 nm are routinely used to fabricate devices at dimensions of 180 nm, and recent developments in 157 nm F_2 excimer sources suggest that optical lithography may be used until the 70 nm generation [2].

This extension of optical lithography has been enabled by several developments, including improvements in chemically amplified photoresists and the routine adoption of anti-reflective coatings. For decades, it has been known that physical phenomena of the optical systems used for lithography (especially diffraction and phase interference) can be well understood and predicted. By predicting these effects and compensating for them, dramatically improved image contrast and pattern fidelity can be achieved, and the minimum feature and pitch that can be resolved are significantly extended. The general name for this field is Resolution Enhancement Technologies (RET) [3].

The adoption of different RET approaches, however, dictates certain tradeoffs with various aspects of the layout. Currently, communication between designers and process development exists as an arm's-length handoff, with little communication between the two communities. The usual medium of exchange between these two communities is a set of design rules. Since the adoption of RET can significantly alter the design rules, this makes the progress required to continue along the Moore's Law development trajectory far more cumbersome and difficult.

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2. RET

2.1 Three approaches to RET
An optical wave for lithography, like all waves in physics, has three major components. These are direction, amplitude, and phase. The various RET techniques have evolved around these three orthogonal "handles" for a wave.

The first category of Direction includes the various Off Axis Illumination (OAI) techniques developed in the past ten years [3,4,5]. These use a shaped illuminator to direct light only at certain angles onto the photomask. The combination of the angle and the pitch of features in the mask can enhance certain spatial frequencies in the image, and leads to resolution enhancement. Various Off-axis designs have been commercialized in recent years, including annular illumination techniques, various quadrupole techniques, and more recently dipole illumination [6].

The second category of Amplitude concerns techniques known as OPC (Optical & Process Correction). These techniques alter the layout data for the photomask to make certain portions of features larger or smaller, in accord with how much additional exposure (or lack of exposure) is desired at certain points on the wafer [7,8,9]. When these adjustments are appropriately calibrated, overall pattern fidelity is greatly improved, reducing linewidth variation. Various phenomena can be corrected in this way, such as corner rounding and isolated–dense line bias [9]. This technique in one form or another has now become standard in IC production at 0.25 micron and below.

The third category is Phase, which is controlled by phase-shifting masks (PSM). In this case, certain portions of the photomask are etched to create phase shifts between different regions of the mask. The relative difference in phase between regions enhances certain interference effects in the image, and increases contrast. Many varieties of phase masks have been developed in the past 20 years [3,4,10,11]. The improved contrast from the interference effects

allow features to be printed more densely than would otherwise be possible, typically allowing pitch to decrease by a factor of 2 [10].

2.2 Points of insertion

Each of these techniques must be inserted in the sequence of steps involved with the manufacture of circuits or the production of layouts in order to enhance the production of a working chip.

For all varieties of off-axis illumination, it is clear that the new illuminator is a physical modification to the lithography tool, and the proper point of insertion is in the tool itself, affecting how light impinges on the photomask.

For OPC techniques, insertion at physical layout verification, prior to tape-out, has become the standard insertion point [12]. By adding the OPC alterations as a correction loop to "repair" a layout that fails a manufacturability check, OPC is applied only when needed, and in the degree needed. This has also been facilitated by the introduction of simulation based manufacturing checking software packages.

Insertion for phase shifting is still a matter of some debate. Originally, phase shifting structures were identified and added during photomask fabrication, after the layout had been created and verified. This gave the maskmaker certain flexibility in choosing which process or PSM technique would be most suitable to the equipment and requirements available.

However, phase conflicts can arise using this methodology [13], because original layout had already been determined and cannot be altered. This has motivated the push to create layouts with phase shifting anticipated by the place & route tool [14]. By forming the layout with phase rules in mind, phase conflict regions are prevented from ever coming into existence. This can work well to prevent the phase conflicts, but removes the flexibility that the mask shop may wish to retain.

A compromise has been successfully reached by inserting PSM creation and assignment also at the point of physical verification [15]. In this case, the manufacturability checks of the verification tool can identify any phase conflicts that might arise, and the ability to alter or edit the layout allowed at this point in the data flow still leaves room for these errors to be corrected. Since some of the metrics of the mask manufacturing process may be established by this point, some of the mask shop optimization can still be retained as well.

3. IMPACT OF RET ON LAYOUT

The adoption of each of these techniques, or a combination of them, provides certain advantages for lithographic manufacturing. However, each of these techniques also comes with trade-offs that cannot be ignored in the layout. The impact on physical design is different but significant in each case.

OAI: Off-axis techniques are introduced to enhance resolution, particularly of very small lines and dense pitches. This is illustrated in Figure 1, reproduced with data from reference 5. This figure shows the process depth of focus that can be achieved for Line/Space pairs of diminishing pitches, using a quadrupole illumination. Although eventually very small pitches are not resolved in either case, the graph shows a "resonance" that occurs when the illumination angle suitably corresponds to the light to be diffracted from the pitch grating.

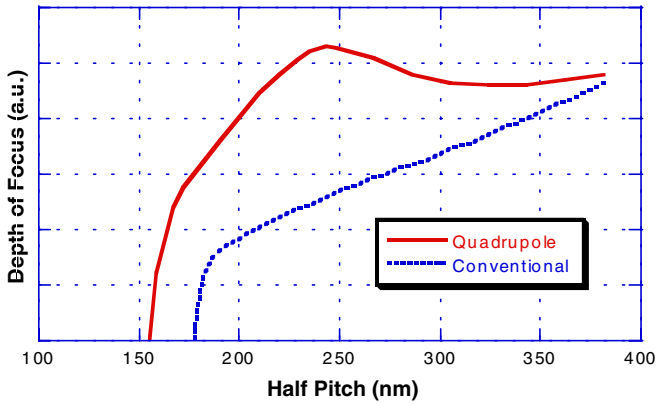

Figure 1: Pitch behavior of quadrupole illumination for vertical and horizontal lines, reproduced from Reference [5]. For this case (λ=248 nm, NA = 0.63), 250 nm lines and spaces are significantly enhanced with the quadrupole illumination.

This means in effect that certain large pitches are well reproduced, and certain very fine pitches are well reproduced, but certain intermediate pitches may not reproduced as well. This creates a rather complicated set of design rules, in which small features are allowed, large features are allowed, but certain intermediate pitches and feature sizes are forbidden.

An additional phenomenon inherent in certain designs of off-axis illumination is their asymmetry. This is most pronounced to lines orthogonal to the quadrupole orientation, i.e. diagonal lines at ±45°. Here, the lines are routinely reproduced until the resolution limit of the lens is reached, and then lithographic failure occurs at the same pitches that are dramatically enhanced for the vertical horizontal features.

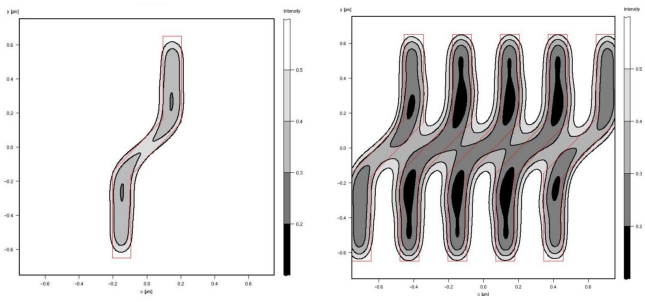

Figure 2: Imaging behavior of vertical and diagonal lines under Quasar illumination (similar to quadrupole). Only the black and darkest grey regions are formed as structures on the wafer. The images of the diagonal portions are very poor, and for isolated lines, are completely broken.

The consequence on imaging is illustrated in figure 2. Here, the image of a set of dense lines is illustrated, using a quadrupole – type illumination system. Although the vertical lines can print and be resolved, the diagonal jogs are poorly resolved, and the image contrast fades away.

A layout which allowed these diagonal lines would therefore fail utterly, since these lines would be severed on the wafer. This adds further complexity to the set of design rules, assuming that 45° lines had been allowed, or forces the additional restriction of prohibiting 45° lines altogether. In combination with the allowed

fine pitches, but forbidden intermediate pitches, the set of design rules for such a process becomes very counter intuitive.

Similar behavior is found in dipole illumination as well, where one orientation will only print horizontal lines, while the orthogonal orientation will only print vertical lines [3,6]. To assemble an entire layer, 2 masks and a double exposure are required, in addition to the restrictive rules found in quadrupole illumination.

OPC: The restrictions posed by OPC are less prohibitive, in that the small alterations to the layout features to facilitate diffractive effects are carefully chosen and calibrated to improve fidelity of the layout as given. This applies to both deterministic rule-based OPC, and to empirically calibrated model based OPC. However, certain types of OPC, notably the addition of SRAF (Sub Resolution Assist Features) can lead to further layout restrictions.

SRAFs are illustrated in Fig. 3. The additional small features, typically added to the photomask by some simple width and spacing rules, allow isolated or semi-isolated lines to diffract light like dense lines, and yet do not themselves print on the wafer. [16,17,8,19]. This can work well for bringing the lithographic performance of isolated and dense lines into agreement, but for the case of intermediate pitches, things can be more difficult. In this case, at times a single and at other times multiple assist features may be required [19]. Intermediate pitches where the transition occurs will often have sub-optimal performance.

If an intersection of assist features occurs, the junction may become larger than a sub-resolution feature, causing the spot to actually print on the wafer. These unwanted features can destroy the performance of the IC, so systematic checking mechanisms are required to "clean-up" any layout once SRAFs have been added. These additional steps, although not impacting design rules for original layouts directly, can significantly increase the complexity of verification. They also only detect the unwanted side-lobes if they are actually simulation based, so that the imaging effects are faithfully modeled.

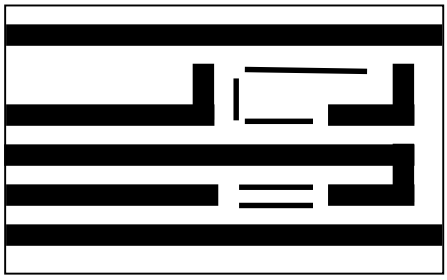

Figure 3: A representative layout including sub-resolution assist features (SRAFs). Although the large features print, the small ones do not.

PSM: As mentioned above, phase-shifting assignments have been inserted at various points in a layout flow, with varying degrees of success. The most important consideration is that phase shifting can truly enhance resolution for dense pitches, typically by a factor of 2 [10], and phase shifted interference effects allow for the formation of extremely thin dark lines, far below the minimum feature allowed in most design rules [15]. These fine features come at a price, however, usually in either the creation of an extremely expensive mask, or at the cost of a double exposure technique to remove unwanted phase artifacts.

Because the minimum feature and minimum pitch are indeed smaller, layouts anticipating phase shifting that allow these pitches need to be created by layout and library generation tools. However, it is important to understand the difference between creating phase-compliant layouts (which generate features suitable for manufacture by phase-shifting) and phase-shifted layouts themselves. Because the actual phase shifting process can be different at different photomask manufacturing locations, and at this time there is currently still no reliable method for inspecting and repairing phase shifted photomasks, refraining from the actual assignment of the exact sizes and shapes of the phase shifting polygons until these process boundary conditions are established is essential. This provides the flexibility for the mask maker to optimize his process, yet allows phase conflicts and structures to be generated in an EDA tool.

4. REMEDIES

4.1 Simulation Based Layout Checking

All of the physical phenomena of RET that create limitations on design rules are well understood, and can be modeled through simulation. Fast simulation tools have now been coupled to DRC tools, to allow a general, full chip check of the RET layout prior to manufacturing. This can catch errors caused by broken diagonal lines, improperly placed assist features, and phase conflicts, reporting these results just as normal DRC violations are reported.

Although sounding like a simple addition, the adoption of simulation based checking has not yet become a standard part of the tape-out procedure. This is primarily due to concerns over how long this additional checking step will take, since simulation tools are traditionally much slower than DRC tools. Fortunately, several EDA suppliers are now offering products for this purpose, and their adoption is expected to increase as the performance becomes tuned to guarantee overnight processing runs.

4.2 The Importance of a "Target" Layer

A major barrier, however, to the utility of any RET is the absence of a design process which insures that the layout, prior to any modifications that RET will provide, exactly matches the actual intent for the IC. Only if this is done will there be a clean handoff, which will allow RET to be used to their fullest potential. This is typically called the creation of a "target" layer.

Currently, when a layout is produced, it is often the result of various design rules, some created and used over the course of years. When various ICs are assembled from different libraries, created under different design rules, the result can be a mixture of styles and specifications. Typically, some of these rules, such as the addition of a line-end extension, were created long ago in response to the observation of a physical effect in an older process. This was long before such effects had a solution such as OPC to provide automatic compensation.

These rules are now often unconsciously reproduced, and actually represent a "legacy" OPC, grandfathered into the design through generations of rewritten design rules. This approach has many problems. First, the physical phenomena that OPC correct for are different with each process, so while these "legacy" rules may have been effective at one time, they may equally have lost effectiveness as well, harming the fidelity to the original intent.

Second, most OPC software programs, especially those inserted at verification to provide simulation based checks, assume that the

layout presented to it is the exact layer as the designer wishes it to appear on the wafer. The software then proceeds to verify that this will remain invariant with processing, or adds OPC features that insure that the final image converges to the initial input layer. When these "legacy" rules of ad hoc OPC have been added, this layout no longer really represents the designer's intent. The OPC program will faithfully attempt to make a mask that will produce an image that looks just like the layout presented, and in effect will add OPC to the "legacy" OPC structures. This can lead to wafer images that are not at all what the designer intended, and actually cause devices to fail.

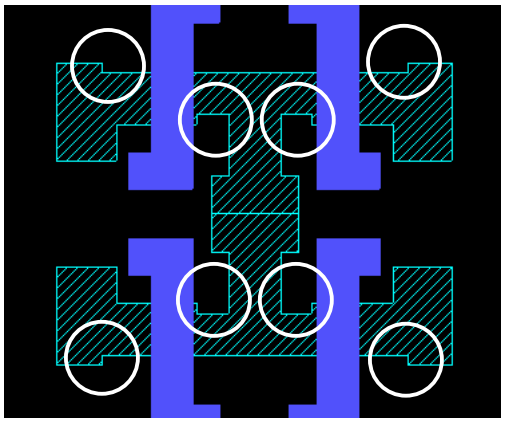

Figure 4: An example of a layout presented for OPC, constructed using design rules which had already created basic inner corner serifs and partial hammerheads (circled in white).

This is illustrated in figure 4. In this case, a portion of an SRAM layout is shown. The layout clearly has inner corner serifs and line end hammerhead structures already added, yet was presented to the OPC tool as the desired layer in good faith. Attempts to produce a working device with these small inner serifs retained would cause severe thinning on the wafer, reducing yield.

For this example, the only way to actually produce a correct OPC layout was to "de-OPC" the provided layout, using a set of rules to attempt to restore the layout to the designer's intent. Only once the OPC program was run on a clean "target" layout could yielding devices be produced.

5. CONCLUSIONS

The adoption of RET allows IC manufacturing to move forward several generations in an extremely cost effective manner. However, only when the design community consciously audits the origin of their layouts, assembles layouts that will cleanly represent the designer's intent, and routinely practices simulation based verification of the final RET layouts prior to manufacturing, will the new generations enabled by RET achieve their full potential.

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