Double-Gate Fully-Depleted SOI Transistors for Low-Power High-Performance Nano-Scale Circuit Design *

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ABSTRACT

Double-gate fully-depleted (DGFD) SOI circuits are regarded as the next generation VLSI circuits. This paper investigates the impact of scaling on the demand and challenges of DGFD SOI circuit design for low power and high performance. We study how the added back-gate capacitance affects the circuit power and performance; how to trade off the enhanced short-channel effect immunity with the added back-channel leakage; and how the coupling between the front- and back-gates affects circuit reliability. Our analyses over different technology generations using MEDICI device simulator show that DGFD SOI circuits have significant advantages in driving high output load. DGFD SOI circuits also show excellent ability in controlling leakage current. However, for low output load, no gain is obtained for DGFD SOI circuits. Also, it is necessary to optimize the back-gate oxide thickness for best leakage control. Moreover, threshold variation may cause reliability problem for thin back-gate oxide DGFD SOI circuits operated at low power supply voltage.

1. INTRODUCTION

The concept of device scaling has been consistently endorsed over the past few decades in meeting performance and power consumption requirements in VLSI circuits [1]. However, conventional device structures, such as bulk MOS transistors, are approaching fundamental physical limits [2]. As device dimensions shrink to submicron and below, the limits of conventional MOS structures are becoming more pronounced due to strong short-channel effect and quantum effect, causing the increase in performance to be limited. It is, therefore, necessary to look for new device structures to sustain the growth of the VLSI industry in the nano-scale generations. Double-Gate Fully-Depleted (DGFD) Silicon-on-Insulator (SOI) transistors can be a good technology choice for nano-scale circuits [1].

SOI technology has demonstrated many advantages over bulk silicon technology, such as low parasitic junction capacitance, high soft error immunity, elimination of CMOS latch-up, no threshold voltage degradation due to body effect, and simple device isolation process [3]. Recently, DGFD SOI structure has attracted particular attention due to its inherent robustness to short-channel effect and improved current drive capability [4][5]. Yet, much of the focus is at the device level. The advantages of DGFD SOI transistors come at the expense of an additional gate (back-gate), leading to high gate capacitance, dual leakage channels, and tricky front- and back- gates coupling, which complicates circuit design. In this paper, we attempt to address the design issues of DGFD SOI circuits. The demand and challenges of DGFD SOI circuits for low-power high-performance in the nano-scale region are investigated. We study how the increased gate capacitance and improved drive capability affect overall circuit performance and power dissipation, and how to trade off the added back-gate leakage with the superb short-channel effect immunity. The implications of coupling between front- and back-gates to the noise immunity and circuit reliability are also examined. The study is based on *International Technology Roadmap for Semiconductors* (ITRS) [1]. ITRS provides a 15-year outlook on the major trends in the semiconductor industry and is a good reference document for research of the outer years.

All device and circuit simulations are run on MEDICI, a powerful device simulation tool [6]. By solving Poisson's equation and the electron and hole current continuity equations, MEDICI models the two-dimensional distribution of potential and carrier concentration in a device to predict its electrical characteristics for any bias condition.

2. DGFD SOI DEVICES

2.1 DGFD SOI Device Structures

Fig. 1 (a) shows the cross section of a fully-depleted SOI transistor, where t_{of}, t_{si}, and t_{ob} represent front-gate oxide, silicon film, and back-gate oxide thickness, respectively. t_{of} is usually taken as the minimum oxide thickness for high performance. t_{ob} is usually larger than t_{of}. When the silicon film is thicker than the maximum gate depletion width, SOI exhibits a floating body effect and is regarded as a partially-depleted SOI MOSFET. If the silicon film is thin enough such that the entire film is depleted before the threshold condition is reached, the SOI device is referred as a fully-depleted SOI MOSFET [9]. Fully-depleted SOI is of interest in this paper.

The advance of process technology has made the fabrication of double-gate fully-depleted devices possible and eliminated the concerns in making a small well-aligned back-gate. Fig. 2 shows one of such technology using Epitaxial Lateral Overgrowth (ELO) [7]. A silicon island sandwiched with silicon dioxide is grown from the silicon substrate (Fig. 2 (a)). Reactive ion etch is used to define the Source/Drain cavities (Fig. 2 (b)) and another low temperature ELO with remaining silicon island as seed is used to grow the S/D

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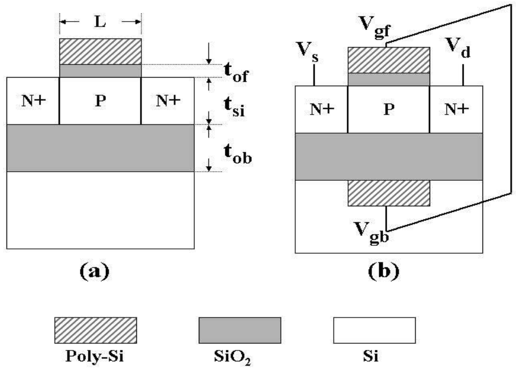

Figure 1: DGFD SOI MOSFETs.

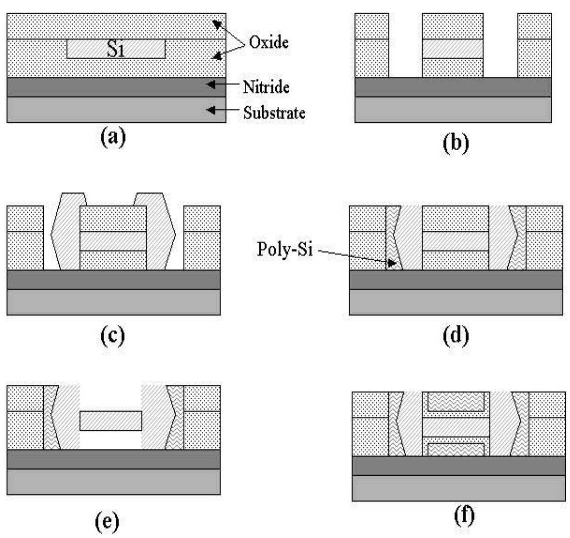

Figure 2: DGFD SOI Technology.

contact (Fig. 2 (c)). S/D cavities is then filled with polysilicon (Fig. 2 (d)). Wet etchiing is used to remove the top and bottom oxide dummy gates (Fig. 2 (e)). Then gate oxide can be grown on the channel region (Fig. 2 (f)). Finally an in-situ doped LPCVD polysilicon deposition is used to refill the etched gate cavities.

There are several connections of front- and back-gates in circuit applications [8]. If the back-gate is left open or connected to supply voltage (V_{dd} for PMOS and ground for NMOS), the device is then called single-gate transistor. Single-gate transistor usually has very thick back-gate oxide so that the channel can be effectively isolated from the substrate. A more promising application of fully-depleted SOI transistors is to take advantage of the coupling between front- and back-gates. The back-gate oxide is made relatively thin and two gates are tied together (Fig. 1 (b)). We call such transistor as double-gate transistor. However, even with the front- and back-gates tied together, when the back-gate oxide is very thick, the two gates are physically decoupled, and circuits act as single-gate circuits. This paper analyzes how the back-gate coupling affects circuit performance and power dissipation. By increasing the back-gate oxide thickness, the circuit changes from symmetric double-gate, to asymmetric double-gate, and finally to a single-gate circuit.

Table 1: Device Parameters for High Performance MPUs.

Year Technology Nodes	2002 130nm	2005 100nm	2008 70nm	2011 50nm	2014 35nm
Gate Length (L_n, L_p) (nm)	85	65	45	32	22
Gate Oxide Thickness (t_{of}) (nm)	1.9	1.5	1.2	0.8	0.6
Channel Doping (N_a) $(10^{18}cm^{-3})$	2.5	6.0	9.0	15	25
Supply Voltage (V_{dd}) (V)	1.5	1.2	0.9	0.6	0.6
Performance (f_{clk}) (MHz)	1600	2000	2500	3000	3600

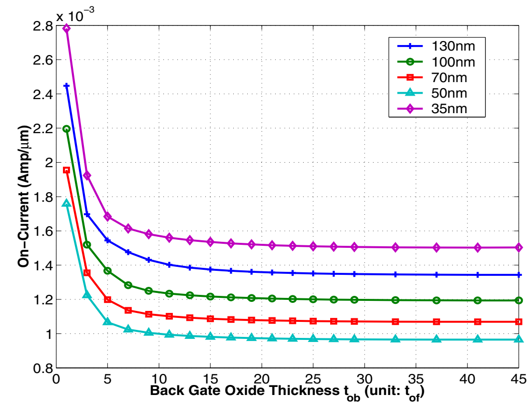

Figure 3: On-current of N-Channel DGFD SOI transistor.

2.2 DGFD SOI Device Characterization

DGFD SOI device characteristics are studied in the view of scaling. By increasing the back-gate oxide thickness, we study how the front- and back-gate coupling affects on- and off-currents. *International Technology Roadmap for Semiconductors* (ITRS) [1] is used as the guideline. ITRS identifies the trends and challenges and projects the targets and requirements of the VLSI technology. Table 1 lists the parameters of high performance MPUs for the upcoming five technology generations. The silicon film thickness, t_{si}, is taken as $5t_{of}$ to guarantee the full depletion of the body. Our study focuses on high performance applications of DGFD SOI devices and therefore the threshold voltages are set as $V_t = \frac{1}{5}V_{dd}$. By uniformly setting $t_{si} = 5t_{of}$ and $V_t = \frac{1}{5}V_{dd}$, we enable the comparability among the technology generations.

Fig. 3 plots the on-current of N-Channel DGFD SOI transistors versus the back-gate oxide thickness for five technology generations. In this figure, and in all the following figures, left ends of these curves represent the symmetric DGFD SOI transistors ($t_{of} = t_{ob}$) and right ends represent SGFD SOI transistors ($t_{of} \ll t_{ob}$), while in-between are the asymmetrical DGFD SOI ($t_{of} < t_{ob}$). Back-gate oxide thickness t_{ob} is taken as a multiple factor of front-gate oxide thickness t_{of} for two reasons: First, it reflects the scaling of physical dimensions over technology generations, and second, it guarantees the comparability across the technology generations.

From Fig. 3 We observe that on-current decreases from one technology generation to another. This is due to the decrease of power supply voltage over technology generations to accommodate the aggressive down scaling of physical dimensions. Fig. 3 also shows that on-current increases significantly with thinner back-gate oxide. Under same threshold voltage, symmetric DGFD transistors have on-current which are almost double that of SGFD transistors. Two factors contribute to the lack of current doubling: the stronger source/drain resistance effect of symmetric DGFD transistors and the stronger DIBL effect of SGFD transistors. Nevertheless, the

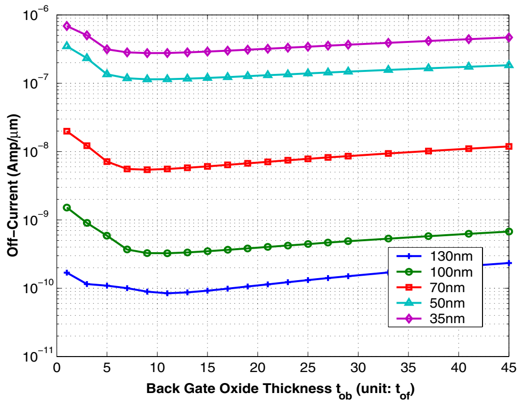

Figure 4: Off-current of N-Channel DGFD SOI transistor.

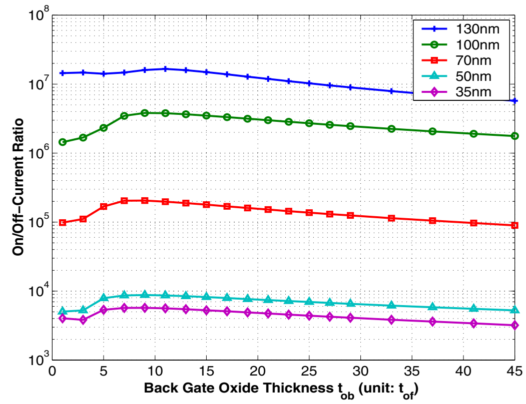

Figure 5: On/Off-current ratio of N-Channel DGFD SOI transistor.

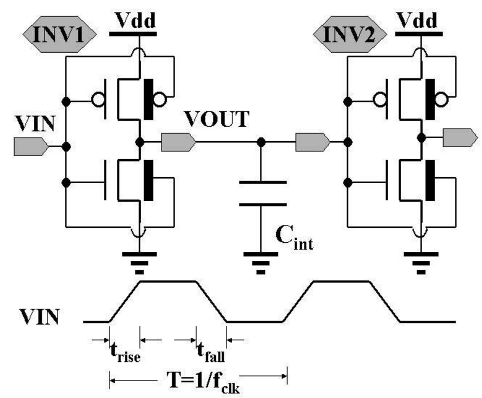

Figure 6: Circuit with an inverter driving another inverter.

high drive capability makes DGFD SOI very attractive for high performance applications.

There is an exception in Fig. 3, however. $35nm$ node has higher on-current than any other technology generations. ITRS suggests that V_{dd} should be maintained at $0.6V$ for $35nm$ node even though the physical dimensions are scaled aggressively. Maintaining high supply voltage poses serious problem to the off-current control and device reliability, since the field in the gate dielectric and channel may not be possible to control within some reasonable levels.

The off-current versus back-gate oxide thickness for five technology generations are plotted in Fig. 4. I_{off} is measured with $V_s = V_{gf} = V_{gb} = 0$ and $V_d = V_{dd}$. It can be seen that down to $100nm$ node, leakage is well within tolerable limit ($< 10^{-9} Amp/\mu m$ as required by ITRS). But beyond $70nm$ node, leakage current is of concern.

A surprising observation from Fig. 4 is that the lowest off-current does not occur when the back-gate oxide is thinnest. Rather, there is an optimal thickness that results in lowest off-current. The off-current of a DGFD SOI transistor is the combined leakages induced by both front- and back-gates. Recall that subthreshold slope is a function of depletion capacitance C_d and gate capacitance C_{ox} and can be descripted as

$$s = \frac{kT}{q} log(1 + \frac{C_d}{C_{ox}}). \qquad (1)$$

The symmetrical structure of front- and back-gate implies that only half depletion region is control by both gate and the C_d for each gate is doubled. Therefore, although the thinner back-gate oxide offers better body potential control, the leakage is actually higher. Therefore, there is a trade-off between improving the short-channel effect immunity and reducing high leakage induced by back-gate.

A better measurement of device characteristics is the on/off current ratio. Fig. 5 plots the on/off current ratio versus back-gate oxide thickness. On/off current ratios decrease significantly beyond $70nm$ node. In fact, they are so low for $50nm$ and $35nm$ nodes that leakage power may play significant role in overall power dissipation. From Fig. 5 we again observe that there are optimal back-gate oxide thicknesses for highest on/off current ratios.

3. DGFD SOI CIRCUIT DESIGN

The inverter circuit shown in Fig. 6 is used as the vehicle for DGFD SOI circuit study. $INV1$ and $INV2$ are two identical inverters with $W_n/L_n = 5$ and $W_p/L_p = 10$. The transistor structures are the same as shown in Section 2. That is, their parameters are taken from ITRS, $t_b = 5t_{of}$, and $V_t = \frac{1}{5}V_{dd}$. C_{int} is the interconnect capacitance. Such a configuration reflects the typical circuit composition and is sophisticated enough to capture the fundamental properties of the real circuits [9], yet compact enough to run on the device simulation tool such as MEDICI.

We take the pulse waveform as the input. The rise and fall times are set as $\frac{T}{6}$, where $T = \frac{1}{f_{clk}}$ is the clock period. The delay, τ, is the time period from the 50% point of the input to the 50% point of the output of $INV1$. The total average power dissipation of a CMOS inverter is measured as

$$P_T = \frac{1}{T}\int_0^T I(t) \cdot V_{dd} \cdot dt, \qquad (2)$$

In CMOS digital circuits, power dissipation consists of dynamic and static components. $I(t)$ is the sum of dynamic and standby leakage current.

3.1 Dynamic Power Dissipation and Circuit Performance

Fig. 7 plots the power dissipation of the inverter with respect to different interconnect loads, C_{int}, for the $50nm$ node (C_{inv} is the equivalent load capacitance of the SGFD SOI inverter ($t_{ob} \gg t_{of}$)). The switching activity ω is set to be 1. Based on our measurements, the power dissipation under this condition is dominated by the load capacitance. Leakage power is insignificant.

Fig. 7 shows that thinner back-gate oxide circuits consistently have higher power dissipation due to higher inverter ($INV2$) gate

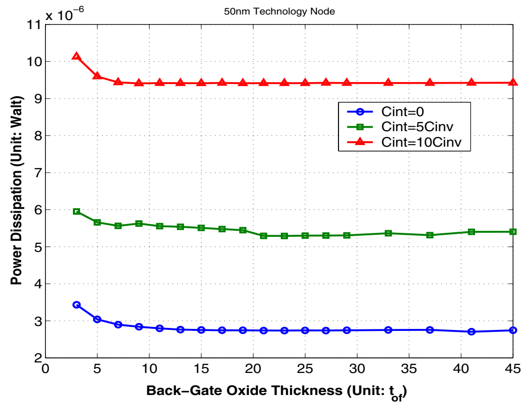

Figure 7: Power dissipation of the inverter at $50nm$ node.

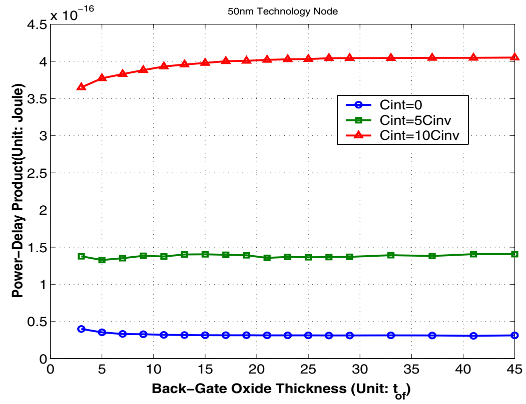

Figure 9: Power-delay product of the inverter at $50nm$ node.

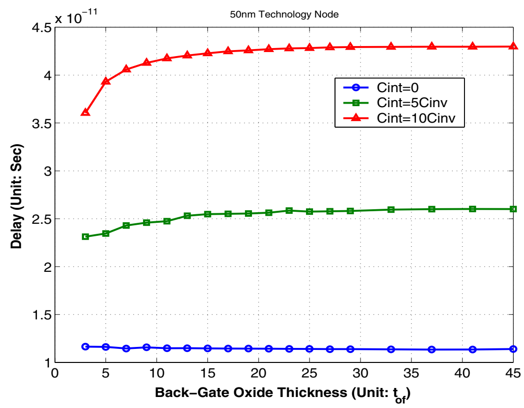

Figure 8: Delay of the inverter at $50nm$ node.

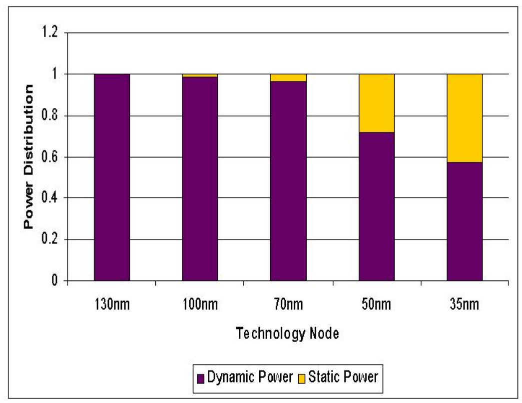

Figure 10: Fractions of dynamic and static power.

load. This is the price DGFD SOI circuits pay for high performance. Unfortunately, thinner back-gate oxide does not always result in better performance. Fig. 8 plots the delay of the inverter with respect to different interconnect capacitances for the $50nm$ node. With zero interconnect load, that is, when the output load of $INV1$ is dominated by the gate capacitance of $INV2$, thinner back-gate oxide circuit has higher delay despite its higher drive capability (refer to Fig. 12 for enlarged delay plot). This implies that the increase in drive current due to the coupling of the back-gate is not sufficient to compensate the increase in gate capacitance.

However, when C_{int} is increased to $5C_{inv}$, or $10C_{inv}$, significant performance gain is obtained. The higher the interconnect load, the more gain is obtained by thinner back-gate oxide DGFD SOI circuits.

A quality measure of a logic gate, which combines both power and performance, is the power-delay product ($PDP = \tau \times P_T$). Fig. 9 plots the power-delay product of the inverter with respect to different interconnect loads for the $50nm$ node. Again, we observe that thicker back-gate oxide SOI circuits have lower *PDP* than thinner ones when the interconnect load is around 0. But when $C_{int} = 10C_{inv}$, significant *PDP* reduction is obtained with thinner back-gate oxide. From Fig. 9, we see an interesting transition in *PDP* curves. When $C_{int} = 0$, the left end of the curve bends upward, while when $C_{int} = 5C_{inv}$, it remains almost flat, and finally when $C_{int} = 10C_{inv}$, it bends downward. At $C_{int} = 5C_{inv}$, the delay gained by DGFD SOI circuits is offset by the increase in power dissipation so we do not see significant PDP difference for different back-gate oxide thicknesses. However, at $C_{int} = 10C_{inv}$, significant performance improvement due to DGFD SOI circuits overrides higher power dissipation. Therefore, better PDP is obtained for thinner back-gate oxide DGFD SOI inverter. We conclude that DGFD SOI circuits are suitable for high output loads, or high interconnect loads.

It should be noted that although the above discussion is based on $50nm$ technology node, our simulations were performed over all five generations and similar observations were obtained.

3.2 Static Power Dissipation and Circuit Performance

In the previous subsection, we assume that $\omega = 1$, i.e., circuit switches at every clock cycle. In reality, however, the switching activities of most circuit blocks are relatively low. Low switching activity lowers the dynamic power dissipation and increases the fraction of static power in overall power consumption. By varying the switching activity, this section studies the static power dissipation of DGFD SOI circuits.

Fig. 10 plots the fractions of dynamic and static power at $\omega = 0.01$ and $C_{int} = 0$ for the inverter circuits with $t_{ob} = 5t_{of}$. The fraction of static power increases steadily from $130nm$ node down to $35nm$ node. In fact, the fraction of static power dissipation at $50nm$ and $35nm$ nodes is so significant that it is comparable to dynamic power and cannot be ignored.

Fig. 11 plots the power dissipation of inverter circuit for $\omega = 0.01$ and $C_{int} = 0$ for five technology generations. Down to $70nm$

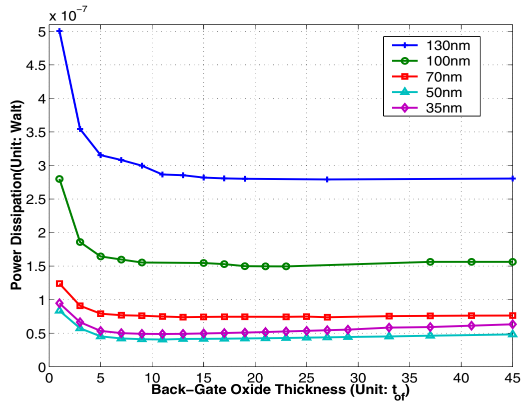

Figure 11: Power dissipation of inverter circuit at $\omega = 0.01$.

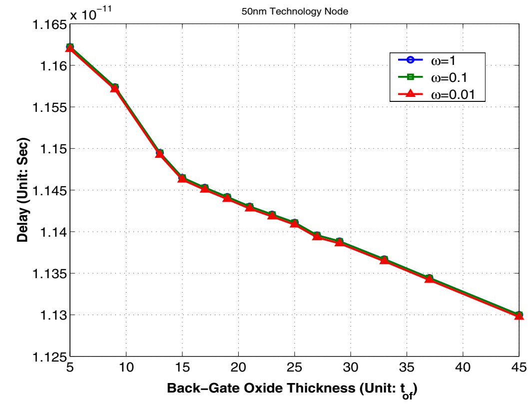

Figure 12: Delay of inverter circuit at $50nm$ Node for different switching activity.

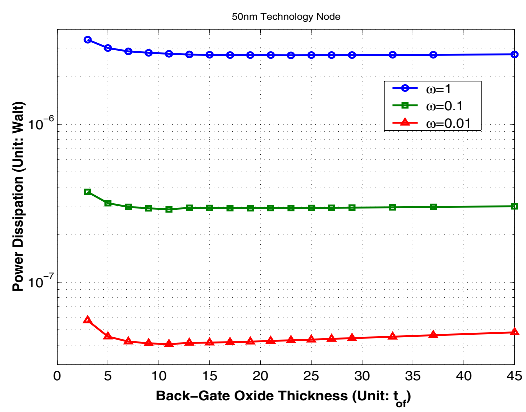

Figure 13: Power dissipation of inverter circuit at $50nm$ node for different switching activity.

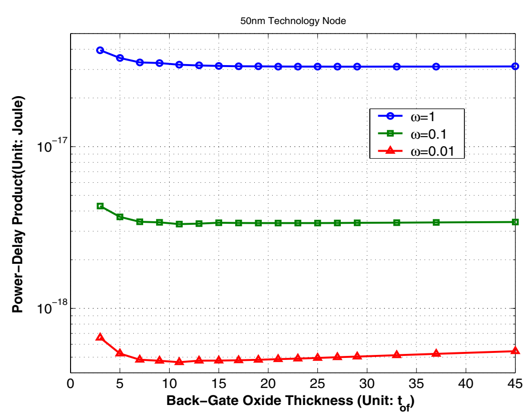

Figure 14: Power-delay product of inverter circuit at $50nm$ node for different switching activity.

node, the power dissipation is dominated by the dynamic component and the curves display the same shape which we saw in the previous subsection (Fig. 7). That is, thicker back-gate oxide results in lower power dissipation. However, beyond $70nm$, the strong short-channel effect induces high leakage, and strongly modifies the power dissipation curves. There exists an optimal back-gate oxide thickness that results in lowest static power dissipation, and hence, lowest overall power dissipation. Thicker back-gate oxide circuits are not necessarily associated with smaller power consumption beyond $70nm$ technology generation. Hence, optimization of back-gate oxide thickness for low power is required.

To illustrate the effect of leakage power in overall power dissipation, we take $50nm$ technology node as an example, and plot the delay, power, and power-delay product with respect to switching activity $\omega = 1$, 0.1, and 0.01 as shown in Figs. 12, 13, and 14 ($C_{int} = 0$). It is not surprising to see the delay curves for different switching activities are similar, since altering the switching activity does not affect the circuit performance. However, when the switching activity is reduced, overall power dissipation is reduced as well due to the decrease in dynamic power consumption. Decrease in dynamic power consumption, in turn, increases the fraction of static power in overall power dissipation. Unlike the conclusions we have drawn in the previous subsection, when the static power becomes significant (such as for $50nm$ and $35nm$ nodes), thicker back-gate oxide SOI circuits do not necessarily show better power-delay product. Hence, optimization of the back-gate oxide thickness is necessary in achieving best performance and best power dissipation.

4. THRESHOLD VOLTAGE VARIATION

With the continuous scaling of the technology, the circuit reliability due to threshold variation is expected to become more serious [1]. In this section we study the effect of the transistor threshold variation on DGFD SOI circuits. The threshold voltage of DGFD SOI transistor is a function of front- and back-gate biases and gate surface states (depletion or inversion). For simplicity, we take a symmetric N-channel DGFD SOI transistor as an example. Similar evaluation can be extended to other DGFD SOI transistors.

For a symmetric N-channel transistor, assume that both front and back-gate threshold voltages at zero bias are $V_{t0} = \theta V_{dd}$ ($\theta < 1$), and $\gamma_f = \gamma_b = \gamma$, where γ_f is the back-gate effect on front-gate threshold voltage, and can be obtained by [3]

$$\gamma_f = \frac{dV_{thf}}{dV_{gb}} = \frac{C_{si}C_{ob}}{C_{of}(C_{si} + C_{ob})}; \tag{3}$$

γ_b is the front-gate effect on back-gate threshold voltage and can be otained with similar equaitons:

$$\gamma_b = \frac{dV_{thb}}{dV_{gf}} = \frac{C_{si}C_{of}}{C_{ob}(C_{si} + C_{of})}, \quad (4)$$

The threshold voltage at saturation, V_{ts}, then can be expressed as

$$V_{t0} - \gamma V_{ts} = V_{ts}. \quad (5)$$

Thus, $V_{ts} = \frac{1}{1+\gamma}V_{t0} = \frac{\theta V_{dd}}{1+\gamma}$, and the saturation current, using α-power law model [10], is given by

$$I_{sat} \propto (V_g - V_{ts})^{\alpha} = [(1 - \frac{\theta}{1+\gamma})V_{dd}]^{\alpha}. \quad (6)$$

Now, assume that there is a threshold voltage variation, induced by noise or process variation, so that $V_{t0} \rightarrow V_{t0} + \delta V_t$, then the new threshold voltage at saturation is given by $V'_{ts} = \frac{\theta V_{dd}}{1+\gamma} + \frac{\delta V_t}{1+\gamma}$, and the new saturation current is

$$I'_{sat} \propto [(1 - \frac{\theta}{1+\gamma})V_{dd} - \frac{\delta V_t}{1+\gamma}]^{\alpha}. \quad (7)$$

The percentage change in saturation current, η, due to V_t variation, can be estimated as follows:

$$\eta = \frac{I'_{sat} - I_{sat}}{I_{sat}} \times 100 = \{[1 - \frac{\delta V_t}{V_{dd}(1+\gamma-\theta)}]^{\alpha} - 1\} \times 100. \quad (8)$$

If δV_t is positive, then a reduction in saturation current is expected. One fact can be readily deduced from Equation (8) — lower supply voltage results in higher saturation current variation. That is a disadvantage that may limit the performance of DGFD SOI circuits for low-power operation. It should be pointed out that process variation or noise is relatively constant and can not be scaled down when the device dimensions or supply voltage are aggressively reduced. The impacts of variation on circuit performance and reliability of DGFD SOI circuit are expected to become severe for $70nm$ technology and beyond when supply voltages are low.

At first sight, we may conclude that higher saturation current variation would come from thinner back-gate oxide due to larger γ_f (γ_f increases when t_{ob} decreases, as indicated by Equation (3)). Recall that the current in a DGFD SOI transistor is induced by both front- and back-gates. γ_b, however, reduces when t_{ob} decreases (Equation (4)). Equations (3) and (4) show that the decrease of γ_b is more significant than the increase of γ_f when t_{ob} decreases. Therefore, more saturation current variation may actually be expected with thinner back-gate oxide.

The above analysis is confirmed by our MEDICI simulation. The simulation is done on N-Channel DGFD SOI transistors. δV_t is assumed to be the thermal voltage $\frac{KT}{q} = 26mV$ and the device structures are assumed to be the same as those described in Section 2. Fig. 15 plots the saturation current degradation (in percentage) due to δV_t for different back-gate oxide thicknesses. It is clear from Fig. 15 that the variation becomes significant from less than 3% for $130nm$ technology up to as much as 10% for $35nm$ technology. Moreover, comparing the variation with different back-gate oxide thicknesses shows that thinner back-gate oxide DGFD transistors at $35nm$ node have up to 3% more variation than thicker ones, while the difference at $130nm$ node is negligible.

5. CONCLUSIONS

Based on the projection of ITRS, we investigate the impact of scaling on DGFD SOI circuits. We observe that DGFD SOI devices are suitable for circuits with high interconnect load. When the

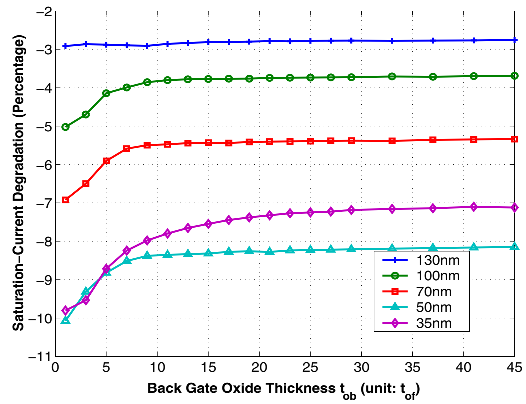

Figure 15: Saturation current degradation due to increase of threshold voltage.

leakage current becomes significant, optimization of back-gate oxide thickness is necessary to achieve better leakage current control and better power dissipation, as well as better power-delay product. We also found that variation of threshold voltage can be of concern for DGFD SOI circuits, particularly for low supply voltage operations.

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