Vertical Integration of Submicron MOSFETs in Two Separate Layers of SOI Islands Formed by Silicon Epitaxial Lateral Overgrowth

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ABSTRACT

Reported here is the vertical integration of submicron P-MOSFETs in two separate layers of SOI device islands fabricated using the selective epitaxial growth and epitaxial lateral overgrowth of silicon (SEG/ELO). The fabrication technique has the potential for three-dimensional device integration. Underlying P-MOSFETs in the first SOI device layer experienced all the process steps required to fabricate devices on the second layer SOI islands. The fully-depleted first layer SOI P-MOSFET device (L_{eff}= 0.6 µm) characteristics showed normal MOSFET behavior, low off-state leakage currents below 0.2 pA/µm with a subthreshold slope as low as 65 mV/dec. The P-MOSFETs in the second SOI layer (L_{eff}= 0.4 µm) showed normal device characteristics similar to those fabricated in the first SOI layer without second level devices.

Keywords

silicon, silicon on insulator, three dimensional circuits, SOI MOSFET, selective epitaxial growth, thin film SOI

1. INTRODUCTION

Continued conventional bulk MOSFET device scaling will eventually reach its performance limit, thus new fabrication methods need to be investigated [1,2]. Fabrication of devices and circuits in multiple layers of SOI (MLSOI) will be necessary to increase the number of transistors integrated into a given volume and enhance the circuit performance by reducing interconnect delay via vertical interconnection [3].

Three-dimensional (3-D) stacked device structures and circuits have been already demonstrated in various forms of SOI-type techniques. These include zone-melt re-crystallization [4-6] and more recently, metal seeded crystallization [7], and the selective epitaxial growth and epitaxial lateral overgrowth of silicon (SEG/ELO) [8,9]. To fabricate high performance deep-submicron devices in 3-D MLSOI, a very thin, uniform and high quality SOI material is required. SEG/ELO is an alternative and cost-effective SOI technique, which has been applied to fabricate self-aligned double-gate MOSFETs [10] and advanced 3-D device structures and has shown excellent material quality and fabrication process flexibility [11].

SEG/ELO has been used to form SOI P-MOSFETs on top of underlying substrate N-MOSFETs [9]. However, the thermal budget to produce MLSOI deep-submicron devices in 3-D SOI is a concern using the SEG/ELO technique. A unique process, which allows the formation of fully-planar and self-isolated device sized SOI islands in multiple levels has been developed [11]. The MLSOI islands were formed entirely by SEG/ELO using commercial cold wall RPCVD RF-heated pancake-type reactor.

For the first time, vertical integration of submicron P-MOSFETs in two different SOI layers formed by ELO and the resulting device characteristics is to be reported. Underlying P-MOSFETs in the first SOI layer have experienced all the required process steps to fabricate devices on second layer SOI islands. This fabrication process has the potential for 3-D vertical integration. The electrical performance of the submicron P-MOSFETs in the first SOI layer demonstrate the feasibility of stacking deep-submicron MOSFETs. The first level P-MOSFETs in the buried SOI layer are the worst case scenario due to the lateral Boron diffusion caused by the large thermal budget.

2. DEVICE FABRICATION

The first SOI layer (SOI-1) device islands were created as discussed in [11]. P-MOSFETs with drawn gate lengths down to

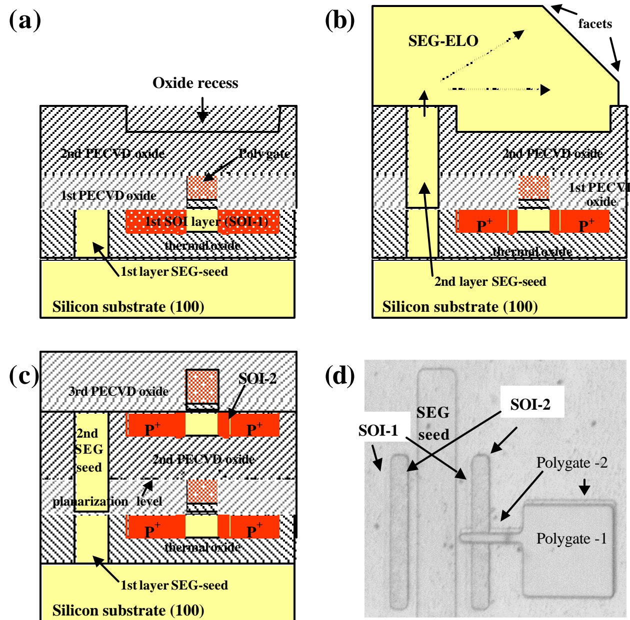

Figure 1. Key fabrication process steps of P-MOSFETs, a) after first layer SOI P-MOSFET device fabrication and Boron implantation followed by first PECVD oxide CMP and oxide recess pattern in the second PECVD field oxide, b) Second SEG growth from the exposed second SEG-seed window, c) CMP process to planarize and remove excess SEG down to the field oxide level, and d) Top-view microphotograph showing vertical integration of MOSFETs in two different SOI layers. Shown are devices with drawn gate length of 2 µm.

1.25 µm were fabricated and implanted with Boron (dose: 1 x 10^{14} cm^{-2}, energy: 25KeV). Boron activation and drive-in annealing were not carried out immediately, as the second SEG cycle for the fabrication of the second SOI layer (SOI-2) is more than sufficient. An initial PECVD field oxide deposited over the SOI-1 devices and a chemical mechanical planarization (CMP) process was used to planarize the wafer down to the polysilicon gate level. A second deposition of thick (~500 nm) PECVD field oxide was used as an interlevel dielectric (ILD) and to create the SOI oxide wells for the SOI-2 devices. The SOI-2 device islands were formed by a second SEG/ELO growth into the pre-defined oxide wells (Figure 1a) at T=970°C, P=40 Torr for 140 min using SiH_2Cl_2 (0.22slm), HCl (0.66slm), and H_2 (60slm) (Figure 1b). Excess SEG over the field oxide level was removed using CMP and formed the second level SOI device islands (Figure 1c). Using a typical MOSFET process, P-MOSFETs were fabricated on SOI-2 device islands with gate lengths down to L_{eff} = 0.4 µm using E-beam lithography. No salicide process was used to lower series resistance in the device fabrication process. Figure 1c shows the schematic cross section of the fabricated P-MOSFETs in two SOI layers. The SOI-1 P-MOSFETs went through all the thermal steps to fabricate second level devices on SOI-2. Devices can be fabricated in the bulk Si substrate as well and the fabrication of N-MOSFETs in SOI-1 and P-MOSFETs in SOI-2 for stacked CMOS application can also be made. SOI islands size down to 150 nm x 150 nm have been produced, thus a significant reduction of thermal budget can be achieved for nanoscale device fabrication [11].

3. EXPERIMENTAL RESULTS

Figure 1d is a top-view microphotograph showing the vertically stacked SOI P-MOSFETs in two different SOI layers. The devices are intentionally misaligned for the purpose of viewing. The SOI-2 devices on top of the SOI-1 were removed and contact was made to the SOI-1 devices, which were then tested. The SOI-1 P-MOSFETs had gate oxide thickness of 16 nm to prevent Boron outdiffusion from the polysilicon gate during the thermal cycles. Thinner gate oxide or nitrided oxides can be used for shorter SEG/ELO growths. Figure 2 shows the measured DC characteristics of SOI-2 P-MOSFET devices (L_{eff}/W= 0.4/5) with subthreshold slope of 118 mV/decade and low off-state leakage currents below 0.2 pA/µm. Figure 3 shows the subthreshold plots of a fully-depleted bottom layer SOI-1 P-MOSFETs (L_{eff}/W= 0.6/5) with SOI-1 and buried oxide thickness of 100 nm and 140 nm, respectively. Low current drive was due to very large series resistance, which came from (1) large gate to contact spacing of several microns, (2) reduced S/D doping due to Boron outdiffusion into ILD, (3) large LDD region formed by lateral Boron diffusion. An inverse subthreshold slope of 65mV/dec was measured when the back interface was depleted. An increased GIDL current was observed (indicated in Figure 4a) due to the Boron out diffusion

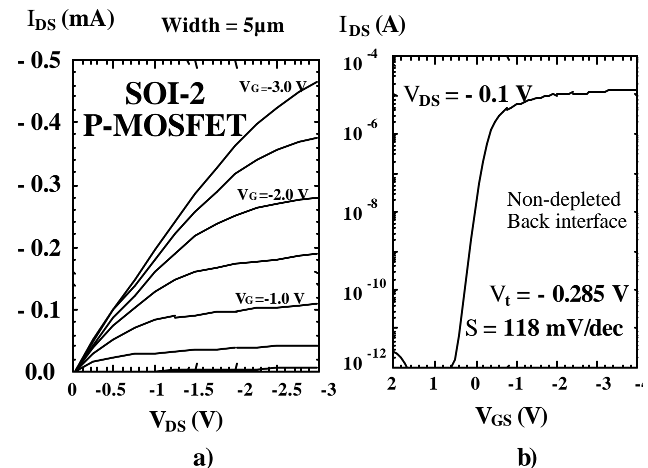

Figure 2. Measured electrical characteristics of L_{eff} = 0.4 µm (Width = 5µm) SOI P-MOSFET in the second SOI layer, a) I_{DS}-V_{DS} characteristics with V_G step of 0.5 V, and b) Subthreshold characteristics at V_{DS} = -0.1 V.

after the long high temperature heat treatment. Figure 4b shows the subthreshold plot of the L_{eff} = 0.65 µm P-MOSFET device in the SOI-1 without top SOI-2 devices. This device had a gate oxide thickness of 6.5 nm and PtSi contacts. No enhanced GIDL currents were observed. All the fabricated P-MOSFET devices had low off-state leakage currents below 0.2 pA/µm for V_{DS} = -0.1 V. Figure 5 shows a cross sectional SEM of a SOI-2 P-MOSFET over on SOI-1 layer. Future process improvements will enhance overall device operation, such as higher quality ILD between the SOI levels to improve subthreshold characteristics [13], and SEG/ELO growth in a single wafer epitaxial system to reduce the growth time by an order of magnitude.

4. CONCLUSION

Vertical integration of submicron P-MOSFETs in two different SOI layers using previously developed MLSOI technique has been reported for the first time. P-MOSFETs were investigated, as they are more prone to degradation for large thermal budgets due to Boron dopant outdiffusion and gate penetration. The P-MOSFET device in the first SOI layer showed typical MOSFET behavior after required processes to fabricate second SOI layer P-MOSFET. SEG/ELO growth temperature and duration can be reduced to relieve the thermal budget for the fabrication of stacked deep-submicron devices. The flexibility of developed process allows various types of devices, such as bulk MOSFETs and N-MOSFETs to be used also.

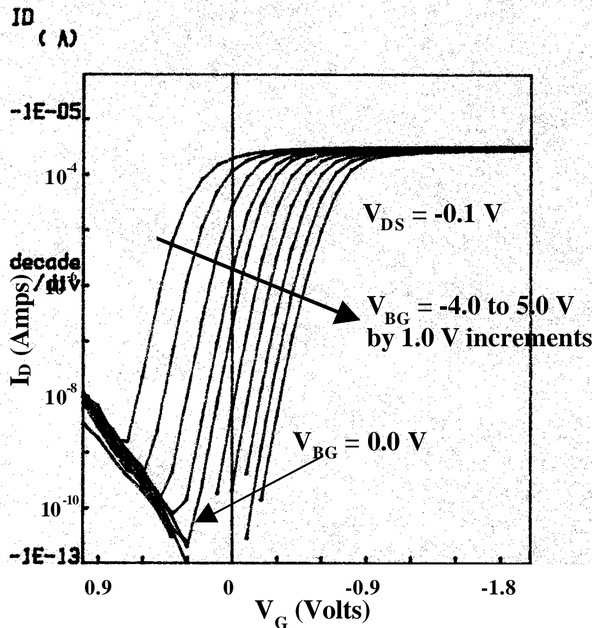

Figure 3. Measured subthreshold characteristics of L_{eff} = 0.6 mm (W = 5 mm) fully-depleted SOI P-MOSFET in the first SOI layer after all the process steps to fabricate devices on the second SOI layer. The subthreshold characteristics are with applied back bias to deplete or accumulate the back interface.

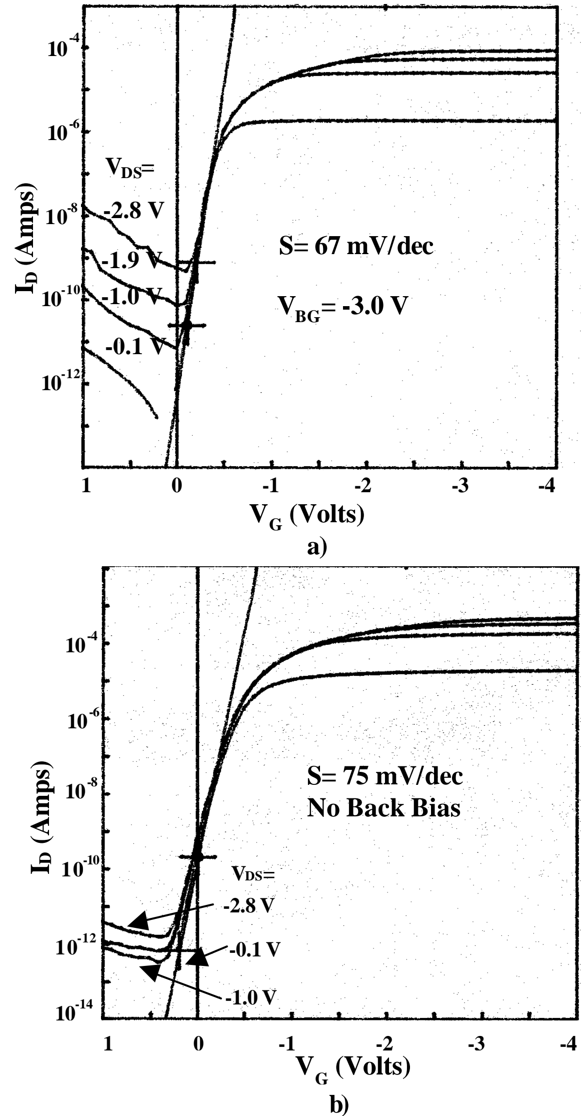

Figure 4. Measured subthreshold characteristics of a) SOI-1 device with SOI-2 fabrication process, L_{eff} = 0.6 mm (W= 5 mm). Notice the increase in GIDL current. V_{DS} steps are -0.9 V and back bias of V_{BG} = -3.0V was applied to deplete the back interface. Subthreshold slope of 66.5 mV/dec was measured for this case, and b) SOI-1 P-MOSFET without SOI-2 fabrication process L_{eff} = 0.65 mm (W= 5mm). No GIDL current was observed for thin gate oxide thickness of 6.5 nm.

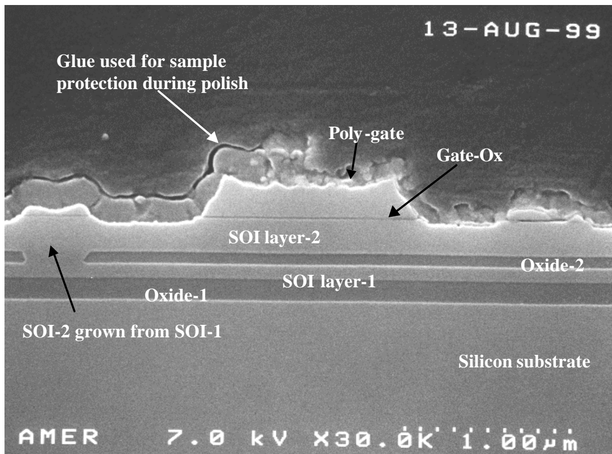

Figure 5. Cross sectional SEM of second level P-MOSFET over first layer SOI material. The second layer seed window is from the first layer material.

5. ACKNOWLEDGMENTS

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