Hierarchical Model Order Reduction for Signal-Integrity Driven Interconnect Synthesis

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ABSTRACT

The goal of this paper is to establish the basic framework and theoretical foundations for the hierarchical model order reduction with an emphasis on signal integrity analysis. The proposed algorithm, HMOR (Hierarchical Model Order Reduction), performs model reduction for both linear elements and independent sources simultaneously and hierarchically. Hence it is very suitable for fast timing and signal integrity analysis for tightly coupled RLC interconnects or with lots of independent sources such as power delivery circuits. It can fully utilize RICE [9] and PRIMA [11] to perform moment matching in the subcircuits to achieve the best performance and reduction ratio with passivity guarantee. HMOR significantly speeds up the simulation time for minor modified circuits. Combining with hierarchical interconnect synthesis algorithms such as routing, sizing and repeater insertion, HMOR can speed up N times over flat analysis where N is the number of circuit elements in the tree. In addition, we also develop a FM-based partition algorithm to partition the circuit into small weak-coupled blocks to enhance runtime. This extension enables HMOR to handle the interconnect topology with loops, meshes, even with complicated current return paths.

1. INTRODUCTION

The relentless push for density and performance drives the feature size of the VLSI technology to deep sub-micron and the clock frequency to giga hertz regime. This continuous condensation in both time and space enforces VLSI interconnects to exhibit complicated microwave behaviors. As a result, the traditional RC based interconnect methodology needs to be significantly revised in order to take inductance effects into consideration to improve the circuit analysis accuracy. Furthermore, the tightly electric and magnetic coupled 3-D interconnect structures induce unexpected interferences between signals which may create potential errors in both logic and timing. Therefore, signal integrity becomes one of the primary concerns for the high-end VLSI design.

Designs are subjected to frequent modifications. It is extremely inefficient to do full-blown analysis every time when we make slight modification of the circuits. In addition, design reuse has become a popular design methodology to save design efforts and reduce time to market. In both cases, hierarchical modeling can potentially speed up design cycle by preserving the analysis result of the unmodified parts in the circuit and directly plugging into the reduced module.

MOR (Model Order Reduction) has shown to be a very efficient way to speed up the interconnect analysis [9], and has been widely studied and improved over the last decade [9, 6]. Although the accuracy and stability of MOR methods have been improved, there seems to be a lack of framework and theoretical foundations to facilitate the hierarchical analysis. More precisely, most proposed hierarchical MOR methods [7, 5] are targeting relatively simple cases with only one or two ports with no noise analysis capability. We are exactly targeting to solve those issues.

In this paper, we endeavor to establish the basic framework and theoretical foundations for the hierarchical model order reduction with an emphasis on the signal integrity analysis. We not only present efficient hierarchical moment computation methods for noisy RLC trees but also provide a general framework to perform the hierarchical multi-port model order reduction.

The proposed algorithm, HMOR (Hierarchical Model Order Reduction), is special in the sense that it performs model reduction for both linear elements and independent sources simultaneously and hence is very suitable for fast timing and signal integrity analysis for tightly coupled RLC interconnects. HMOR is fully compatible with RICE and PRIMA [9] in a way that it can fully utilize RICE to perform moment matching in subcircuits which it decomposes.

Given a circuit with N elements, if the runtime of the general model order reduction method is N^r, where $r \geq 1$, the runtime of HMOR could be $N^r \frac{K}{K^r}$ when the circuit can be properly partitioned into K small modules. The hierarchical nature of HMOR can significantly speed up the turn around time during the circuit design. For a circuit with N elements, HMOR could potentially gain $N/log(N)$ speedup over flat analysis to regenerate the new module for the modified circuit.

For instance, given a N series connected wire segments. We can perform the model order reduction flat or hierarchical, say, in a binary fashion as shown in Figure 1. The run time

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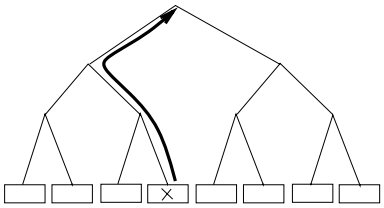

Figure 1: Hierarchical v.s. flat model reduction.

is approximated linear in terms of N for both flat reduction and binary reduction. If one of the wire segments has been changed, the flat method will need to do it from scratch, which causes a runtime penalty to be $O(N)$. On the other hand, the hierarchical way only needs $O(log(N))$ runtime in order to fulfill this task. The benefit of hierarchical over flat is clear in this case.

HMOR, a fusion of circuit decomposition theorems and moment matching algorithms, can be easily embedded into interconnect synthesis algorithms to perform hierarchical timing and multi-attacker noise analysis with great efficiency and accuracy. In particular, we present its application to repeater insertion for multiple-attacker noise analysis for both capacitive and inductive coupling. It can further speed up N times by integrating with hierarchical interconnect synthesis algorithms such as routing, sizing, and repeater insertion [1, 5].

In addition, we extend our algorithm to handle the multi-port circuit analysis. This extension enables HMOR to handle interconnect topology with loops, meshes, or even complicated current return paths. HMOR advances traditional N-port theorems in the following ways. First, it simultaneously reduces the active sources and passive circuit elements to achieve best reduction. Second, it effectively reduces the number of ports by keeping the observation components, internal connections, and independent sources as internal variables. Third, it uses a novel moment computation method to effectively reduce the circuit size. These improvements effectively reduce the runtime and the memory space by keeping the number of ports as small as possible.

The outline of this paper is as follows. In section 2, we present the basic theorems of decomposition, superposition, substitution, and Thevenin equivalent circuit which we will use to develop HMOR. In section 3, we apply those theorems to develop the HMOR method for the RLC routing tree with capacitive and inductive coupling. In section 4, we derive and present the formulae of moment computation for the routing tree. In section 5, we develop an efficient partition algorithm based on the Fiduccia-Mattheyeses algorithm to search good partitions within linear time. In section 6, we extend HMOR to handle general multi-port circuits. In section 7, we discuss the runtime and the accuracy of HMOR.

2. PRELIMINARY

2.1 Fundamental Circuit Theorems

There are several basic circuit theorems we need to develop the hierarchical model order reduction.

- **Superposition Theorem** The response of a circuit due to multiple sources can be calculated by summing the effects of each source separately with all others being turned off.
- **Thevenin Equivalent Circuit Theorem** The equivalent circuit consists of a voltage source which is identical to the open-circuit voltage, in series with an equivalent impedance which can be calculated by turning off all sources in the circuit.
- **Substitution Theorem** Circuits with unique solution can be decomposed into several subcircuits without any change of internal voltages (currents) if we attach independent voltage (current) sources containing the same values of voltages (currents) on the boundary nodes.

Note that Substitution Theorem is valid in both linear and nonlinear circuits as long as the circuit solution is unique. Therefore, we can also apply this theorem to partition nonlinear circuits. We will use STS as an abbreviation for the above three theorems.

2.2 Interconnect Model

In general, a RLC wire segment can be modeled by series connection of lumped RLC models in Figure 2 where R, L and C are resistance, inductance and capacitance per unit length.

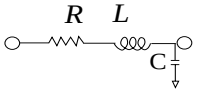

Figure 2: A RLC wire segment.

Consider the case when there is a capacitance coupled noise attacker as shown in Figure 3. We can use a voltage source V_{X_i} to act as the capacitance coupled noise attacker.

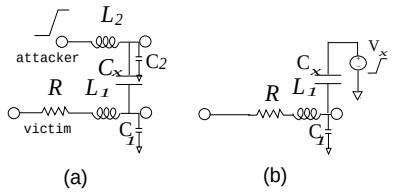

Figure 3: Capacitance coupling noise model.

In the case when there is an inductance coupled noise attacker as shown in Figure 4. We can use the voltage source V_{Y_i} to act as the inductance coupled noise.

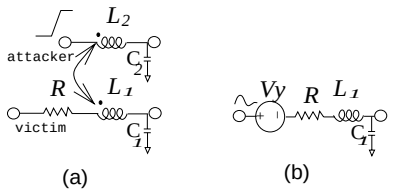

Figure 4: Mutual inductance noise model.

Series connected lumped RLC segments are used to model the transmission line. In Figure 5, we show a K-segment lumped approximation of the transmission line with capacitive and inductive coupled noises. The symbols of R_i, L_i,

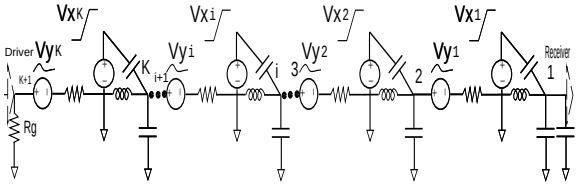

Figure 5: Transmission model with capacitance and inductance coupling noises.

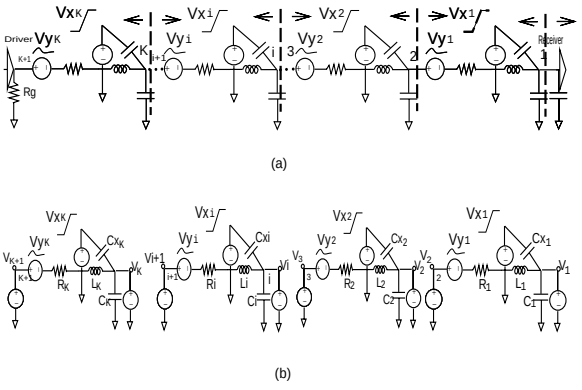

Figure 6: Decomposition.

C_i, V_{X_i} and V_{Y_i} are used to represent the resistance, inductance, capacitance, equivalent capacitance coupling noise and equivalent inductance coupling noise at i-th segment, respectively.

3. ALGORITHM

In this section, we present our hierarchical model order reduction algorithm (HMOR). Given a linear circuit, HMOR first partitions the circuit into several smaller modules. After applying a novel model order reduction to each module, HMOR obtains a reduced circuit in a multi-port Thevenin equivalent circuit form. These modules are then iteratively combined together to complete the reduction procedure. We explain this two-phase procedure as follows:

STEP 1. [**Decomposition**] *HMOR recursively applies a modified FM algorithm to partition the circuit into loosely-connected small modules and then attaches voltage or current sources to the cuts to represent the cuts behavior before partitioning. By Substitution Theorem, the circuit behavior of each module remains the same if all the cut ports have the same voltage waveforms. For example, given a circuit as shown in Figure 6(a), HMOR first partitions Figure 6(a) into several subcircuits as shown in Figure 6(b) and attaches voltage or current source to each port.*

STEP 2. [**Reduction & Combination**] *First, HMOR applies model order reduction to each module and obtains a reduced model in a multi-port Thevenin circuit form. Note that HMOR reduces both linear elements and active independent sources and hence can obtain a better reduction ratio than keeping those active sources as ports. Then, HMOR iteratively combines adjacent modules until the full circuit is glued together. This process is illustrated in Figure 7.*

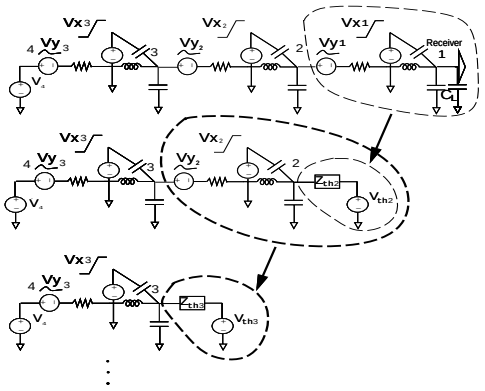

Figure 7: Reduction & Combination.

4. HIERARCHICAL MOMENT MATCHING FOR "NOISY" RLC TREES

When circuits are with special structures such as trees, HMOR applies a very efficient hierarchical computation method to compute the moments of the transfer function, admittance, and Thevenin circuit. These moments of delay and noise transfer functions are updated in an incremental fashion such that it only requires linear runtime and storage for a multi-attacker interconnect environment.

Given a RLC tree which is constructed by coupled lumped wire segments as shown in Figure 8. HMOR computes all the transfer functions from the port nodes to the center node in a bottom-up fashion by Superposition Theorem, as illustrated in Figure 9. Those transfer functions are defined as follows. $H_{i+1,i}$ is the transfer function from node $i+1$ to node i, $H_{x_i,i}$ is the transfer function from capacitive noise source V_{x_i} to node i, and $H_{y_i,i}$ is the transfer function from inductive noise source V_{y_i} to node i. We now show an iterative formula to update the new transfer function of the observation node 1 in this case. For simplicity, we temporarily ignore the inductance noise V_{y_i}.

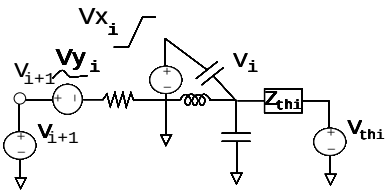

Figure 8: One stage model.

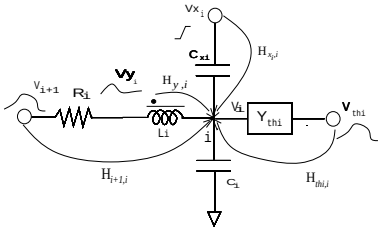

Figure 9: Transfer functions for a wire segment.

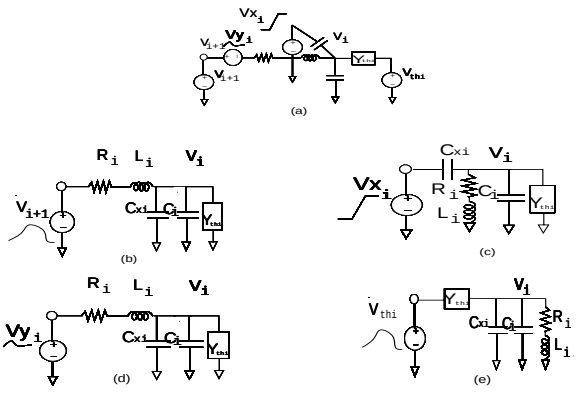

Figure 10: Moment computation by superposition.

From first to second stage

By STS theorems, we have

$$V_1 = V_2 H_{2,1} + V_{x_1} H_{x_1,1} \quad (1)$$
$$V_2 = V_3 H_{3,2} + V_{x_2} H_{x_2,2} + V_{th_1} H_{th_1,2}. \quad (2)$$

Substituting Equation (2) into Equation (1), we get

$$V_1 = V_3 H_{3,1} + V_{th_1} H_{th_1,1} + \sum_{j=1}^{2} V_{x_j} H_{x_j,1}.$$

From i-th to $i+1$-th stage

By STS theorems, we have

$$V_1 = V_{i+1} H_{i+1,1} + \sum_{j=1}^{i-1} V_{th_j} H_{th_j,1} + \sum_{j=1}^{i} V_{x_j} H_{x_j,1} \quad (3)$$
$$V_{i+1} = V_{i+2} H_{i+2,i+1} + V_{th_i} H_{th_i,i+1} + V_{x_{i+1}} H_{x_{i+1},i+1}. \quad (4)$$

Substituting Equation (4) to Equation (3), we get

$$V_1 = V_{i+2} H_{i+2,1} + (\sum_{j=1}^{i} V_{th_j} H_{th_j,1} + \sum_{j=1}^{i+1} V_{x_{j+1}} H_{x_{j+1},1}). \quad (5)$$

Note that the terms in parenthesis can be further reduced into a single term if accumulation effects are preferred. The above equations provide a great option to update transfer functions immediately after reduction. On the other hand, we can also push back the computation till the full circuit has been reduced to get the maximum reduction performance. At the end, the new circuit is compacted into a Thevenin equivalent circuit for the next reduction.

In the rest of this section, we present efficient moment computation methods and formulae for RLC trees with coupling noises coming from capacitors as well as inductors (mutual inductance). The formulae derived in this section can be plugged into the algorithms in [1] to perform noise-aware repeater insertion with even better efficiency. Furthermore, the inductance coupled noises computation formulae can be used to extend [1] to perform inductive noises aware repeater insertion.

Given a RLC routing tree, HMOR first decomposes the tree into lumped RLC segments as shown in Figure 5. HMOR then iteratively combines segments with their adjacent segments. The moment expressions of all transfer functions from ports or voltage sources to connecting nodes, as shown in Figure 9, are defined as $V_i(s) = \sum_{q=0}^{\infty} m_q s^q$, $H_{i+1,i}(s) = \sum_{q=0}^{\infty} m_q^V s^q$, $H_{x_i,i}(s) = \sum_{q=0}^{\infty} m_q^X s^q$, $H_{y_i,i}(s) = \sum_{q=0}^{\infty} m_q^Y s^q$, $H_{th_i,i}(s) = \sum_{q=0}^{\infty} m_q^{TH} s^q$, and $Y_{th_i}(s) = \sum_{q=0}^{\infty} y_q^i s^q$.

The following variables are introduced to assist the transfer function computation: $Y_q^V = \sum_{n=0}^{q} m_n^V y_{q+1-n}^i$, $Y_q^X = \sum_{n=0}^{q} m_n^X y_{q+1-n}^i$, $Y_q^Y = \sum_{n=0}^{q} m_n^Y y_{q+1-n}^i$, $Y_q^{TH} = \sum_{n=0}^{q} m_n^{TH_i} y_{q+1-n}^i$. These variables represent the superimposed currents flowing through the Y_{th_i} by activating one exciting source at a time.

The following Lemma derives the nodal voltage $V_i(s)$ at node i in terms of the accumulated effects of exciting sources.

LEMMA 1. *Let $V_i(s) = \sum_{q=0}^{\infty} m_q s^q$, we have*

$$V_i = V_{i+1} H_{i+1,i} + V_{x_i} H_{x_i,i} + V_{y_i} H_{y_i,i} + V_{Th_i} H_{th_i,i}$$
$$m_q = \sum_{n=0}^{q} (m_{q-n}^V m_n^v + m_{q-n}^X m_n^x + m_{q-n}^Y m_n^y + m_{q-n}^{TH} m_n^{th_i})$$

where m_n^v, m_n^x, m_n^y and $m_n^{th_i}$ are the moments of voltage sources V_{i+1}, V_{x_i}, V_{y_i}, and V_{th_i} respectively.

The following lemmas present the transfer functions from each source to the connecting node i by the Superposition Theorem as illustrated in Figure 10. We use several basic moment computation techniques [9] to derive these formulae. They are also used in the derivations of the rest lemmas. All proofs are omitted for brevity.

LEMMA 2. *Let $H_{i+1,i}(s) = \sum_{q=0}^{\infty} m_q^V s^q$, we have*

$$m_q^V = \begin{cases} 1 & \text{if } q = 0 \\ -R_i(y_1^i + C_i + C_{x_i}) & \text{if } q = 1 \\ -(C_i + C_{x_i})(R_i m_{q-1}^V + L_i m_{q-2}^V) & \\ -R_i Y_{q-1}^V - L_i Y_{q-2}^V & \text{if } q > 1 \end{cases}$$

LEMMA 3. *Let $H_{x_i,i}(s) = \sum_{q=0}^{\infty} m_q^X s^q$, we have*

$$m_q^X = \begin{cases} 0 & \text{if } q = 0 \\ R_i C_{x_i} & \text{if } q = 1 \\ -(C_i + C_{x_i})(R_i m_{q-1}^X + L_i m_{q-2}^X) & \\ -R_i Y_{q-1}^X - L_i Y_{q-2}^X + L_i C_x & \text{if } q = 2 \\ -(C_i + C_{x_i})(R_i m_{q-1}^X + L_i m_{q-2}^X) & \\ -R_i Y_{q-1}^X - L_i Y_{q-2}^X & \text{if } q > 2 \end{cases}$$

LEMMA 4. *Let $H_{y_i,i}(s) = \sum_{q=0}^{\infty} m_q^Y s^q$, we have*

$$m_q^Y = \begin{cases} -1 & \text{if } q = 0 \\ R_i(y_1^i + C_i + C_{x_i}) & \text{if } q = 1 \\ -(C_i + C_{x_i})(R_i m_{q-1}^Y + L_i m_{q-2}^Y) & \\ -R_i Y_{q-1}^Y - L_i Y_{q-2}^Y & \text{if } q > 1 \end{cases}$$

LEMMA 5. *Let $H_{th_i,i}(s) = \sum_{q=0}^{\infty} m_q^{TH} s^q$, we have*

$$m_q^{TH} = \begin{cases} 0 & \text{if } q = 0 \\ R_i y_1^i & \text{if } q = 1 \\ -(C_i + C_{x_i})(R_i m_{q-1}^{TH} + L_i m_{q-2}^{TH}) & \\ -R_i Y_{q-1}^{TH} - L_i Y_{q-2}^{TH} + R_i y_q^i + L_i y_{q-1}^i & \text{if } q > 1 \end{cases}$$

The following Lemma derives the new Thevenin Equivalent circuit for the combined circuit.

LEMMA 6. *Let the Thevenin equivalent voltage and admittance of the combined circuit be $V_{th_i} = \sum_{q=0}^{\infty} m_q^{th_i} s^q$,*

and $Y_{th_i} = \sum_{q=0}^{\infty} y_q^{th_i} s^q$. $m_q^{th_0} = y_q^{th_0} = 0 \ \ \forall q$. *With following auxiliary variables*

$$m_q^{x'} = \begin{cases} \frac{C_{x_i}}{C_i + C_{x_i} + y_1^i}, & \text{if } q = 0 \\ -\frac{\sum_{n=0}^{q-1} m_n^x \, y_{q-n+1}^i}{C_i + C_{x_i} + y_1^i} & \text{if } q > 0 \end{cases}$$

$$m_q^{th'} = \begin{cases} \frac{y_1^i}{C_i + C_{x_i} + y_1^i} & \text{if } q = 0 \\ \frac{y_{q+1}^i - \sum_{n=0}^{q-1} m_n^{th'} \, y_{q-n+1}^i}{C_i + C_{x_i} + y_1^i} & \text{if } q > 0, \end{cases}$$

we have

$$m_q^{th_{i+1}} = m_q^y + \sum_{n=0}^{q} (m_n^{x'} \, m_{q-n}^x + m_n^{th'} \, m_{q-n}^{th_i}) \quad \forall q$$

$$y_q^{i+1} = \begin{cases} 0 & \text{if } q = 0 \\ (C_i + C_{x_i}) m_{q-1}^V + \sum_{n=0}^{q-1} m_n^V \, y_{q-n}^i & \text{if } q > 0 \end{cases}$$

The following lemma computes the new Thevenin equivalent circuit (V_{th_3}, Y_{th_3}) when two Thevenin equivalent circuits (V_{th_1}, Y_{th_1}) and (V_{th_2}, Y_{th_2}) are parallel connected. This condition happens when two branches of tree edges join together.

LEMMA 7. *Parallel Connection. Let* $V_{th_1}(s) = \sum_{q=0}^{\infty} v_q^{TH_1} s^q$, $Y_{th_1}(s) = \sum_{q=0}^{\infty} y_q^{TH_1} s^q$, $V_{th_2}(s) = \sum_{q=0}^{\infty} v_q^{TH_2} s^q$, $Y_{th_2}(s) = \sum_{q=0}^{\infty} y_q^{TH_2} s^q$, $V_{th_3}(s) = \sum_{q=0}^{\infty} v_q^{TH_3} s^q$, *and* $Y_{th_3}(s) = \sum_{q=0}^{\infty} y_q^{TH_3} s^q$, *we have*

$$y_q^{TH_3} = y_q^{TH_1} + y_q^{TH_2} \quad \forall q > 0$$

$$m_q^{TH_3} = \begin{cases} \frac{m_0^{TH_1} y_1^{TH_1} + m_0^{TH_2} y_1^{TH_2}}{y_1^{TH_1} + y_1^{TH_2}} & \text{if } q = 0 \\ (m_q^{TH_1} y_1^{TH_1} + m_q^{TH_2} y_1^{TH_2} \\ + \sum_{n=0}^{q-1} ((m_n^{TH_1} - m_n^{TH_3}) y_{q-n+1}^{TH_1} \\ + (m_n^{TH_2} - m_n^{TH_3}) y_{q-n+1}^{TH_2})) \\ / (y_1^{TH_1} + y_1^{TH_2}) & \text{if } q > 0 \end{cases}$$

5. PARTITIONING ALGORITHM

The runtime of HMOR heavily depends on the quality of partition. A good partition algorithm can significantly reduce the cut sizes which leads to a big performance gain. For this reason, we develop an efficient partition algorithm based on the Fiduccia-Mattheyeses algorithm to search good partitions with linear time. Let P_i, M_i be the number of ports, and size of module i. We define the objective function as $(P_0 + C)M_0^2 + (P_1 + C)M_1^2$, where C is the cut size to estimate the runtime of performing model reduction for each module. This algorithm iteratively selects the most beneficial element to change set while keeps the ratio between two modules being a constant value. We record the net change of the objective function during the moving process and backtrack the best moving sequence which has the minimum value of the objective function at the end. To improve the performance of F-M algorithm, we maintain a bucket list $Bucket_{d_0^j, d_1^j}$ for the elements in partition 0 and 1 to record the order of the moving benefit for each module. This special data structure allows us to search the next moving candidate in constant time. This algorithm is summarized at Table 1. We recursively apply this algorithm to obtain smaller partitions for each new module until the module size is manageable.

Input: G=(V,E), **Output:** bi-partitions $S[0], S[1]$;
Cost: $cost = (P_0 + C)M_0^2 + (P_1 + C)M_1^2$.
P_k, M_k:#Ports, #Cells in $S[k], k = 0, 1$; C: cut size;
$Bucket^k_{d_0,d_1}$:cells with $\delta(P_0 + C) = d_0$,$\delta(P_1 + C) = d_1$ in S[k]
Begin
Step 1: For $\forall$ cell $j \in S[k], k = 0, 1$ $-2 \le d_0, d_1 \le 2$
Compute $d_0^j = \delta(P_0 + C)$ and $d_1^j = \delta(P_1 + C)$
$Bucket^k_{d_0^j, d_1^j} = Bucket^k_{d_0^j, d_1^j} \cup \{$ cell $j\}$;
Step 2: $i = 1$, for $\forall d_0$,choose free cell $c_i^{d_0}$ with min $d_1(c_i^{d_0})$
Calculate $cost'(k, d_0) = (P_0 + C + d_0)M_0^2 + (P_1 + C + d_1)M_1^2$
Choose $cost_i = min^{k=0,1}_{-2 \le d_0 \le 2}(cost'(k, d_0))$on base cell c_i;
If there is no base cell **then goto** Step 5;
Step 3: Lock cell i, $Bucket^k_{d_0,d_1} = Bucket^k_{d_0,d_1} \backslash c_i$;
$\forall$ cell $j \in S[k]$, **If** $e_{i,j} \in E$, **then**
Update d_0^j and d_1^j;
Move cell j to new corresponding $Bucket^k_{d_0^j, d_1^j}$;
Step 4: **If** free cell $\neq \phi$ **Then** $i = i + 1$; select next base cell;
If $c_i \neq \phi$ then **goto** Step 3;
Step 5: Select best sequence of moves $c_1, c_2, ..., c_n$ $(1 \le n \le i)$, such that $cost_{min} = cost_n$ is minimum;
If $cost_{min} \ge cost_{min}'$ **Then** exit;
Step 6: Make all of the n moves permanent; Free all cells;
$cost_{min}' = cost_{min}$; **goto** Step 1;
End

Table 1: Partitioning algorithm for HMOR

6. MULTI-PORT REDUCTION

In this section, we present our model order reduction algorithm for the multi-port circuit. Given a network, we first partition the network into K multi-ports N_i, $i = 1 \cdots K$ as shown in Figure 11(a). We classify the ports of N_k into four types: external ports $\mathbf{P}_E^k$, connected external ports $\mathbf{P}_I^k$, independent voltage sources $\mathbf{P}_X^k$, and internal observation variables $\mathbf{P}_O^k$. The difference between $\mathbf{P}_I^k$ and $\mathbf{P}_E^k$ is in the combination sequences. $\mathbf{P}_I^k$ are the ports of N_k which have already been connected during the combination step, and $\mathbf{P}_E^k$ are the ports of N_k which have not yet been connected during the combination step. The voltages associated with $\mathbf{P}_E^k$, $\mathbf{P}_I^k$, $\mathbf{P}_X^k$, and $\mathbf{P}_O^k$ are $\mathbf{V}_E^k$, $\mathbf{V}_I^k$, $\mathbf{V}_X^k$, and $\mathbf{V}_O^k$, respectively. The reason for this classification is to reduce the number of ports during combination since those ports are going to be connected in the future and hence can be treated as connected external ports. We define the multi-port Thevenin equivalent circuit of the combined circuit as $(\mathbf{V}_{th}^k, \mathbf{Y}_{th}^k)$.
By STS, we have

$$\mathbf{V}_O^k = \mathbf{H}_{E,O}^k \mathbf{V}_E^k + \mathbf{H}_{X,O}^k \mathbf{V}_X^k + \mathbf{H}_{th,O}^{k-1} \mathbf{V}_{th}^{k-1} \qquad (6)$$

where $\mathbf{H}_{E,O}^k$, $\mathbf{H}_{X,O}^k$, and $\mathbf{H}_{th,O}^{k-1}$ are defined as the matrices of transfer functions from $\mathbf{V}_E^k$, $\mathbf{V}_X^k$, and $\mathbf{V}_{th}^{k-1}$ to $\mathbf{V}_O^k$, respectively.

The above equation provides an alternative way to efficiently update transfer functions from all current external ports to observation variables immediately after one reduction. The evaluation can also be pushed back to the final to reduce the reduction time.

Multi-port Thevenin Equivalent Circuit HMOR uses the following method to generate the Multi-port Thevenin equivalent circuit. Let I_E^k be the attached independent current sources at P_E^k, we have

$$\mathbf{V}_E^k = \mathbf{Z}_E^k \mathbf{I}_E^k + \mathbf{H}_{X,E}^k \mathbf{V}_X^k + \mathbf{H}_{th,E}^{k-1} \mathbf{V}_{th}^{k-1}. \qquad (7)$$

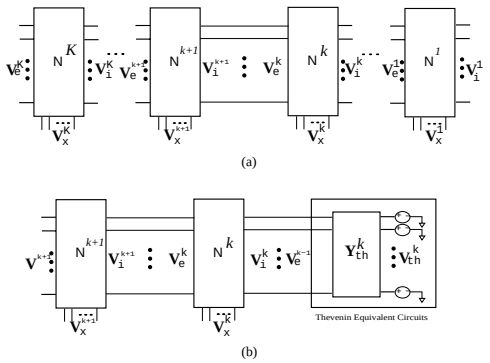

Figure 11: Model for multiple ports.

Let $\mathbf{V}_{th}^k = \mathbf{H}_{X,E}^k \mathbf{V}_X^k + \mathbf{H}_{th,E}^{k-1} \mathbf{V}_{th}^{k-1}$ where $\mathbf{H}_{X,E}^k$, and $\mathbf{H}_{th,E}^{k-1}$ are defined as the matrices of transfer functions from $\mathbf{V}_X^k$, and $\mathbf{V}_{th}^{k-1}$ to $\mathbf{V}_E^k$, respectively. The new Thevenin equivalent circuit will be ($\mathbf{V}_{th}^k$, $\mathbf{Z}_E^k$). In this way, HMOR avoids explicitly generating ports for exciting sources such as $\mathbf{V}_X^k$, and $\mathbf{V}_{th}^{k-1}$ which is a great saving in terms of runtime and memory space.

Remark for Passivity Reduction: HMOR can be extended to perform hierarchical passive reduction when passive reduction algorithms such as PRIMA are utilized. For each partitioned block with $sCv'(t) = -Gv(t) + Bu$, where v is the voltage and current vectors, G and C are the respective conductance matrix and susceptance matrix, B is the excitation configuration vector, and u is the excitation source vector, PRIMA can generate a new reduced system $sC'p'(t) = -G'p(t) + B'u$, where $p(t)$ is the port voltage and current vector, C' and G' are the respective reduced susceptance and conductance matrices, B' is the new excitation configuration vector. These reduced blocks can be iteratively combined together to form the reduced model for the whole circuit. Since any linear combination of passive circuits is still passive [2], the integrated reduced circuit still remains passive.

7. EXPERIMENTAL RESULTS

We implement and test HMOR on several industrial circuits. Table 2 shows the accuracy between HMOR and RICE on clock tree circuits [12]. It is easy to see that all the moments are exactly identical. Table 3 shows the experimental results of HMOR on several industrial examples from the ISCAS'85 benchmarks [8]. It shows that our partition algorithm is able to reduce the reduction runtime by over 50%. It also shows that our partition algorithm is very efficient. For a circuit with around 1,000 elements, our algorithm takes only 0.04 second to obtain a decent solution.

	Ckt#1	Ckt#2	Ckt#3	Ckt#4	Ckt#5
# element	38	928	729	1064	1498
# port	6	73	86	73	58
Cost	7.94e3	6.29e7	4.57e7	8.26e7	1.30e8
Cut Size	3	44	26	40	64
P_0	3	9	23	9	17
P_1	2	32	47	32	21
Newcost	3.97e3	2.73e7	1.59e7	3.32e7	0.99e8
Speedup	2.18	2.30	2.93	2.49	1.31
Runtime	0.00*s*	0.02*s*	0.05*s*	0.04*s*	0.09*s*

Table 3: Runtime deduction by partitioning

8. REFERENCES

[1] C. P. Chen, and N. Menezes, *Noise-aware Repeater Insertion and Wire Sizing for On-chip Interconnect Using Hierarchical Moment-Matching*, 36th DAC, pp. 502-506, June. 1999.

[2] L. O. Chua, C. Desoer and E. Kuh, *Linear and Nonlinear Circuits*, McGRAW-HILL Book Co., 1987.

[3] J. Cong, C. K. Koh, *Interconnect Layout Optimization Under Higher-Order RLC Model*, IEEE/ACM International Conference on Computer-Aided Design, pp. 713-720, CA, Nov. 1997.

[4] J. Lillis, C. K. Cheng, and T. T. Lin, *Optimal and efficient buffer insertion and wire sizing*, Prof. Custon Integrated Circuits Conference, pp. 259-262, May. 1995.

[5] C. J. Alpert, A. Devgan, and S. T. Quay, *Buffer insertion for noise and delay optimization*, Proceedings of the 35th Design Automation Conference, pp. 362-367, June. 1998.

[6] P. Feldman and R. W. Freund, *Efficient linear circuit analysis by Pade approximation via the Lanczos process*, IEEE Trans. Computer-Aided Design, vol. 14, no. 5, pp 639-649, May 1995.

[7] Q. J. Yu, E. S. Kuh, *Exact moment model of transmission lines and application to interconnect delay estimation*, IEEE Trans. on VLSI Systems. vol.3, pp. 311-322, June 1995.

[8] International Symposium on Circuit And System, 1985.

[9] L. T. Pillage, R. A. Rohrer, C. Visweswariah, *Electronic Circuit and System Simulation Methods*, McGRAW-HILL Book Co., 1994.

[10] R. S. Tasy, *Exact zero skew*, IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, 1993.

[11] A. Odabasioglu, M. Celik, and L. T. Pillage, *PRIMA: Passive Reduced-order Interconnect Macromodeling Algorithm*, ICCAD, pp. 58-65, 1997.

	Circuit 1 (532*)		Circuit 2 (1195)		Circuit 3 (1723)		Circuit 4 (3805)		Circuit 5 (6200)	
	HMOR	RICE	HMOR	RICE	HMOR	RICE	HMOR	RICE	HMOR	RICE
m[0]	1.000	1.000	1.000	1.000	1.000	1.000	1.000	1.000	1.000	1.000
m[1]	-1.100e-01	-1.100e-01	-2.303e-01	-2.303e-01	-2.791e-01	-2.791e-01	-5.950e-01	-5.950e-01	-1.001e00	-1.001e00
m[2]	1.014e-02	1.014e-02	4.737e-02	4.737e-02	7.048e-02	7.048e-02	3.227e-01	3.227e-01	9.244e-01	9.244e-01
m[3]	-9.022e-04	-9.022e-04	-9.644e-03	-9.644e-03	-1.768e-02	-1.768e-02	-1.734e-01	-1.734e-01	-8.422e-01	-8.422e-01
m[4]	7.930e-05	7.930e-05	1.962e-03	1.962e-03	4.437e-03	4.437e-03	9.295e-02	9.295e-02	7.630e-01	7.630e-01
m[5]	-6.929e-06	-6.929e-06	-3.990e-04	-3.990e-04	-1.114e-03	-1.114e-03	-4.979e-02	-4.979e-02	-6.896e-01	-6.896e-01

Table 2: Moments comparison between HMOR and RICE on clock trees.

*the number of components in the circuit.