2-Level LFSR Scheme with Asynchronous Test Pattern Transfer for Low Cost and High Efficiency Built-In-Self-Test

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Abstract

This paper describes a new test pattern generator to increase fault coverage and a test pattern transferring method to reduce test time without large hardware overhead in the BIST structure. The new pattern generator uses a 2-level LFSR scheme in which inputs are varied and controlled by the counter output. An asynchronous internal clock generated by an internal ring-oscillator is used for fast test pattern transfer into the scan chain. The new 2-level LFSR scheme is verified by the HITEC fault simulator.

1. INTRODUCTION

With Ultra-Deep Sub-Micron (UDSM) technology, millions of gates can be integrated to build a System-On-a-Chip (SOC). Since SOC is very complicated, not only does chip design takes longer but chip testing is also a big issue. Conventional test methods using external Automatic Test Equipment (ATE) have drawbacks such as the high cost for the capacity to store huge test patterns and their corresponding test programs and unscalability of the testing frequency. Therefore, Built-In-Self-Test (BIST) has been a promising methodology for VLSI circuits including embedded core-based systems due to its simplicity, effectiveness and flexibility. In BIST, the Linear-Feedback-Shift-Register (LFSR) is widely used to generate test patterns due to its low area overhead and scalability. Since pseudo-random test patterns generated by the LFSR have low fault coverage due to their linear dependency and auto-correlation, much research has been done to increase the probability of generating test patterns that detect Random-Pattern-Resistant (RPR) faults. Redesign methods of Chip-Under-Test (CUT) [1], [2], weighted pseudo-random pattern generation techniques [3], [4], re-seeding techniques [5], bit altering technique [6], and bit flipping technique [7] can be classified as pseudo-random test pattern generation techniques for the test-per-scan scheme [8] that requires less hardware overhead than the test-per-cycle scheme [9].

In this paper, we propose a low cost 2-level LFSR scheme to generate pseudo-random test patterns to improve fault coverage and an asynchronous test pattern transfer (ATPT) scheme to reduce the test time for the test-per-scan scheme while minimizing hardware overhead.

This paper is organized as follows. In Section 2, previous approaches are reviewed. In Section 3, the concept and operation of the proposed scheme are discussed. In Section 4, simulation results are shown, followed by our conclusions in Section 5.

2. PREVIOUS APPROACHES

In redesign methods of the CUT [1], [2], test points are inserted into the chip and the CUT is redesigned considering testability. Extra levels of logic need to be added, leading to a potential degradation in system performance.

In weighted pseudo-random pattern generation techniques [3], [4], logic is added to change the probability of each bit in a way that favors selection of patterns that can detect random-pattern-resistance faults. Weighted logic can be inserted at the input of the scan chain and in the individual scan cells. Since a weight set needs to be stored and control logic is required, hardware overhead can be high.

In re-seeding techniques [5], seed patterns to generate the following input patterns by the LFSR can be replaced according to precomputation results, i.e. fault simulation results, as shown in Fig. 1. Different seed patterns are stored and selected after decoding patterns from the LFSR. As a result, the computed deterministic seeds can be loaded into the LFSR. Again, large hardware overhead is a problem.

The test patterns transferred into the scan chain can be modified according to the bit altering [6] and bit flipping techniques [7]. Figure 2 shows the block diagram of the bit altering scheme. After precomputation, test tubes for faults undetected by the original LFSR are found and manipulated to generate the input patterns for those undetected faults. When a test pattern is generated by LFSR, bit-fixing generation logic changes the bit. Besides the hardware overhead, the algorithm to fix the bit depends on the CUT and cannot
3. PROPOSED 2-LEVEL LFSR AND ASYNCHRONOUS TEST PATTERN TRANSFER SCHEME

Fig. 3 shows block diagrams of the conventional scheme and the new 2-level LFSR scheme. In the conventional scheme, two inputs originated from seed bits generate a new output using an XOR gate and the new bit is used as a new entry of the seed bits for the next operation as shown in Fig. 3(a). A counter is used to control the bit transfer to the scan chain. Due to its high linear dependency and auto-correlation, the conventional LFSR quickly gets saturated in generating the test patterns to detect the RPR faults.

In the new 2-level LFSR scheme, the XOR gate inputs from seed bits are changed according to the output of the counter after a certain number of test patterns are generated by the conventional LFSR as shown in Fig. 3(b). After transferring test patterns into the scan chain, an extra bit is increased by one. After some patterns are generated, e.g., 1000, different paths for the XOR inputs for the next input pattern generation are selected. During the logic evaluation cycle, the outputs of the counter are decoded and a new input path is pre-selected. The hardware overhead consists only of the extra counter bits to determine the initial amount of test pattern generation and to select different input paths, decoders and transmission gates, which is much less than the previous techniques requiring complicated logic gates and memories.

Another issue in scan-based BIST is the test time. The total test cycles in scan methodology is expressed as

\[ T_{cycle_{conv}} = \frac{(Num_{of\ scanbit} + 1) \times (Num_{of\ LFSR\ patterns} + Num_{of\ RPR\ patterns})}{f} \]  

where \( T_{cycle_{conv}} \) is the test time for the conventional case, \( Num_{of\ scanbit} \) is the number of latches in the scan chain inside the logic under test, \( Num_{of\ LFSR\ patterns} \) is the total number of test patterns generated by the LFSR and \( Num_{of\ RPR\ patterns} \) is the total number of extra test patterns to detect the RPR faults and \( f \) is the test frequency.

When the same frequency is used for the test pattern transfer into the scan chain and the logic test, most of time is spent on transferring the test patterns. Power consumption due to the clock is significant. Usually, the clock generator is placed in the chip to minimize the clock skew and let the clock signal run freely all the time. The capacitive discharge of the clock line from the clock generator to the logic block under test contributes to the total power consumption even with the use of a clock gating scheme to reduce unnecessary power consumption. Increasing the test frequency with a central clock generator to reduce the test time is difficult due to its heavy capacitive loading.

Therefore, we propose an asynchronous test pattern transfer (ATPT) scheme to reduce the test time and power consumption as shown Fig. 4(a). In the ATPT scheme, instead of using the same global clock for both test pattern transfer and the logic test as shown Fig. 4(b), the test patterns are transferred into the scan chain using the faster local clock generated by a ring-oscillator and the logic test is done using the global clock after synchronization as shown Fig. 4(c). As a result, the test time can be reduced as
4. EXPERIMENT RESULTS

Fault simulation is done using HITEC [10]. Initial values of the LFSR are set to be the same as ones for the full-scan simulation by HITEC. Figure 5 shows fault coverage for the S123B benchmark circuit given by the conventional and the new 2-level LFSR for different LFSR sizes. Fault coverage for small LFSR sizes (5 and 10) is relatively low and gets saturated when LFSR sizes are larger than 15.

Figure 6 shows fault coverage for different numbers of test patterns. The LFSR size is set to be 15. After the conventional LFSR generate invalid test patterns, the new scheme can generate test patterns to detect faults.

Fault coverage for different benchmark circuits is shown in Fig. 7. For all cases, fault coverage is significantly improved. Therefore the 2-level LFSR scheme is shown to be effective for scan-based BIST.

The test time reduction by the ATPT scheme is shown in Fig. 8 for different factors representing the ring-oscillator frequency, which is used only to transfer test patterns into the scan chain. The overall system is assumed as in [11], where test patterns to detect the RPR faults are provided by external equipment. Two additional cycles are assumed for synchronization before the logic test.

If more test patterns are generated by the LFSR, the ATPT is more effective since the time to transfer test patterns can be reduced a lot. The test time can be reduced almost by the factor of the increased internal oscillator frequency.

5. CONCLUSIONS

A new 2-level LFSR using extra counter bits and decoders and an synchronous test pattern transfer scheme by the internal clock are developed for low cost and high efficiency BIST. The new LFSR scheme improves fault coverage significantly without large hardware overhead such as memories for re-seeding and logic for pattern fixing and altering. Test time can be reduced by the new ATPT scheme almost linearly with internal oscillator frequency.

6. ACKNOWLEDGMENTS

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7. REFERENCES


Figure 6: Fault coverage for different numbers of test patterns (benchmark circuit: $\text{S1238}$)


Figure 7: Fault coverage for different benchmark circuits

Figure 8: Test time reduction by the ATPT scheme for different factors