Panel:

Is Marriage in the Cards for Programmable Logic, Microprocessors and ASICs?

Moderator: Sinan Kaptanoglu, Adaptive Silicon

Panelists: John East, Actel,
Tim Garverick, Adaptive Silicon,
Scott Hauck, University of Washington,
David Papworth, Intel,
Danesh Tavana, Triscend,
Steve Trimberger, Xilinx,
Ronnie Vasishta, LSI Logic.

The panelists focus first on the possibility, likelihood or inevitability of combinations of programmable logic, microprocessors and ASICs in a single chip and then address the following issues:

- Will they be as general as possible or application specific?
- Will all three types of logic be involved or perhaps only two?
- How much of the die area should be allocated to programmable logic?
- How will the CAD tools cope with the speed mismatch between the programmable logic and fixed logic on the same chip?
- How will the designs be partitioned into programmable and fixed parts; will it be done by humans or by CAD tools?

These future predictions may depend on the system design size. Are the answers for 500K gate system designs different from those for 5,000K gate system designs? What will happen when 50,000K gate system designs become common place in 5 years?