A Pipelined ADC Macro Design for Multiple Applications

Kuniyuki Tani, Norihiro Nikai, Atsushi Wada, Tetsuro Sawai

Microelectronics Research Center
SANYO Electric Co., Ltd.
180, Ohmori, Anpachi-Cho, Anpachi-Gun, Gifu, Japan, 503-0195
Tel : +81-584-64-5218 Fax : +81-584-65-5214
e-mail : {tani,nikai,wada,sawai}@ul.rd.sanyo.co.jp

Abstract - We present a new design methodology for high-speed Analog-to-Digital Converter (ADC) macros based on our original pipelined 10-bit ADC. With library re-use methodology and performance driven optimization techniques, we have been able to both shorten the design period and to meet application specifications for items such as speed and power consumption.

Using this method, we have developed ADC macros from 10-bit to 8-bit and 6-bit. They can be embedded into system LSIs for communication and multimedia applications.

I. INTRODUCTION

As video and communication systems markets continue to grow every day, high-speed ADC macros in a standard CMOS process are in increasing demand for system LSIs for many applications. However, to maximize profits, system LSIs must be designed quickly. ADC macros for system LSIs are also required to operate at high speeds with low power consumption. However, it is difficult to design these within a short design period. Therefore, it is essential to develop ADC design methodologies that shorten the design period with regard to generators used in memory designs.

Looking at high speed-ADC designs so far, several architectures have been developed. For example, the flash type is useful for high speed operation[1]. However, it is only applicable for less than 8-bit resolution. On the other hand, the multi-stage pipelined type is useful for 8-bit resolution and above[2,4,5], while it is difficult to achieve high-speed operation. For these reasons, architecture suitability varies for each application. This is one of the main reasons why it is difficult to design ADCs in the same way as generators with a memory design.

In order to overcome this problem, we focused on our multi-stage pipelined ADC that has a wider range of applications compared to other ADC methods. Based on our 10-bit pipelined ADC, we have developed new design methodology, which shorten design period of fast ADC macros with various specifications such as resolution, speed and power.

II. PROPOSED DESIGN FLOW FOR PIPELINED ADC MACROS

The new design flow that we developed for pipelined ADC macros is shown in Fig. 1.

A. Architecture Design

At first, the number of pipeline stage and capacitance value of stage amplifier in each stage is decided automatically according to overall resolution.

Fig. 1: Proposed Design Flow

Fig. 2-a): Base architecture of 4-stage pipelined ADC(10-bit)
B. Layout Design

Next, we do physical design. It is easy to obtain layout data like using layout generator by removing stages from the base ADC.

C. Optimization of Analog Block Libraries

Thirdly, we select suitable amplifier from in the prepared library and adjust bias voltage in order to realize minimum power consumption for sampling frequency by the method as described in section IV.

D. Overall Simulation

Lastly, we execute transient simulation of opamp to extract parameter of analog-HDL. Next, we extract gain error of an opamp. And we simulate linearity of ADC with analog-HDL. And, if there is no problem, we can finish ADC design.

The detail of this design methodology will be mentioned in the following sections.

III. LIBRARY RE-USE METHODOLOGY OF PIPELINED ADC

A. Base Architecture

In order to shorten design period for ADC design, we introduced library-reuse techniques, which enable us to re-use the comparators, opamps and so on of previous designs. Adopting this library re-use methodology, it is key issue to decide a base architecture, which has flexibility and can be applicable for several applications including 6-bit and 12-bit. Examining conventional architectures, we found pipelined ADC is an appropriate candidate.

We had developed 10-bit pipelined ADCs suitable for embedded design in a standard CMOS process [3,4], one notes that the first stage consists of a 4-bit ADC and DAC, followed by 2-bit sub AD/DA series. Also, in order to improve interstage bandwidth, we developed a 2-step interstage-amplifying technique and succeeded in developing up to 50 MHz in 0.35 um standard CMOS [4]. This technique is also useful for low power pipelined ADC design.

On the other hand, this architecture with following stages of 2-bit sub AD/DA has good flexibility for many applications. By removing some stages, it can easily cover from 6-bit ADC to 10-bit ADC. For this purpose, we designed a layout of the stage including 2-bits sub AD/DA block and stage amplifier as a module shown in Fig. 3. This enables us to re-use layout data. Therefore, we can quickly generate various ADC layout data according to the required resolution.

B. Design Target of New Methodology

Fig. 4 shows the target ADC performance we expect to achieve by this re-use design technique.

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In Fig. 4, the original 10-bit/50 MHz ADC is plotted by a double circle. As described before, it is easy to realize ADCs in gray region by removing the stage of 2-bit sub AD/DA block from the original one.

For example, the 6-bit/30 MHz ADC plotted by a circle can be achieved by removing two stages from the original 10-bit/50 MHz ADC. However, each analog block is optimized for 10-bit resolution and 50 MHz sampling frequency. So, analog blocks should consume a larger current than required by that of 6-bit/30 MHz ADC. As a result, this method enables us to shorten design period at the sacrifice of performance. Therefore, it is important to develop performance-driven (low-power) optimization techniques in order to realize both short design period and low power consumption.
IV. PERFORMANCE DRIVEN OPTIMIZATION TECHNOLOGY OF ANALOG BLOCKS

A. Dissipation Current Analysis

Table 1 shows the dissipation current of analog and digital blocks in the base 10-bit/50 MHz ADC.

<table>
<thead>
<tr>
<th></th>
<th>Opamps</th>
<th>Bias</th>
<th>Comp</th>
<th>Digital</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>10b/50MHz</td>
<td>24mA</td>
<td>2mA</td>
<td>5mA</td>
<td>9mA</td>
<td>40mA</td>
</tr>
</tbody>
</table>

From Table 1, it is clear that the dissipation current of opamps is much larger than that of the other blocks. Therefore, current optimization of opamps is an effective method for lowering dissipation current of overall ADC.

B. Optimization of Analog Blocks

1) Design Requirement of Opamp

In this part, we describe how to achieve the required accuracy of opamps.

Linearity error is one of the most important characteristics of ADCs. Gain error of a stage amplifier effects linearity error. Linearity error (LE) of our pipelined ADC is represented in Eq. 1.

\[
LE = [\text{LSB}_1 + (\text{LSB}_2/4) + (\text{LSB}_3/16) + \ldots] \times \text{GE}
\]

Eq. 1: Linearity Error

In Eq. 1, \( \text{LSB}_i \) is LSB of \( i \)-th subAD and GE is gain error of a stage amplifier. From Eq. 1, we can obtain required accuracy of a stage amplifier of each stage. Therefore, acceptable value of GE can be determined by overall resolution. It is clear that gain of first stage amplifier is more important.

On the other hand, because we applied 2-step amplifying, permissible gain error (GE2) of one amplifier can be obtained from Eq. 2

\[
(1-\text{GE}) = (1-\text{GE2}) \times (1-\text{GE2}) \\
\text{GE2} = 1 - (1-\text{GE})^{0.5}
\]

Eq. 2: Gain error of stage amplifier

We use switched capacitor (SC) opamps as stage amplifiers. A block diagram of the SC opamp is shown in Fig. 5. In Fig. 5, \( C_p \) represents parasitic capacitance of input node of the amplifier.

Folded cascade amplifier is used as the amplifier in the SC amplifier.

We must consider characteristics of SC amplifier to obtain the required specification from permissible gain error (GE2) of stage amplifier. Closed Loop Gain of SC amplifier in Fig. 4 is given by Eq. 3.

\[
\text{GAIN} = \frac{2C}{(3C+\text{C}_p)/\text{G}+\text{C}}
\]

Eq. 3: Closed Loop Gain

G is open loop gain of the amplifier. The capacitor value of \( C \), shown in Fig. 5, is determined by Eq. 3 and GE2. Now, open loop gain of the base amplifier is 55dB in the worst case and \( C_p \) is 120fF. So, minimum value of \( C \) for 10-bit, 8-bit and 6-bit accuracy obtained from Eq. 1-3 are 307fF, 11fF and 2fF, respectively. Linearity error is determined by not only gain error of stage amplifier but also thermal noise. In addition, we decided that minimum capacitance value is 0.1pF considering some margins.

On the other hand, first S/H shown in Fig. 2-a) is also effective to characteristic of the pipelined ADC. In fact, it must have accuracy that equals to overall resolution. However, gain error of the first S/H does not effect linearity. Therefore, we can determine input capacitance value of S/H by only consideration of thermal noise [2].

As a result, we decided capacitance value for various resolutions as follows.

<table>
<thead>
<tr>
<th>Resolution [bits]</th>
<th>S/H</th>
<th>1st stage</th>
<th>The other stages</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>1.0</td>
<td>0.5</td>
<td>0.1</td>
</tr>
<tr>
<td>8</td>
<td>0.1</td>
<td>0.1</td>
<td>0.1</td>
</tr>
<tr>
<td>6</td>
<td>0.1</td>
<td>0.1</td>
<td>0.1</td>
</tr>
</tbody>
</table>

2) Optimization of amplifiers for low power consumption

We could grantee accuracy of the stage amplifier by the optimization described previously. Therefore, next we must optimize analog blocks in only consideration of sampling frequency. Ideally, folded cascade amplifier has one pole. So,
we can obtain required bias current in consideration of maximum sampling frequency and slew rate as follows.

\[ f = \frac{C}{2\pi a(3C + C_p)} \times \frac{g_m}{C_L} \quad \text{Eq. 4: Maximum Operation Freq.} \]

\[ SR = \frac{I_B}{C_L} \quad \text{Eq. 5: Slew Rate} \]

\( C_L \) output capacitance consisting of input capacitance of next stage and subAD, and feedback loop capacitance of itself. And \( g_m \) is transconductance of the amplifier.

In Eq. 4 and 5, \( C \) is already fixed. So we can control \( g_m \) and \( I_B \) only for low power design.

Next, we describe the method of current optimization of re-use folded cascade amplifier.

1) Channel Width Modification

In the case of modifying channel width of all transistors of amplifier uniformly \( A \) times, frequency characteristic becomes \( A \) times. In spite of this, open loop gain and output voltage range do not change.

2) Bias Current Modification

In the case of modifying bias current \( A \) times, frequency characteristic becomes square root of \( A \) times. However, if bias current is lowered, we must pay attention to turning off of the bias transistor by GND noise. So, lower limit of bias voltage exists.

3) Our Proposed Re-use Amplifier Method

To shorten design period of opamp optimization, we have three opamps in library that have respective channel widths of transistor changed \( x_1, x_{0.5} \) and \( x_{0.25} \) from base opamp.

As mentioned before, to prevent the bias transistor from turning off, we set a lower limit of bias voltage. Therefore, as shown in Fig. 6, we can adjust bias current change from \( I_B \) that means bias current of base opamp to \( I_B x_{0.25} \) continuously without risk and can shorten design period.

![Bias current graph](image)

Fig. 6: Bias current

By this method, we can shorten the optimizing process of an amplifier.

3) Optimization of Comparator

We adopted a differential chopper comparator for its high noise immunity. Characteristic of comparators doesn’t effect so much on overall linearity. Also, dissipation current of comparators is much smaller than that of opamps. Therefore, we have two types of comparators for high/low frequency operation in analog library.

4) Optimization of Bias Generator

Each bias generator is placed by an opamp to be immune from supply voltage variation. Bias voltage variation depends on operation frequency of an opamp, transistor size of a bias transistor, and so on.

However, as mentioned before, dissipation current of bias generators is much smaller than that of opamps. So, we have two types of bias generators for High/Low frequency operation. By this method, we can shorten optimizing process of opamps.

V. SIMULATION RESULTS

In this section, we show some overall simulation results in verification steps of proposed design flow.

We are afraid that low power design approach mentioned in previous section effect worse to overall linearity. So, we must need overall simulation for this verification.

By the way, simulation time with transistor level is too long to get overall results. However, simulation time with analog-HDL is very short. So, we can get linearity information easily. Fig. 7 and 8 show input-output characteristics of 8-bit ADC that are good/bad linearity respectively. By these kinds of simulations, we will evaluate our design.

![Input-output characteristic](image)

Fig. 7: Input-Output Characteristic (Good Linearity)
VI. APPLICATION

We designed two ADCs from the base ADC with our proposed methodology. One is a 6-bit/30 MHz ADC and the other is an 8-bit/60 MHz ADC.

Firstly, we will describe the 6-bit/30MHz ADC. We designed 2-ch ADC. For the reason that sampling frequency becomes lower, there is room for reduction of dissipation current. So, to optimize bias current of opamps, we reduced dissipation current before optimizing. Table 3 and 4 show dissipation current analysis, before and after optimization of analog blocks, respectively. From Table 3 and 4, we can confirm that our optimization methodology is available for re-using analog blocks. Layout of this chip is shown in Fig. 9.

Table 3. Dissipation Current Analysis of 6-bit ADC before optimization of analog blocks

<table>
<thead>
<tr>
<th>Opamp</th>
<th>Bias</th>
<th>Comp</th>
<th>Digital</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>6b/30MHz</td>
<td>8mA</td>
<td>2mA</td>
<td>3mA</td>
<td>4mA</td>
</tr>
</tbody>
</table>

Table 4. Dissipation Current Analysis of 6-bit ADC after optimization of analog blocks

<table>
<thead>
<tr>
<th>Opamp</th>
<th>Bias</th>
<th>Comp</th>
<th>Digital</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>6b/30MHz</td>
<td>1.5mA</td>
<td>0.5mA</td>
<td>1.5mA</td>
<td>4mA</td>
</tr>
</tbody>
</table>

Fig. 9: Chip Layout of 2-ch 6-bit/30MHz ADC

Next, we explain 8-bit/60MHz ADC. Sampling frequency of the base 10-bit ADC is 50MHz. Compared with the base ADC, resolution of this ADC is small. So, load capacitance of opamp is much reduced as mentioned in section III. Consequently, sampling frequency at over 50MHz can be realized by re-using opamps. Fig. 10 shows 2-ch 8-bit/60 MHz ADC.

Fig. 10: Chip Layout of 2-ch 8-bit/60MHz ADC

Lastly, we describe generating 12-bit ADC. 12-bit ADC can be realized with our new design methodology. In this case, operation speed becomes very slow because input capacitance of an opamp for 12-bit accuracy is much larger than that for 10-bit. And in fact it requires high open loop gain of an amplifier compared with 10-bit ADC. However there is possibility that our new design methodology extends to 12-bit ADC. For example, we can increase channel length of transistors and apply an amplifier that has other topology realizing high gain. Consequently, we can draw performance of ADCs that we can obtain with our new design methodology as shown in Fig. 11.

Fig. 11: ADC Performance

VII. SUMMARY

We developed a new design methodology for fast Analog-to-Digital Converter Macros based on our original pipelined ADC. This methodology consists of library re-use methodology and performance driven optimization techniques. We designed 6-bit/30 MHz ADC and 8-bit/60 MHz ADCs from the base ADC with this methodology. And, we can confirm that
our design methodology is available for shortening design period without the sacrifice of performance.

ACKNOWLEDGEMENTS

The authors wish to thank Y. Matsuo for measurements, K. Kato, H. Shimizu, Y. Kimura for helpful discussions, and Y. Harada and K. Yodoshi for their encouragement.

REFERENCES


