Abstract - Manufacturing induced optimizations in the mask preparation step by layout post processing and fabrication inherent imperfections, like trapezoidal interconnect cross sections or variations of the dielectric interlayer thickness, lead to increased mismatches between the layout based timing and signal integrity characterizations and the corresponding Silicon-based behavior measurable after fabrication. Thus, to ensure timing closure between silicon and layout, DFM (Design For Manufacturability) related optimizations need to be taken care of when performing the parasitics extraction step. An example will be given where the mismatch between measurement and layout based extraction data can be demonstrated already for a 0.25μm technology. It will further be shown that the inclusion of simplified process features by applying parameterized 3D-modeling will render sufficiently accurate extraction results. The proposed methodology is in addition efficient enough to handle complex layouts. Thus for all practical purposes parameterized 3D-modeling closes the gap between TCAD tools delivering highest accuracy, but limited to relatively small structures, and more powerful, but insufficiently accurate, standard full chip, layout based extraction tools.

I. Introduction

In today’s most advanced ultra deep sub micron ULSI circuits the steady decrease in minimum feature size and increase in chip size has led to a tremendous amount of total on-chip interconnect length which is currently already on the verge of several kilometers per chip [1]. As at the same time device speed and clock frequencies continue to increase further, the influence of interconnect parasitics on the overall chip performance has taken an increasingly important role, in some cases even dominating active device characteristics.

Therefore, the modeling and extraction of interconnect behavior becomes a very important aspect during design and final verification of a chip. Many approaches have been implemented for taking into account interconnects at several points of the design flow [2]. One of the most crucial points is the extraction of the parasitic RLC elements during the layout verification step since no further checks are carried out before final mask preparation and manufacturing.

Moreover, in current technologies with feature sizes well below quarter micron, the differences between the idealized layout structures in the design database, on which the parasitics extraction for verification is performed, and the interconnect structures found on silicon after fabrication is becoming quite pronounced, making the problem of accurate and reliable interconnect characterization even more difficult.

These differences are not only due to manufacturing inherent process variations of mainly statistical or at least uncontrollable origin, e.g. layer thickness variations during CMP or trapezoidal cross sections, but also due to controlled countermeasures performed to enhance yield, e.g. the introduction of fill structures, or compensation for lithographic and similar effects.

The optimizations are performed in a separate post processing step after verification. During this step the design is manipulated significantly, which has a strong influence on the interconnect behavior. Although many publications in literature [3] - [7] have been focused on capacitance characterization of on-chip interconnects the impact of fill structures and design manipulations for yield enhancement has not been addressed sufficiently. Even more manipulations may arise in the future influencing parasitics as well, such as layout manipulations to deal with optical proximity effects.

An example is being shown where measurements on silicon have been compared to the corresponding extracted data. Very good accuracy can only be achieved by the inclusion of process based features and DFM related layout optimizations together with parameterized 3D-modeling of the interconnects. This methodology is being described in some detail and a verification flow is being proposed as well that accounts for the described features.

In the following the paper focuses mainly on capacitance extraction since this is the most important property when determining signal delays. Resistance and inductance extraction can be accounted for with basically the same approach.

II. Approaches to Parasitics Extraction

A commonly used approach to the extraction and verification of the interconnect parasitics during the design flow is
being described in this section.

The final verification of the timing and signal behavior of
the on-chip interconnects is usually performed on the layout
data that has been prepared during the standard design phase
of the chip under investigation, either automatically by place
& route tools for semi custom design or mostly manually for
full custom design. Thus the final verification is based on
the nominal shape of the interconnect structures. Any
changes that need to be performed for the final mask
preparation step are not included as they are done in a
separate post processing step. It is therefore assumed that the
structures finally to be found on silicon are accurately
described by the layout data and are not further effected by
the post processing and the fabrication process. The next
section shows that this basic assumption will lead to major
mismatches between extraction derived performance esti-
mates and silicon measured performance.

The verification tools available for parasitics extraction
have seen a substantial development over the last years, as
the need for accurate interconnect extraction has been well
known in the industry for some time now. Thus a large
number of different approaches to parasitics extraction have
evolved and are available right now. The methodologies
applied in the extraction tools cover a range that reaches
from coefficient based methods where geometrical opera-
tions like Boolean operations and edge detection are applied
([2], Assura, xCalibre, StarRC), to pattern based solutions
that require a tremendous amount of precharacterized simple
structures ([2], Columbus), to attempts of solving the
Maxwell equations for a complete block by brute force ([2],
Space). They all have in common that they apply a relatively
simple model of the interconnects. The interconnects are
modeled as rectangular shapes without any further features.
The accuracy that can be obtained with these tools is around
2% - 10% as compared to a numerical solution of the
capacitance problem based on the same interconnect model.
The main advantage of these tools is their principal
capability to handle even the largest full chip extraction
problems.

For a more accurate and physically knowledgeable
solution of the interconnect problem, other approaches have
been developed as well ([8] - [11]). They focus on explicitly
handling the physical details that are involved when
performing exposition, deposition and etching during the
fabrication process. In this way very accurate models of the
physical structure of the interconnects can be generated,
even accurate enough to predict SEM microphotographs of
the final silicon. But the numerical effort involved is quite
substantial, thus preventing the application of these methods
to extended layout structures as required for final verifi-
cation. Although some progress has been made in
accelerating the numerical simulations involved by level set
and fast marching methods ([10], [11]), their performance is
still a limiting factor for large scale applications on the full
chip level.

III. Measurement and extraction, a case study

This section presents the results of a comparison between
measurements and standard layout based extracted data for
small test structures that have been fabricated in a quarter
micron CMOS technology [12].

An active circuitry originating from Chen [4] has been
applied to directly measure the on-chip capacitance of a test
structure as compared to a corresponding reference structure.
Measuring the difference between an identical test and
reference structure gives an estimation of the accuracy to be
expected. The measured difference is smaller than 50 aF, and
thus well below the capacitance values of more than 10 fF
to be measured. About 70 test structures have been designed
to allow a more systematic investigation of the issues involved.

In order to achieve high accuracy the extracted data has
been obtained with the full 3-D capacitance extraction
methodology, but limiting the tool to a straightforward rect-
angular interconnect model. The unprocessed original layout
is taken as input. A boundary element based numerical
solver [13] computes the capacitance matrix. The difference
between the extracted capacitance of the reference and test
structure \( C_{\text{meas}} - C_{\text{ref}} \) can be directly compared to the
measured capacitance \( C_{\text{meas}} \). In total the approach closely
resembles the standard parasitics extraction flow for timing
verification.

Table 1 shows a comparison of the measured data to the
extracted data for a selected subset (S1 – S7) of the struc-
tures where the spacing of metal one lines has been varied
from 9x, 7.5x, 6.5x, 4x, 3x, 2x the minimum pitch down to
minimum pitch, see Fig. 1a. Structure S8 is a solid metal one
plate of 50x50 \( \mu \)m\(^2\). Although applying a numerical method,
the differences shown in the second column are as high as
-30%. The case S8 exhibits good agreement between
measurement and extraction which can be explained by the
missing influences of post processing related issues for this
rather large structure. A standard layout extraction system
would exhibit even larger discrepancies due to the added
inherent inaccuracy of these methods.

Tasting a look on all 70 test structures some trends have
been detected summarized by the following items:

- For all test structures the capacitance is under-
  estimated even by the 3-D capacitance extraction using
  the original design. This is caused by missing fill
  structures of poly and active area fills as well as
  neglecting enlargement of line width and process

<table>
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<tr>
<th>No.</th>
<th>( C(\text{meas}) ) [aF]</th>
<th>( C(\text{std}) ) [%]</th>
<th>( C(\text{pp}) ) [%]</th>
<th>( C(\text{full}) ) [%]</th>
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<tr>
<td>S1</td>
<td>1.12e-14</td>
<td>-26.5</td>
<td>-11</td>
<td>-1</td>
</tr>
<tr>
<td>S2</td>
<td>1.11e-14</td>
<td>-25.2</td>
<td>-10</td>
<td>1</td>
</tr>
<tr>
<td>S3</td>
<td>1.14e-14</td>
<td>-26.3</td>
<td>-5.3</td>
<td>2.6</td>
</tr>
<tr>
<td>S4</td>
<td>1.26e-14</td>
<td>-29.5</td>
<td>-16.7</td>
<td>-4.8</td>
</tr>
<tr>
<td>S5</td>
<td>1.35e-14</td>
<td>-30.3</td>
<td>-17</td>
<td>-7.4</td>
</tr>
<tr>
<td>S6</td>
<td>1.60e-14</td>
<td>-33.7</td>
<td>-16.8</td>
<td>-3.8</td>
</tr>
<tr>
<td>S7</td>
<td>1.88e-14</td>
<td>-22.8</td>
<td>-21.3</td>
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</tr>
<tr>
<td>S8</td>
<td>4.92e-14</td>
<td>1.3</td>
<td>1.1</td>
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</tr>
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</table>
specific issues.
• Metal fills do not play an important role for the
capacitance characterization since they are placed several μm apart from signal lines.
• The largest deviations appear in the lowest metal
layer.
• Large differences have been observed as well for
comb like structures which have been designed in
minimal pitch. This can be caused by enlarging the line
width for yield enhancements.
In order to minimize these discrepancies post processing
and process related issues are being taken into account in
the following section.

IV. Consideration of post processing and process
specific effects

A microscopic view (Fig. 1b) of the test structure S7
depicts the designed test structure, the connected circuit and
many additional fill structures in all metal layers, the poly
layer and the active area layer. They can be seen in Fig. 1b
as a regular array of rectangles and l-formed shapes.
Moreover, SEM pictures (Fig. 2, 3) of the vertical cross
section of S1 and S7 exhibit notably different shapes of the
conductors in silicon compared to the nominal ones.
Therefore, two steps have been taken to better match the
measured data so that it can be evaluated how much the
extracted capacitance will change due to each single effect.
First, only corrections for yield enhancement and fill
structures have been inserted into the design. As a result the
comparison improved about 10% for all patterns (Tab. 1,
C(ppp)). Nevertheless, there still is a significant gap.
Including now in a second step all width, thickness and
spacing parameters which have been derived from the SEM
pictures in the 3D-modeling, the agreement to the measured
data is excellent except for the case S7. Obtaining a good
agreement particularly for this structure, a dielectric constant
of εr = 4.4 instead of 4.0 had to be considered besides the
other corrections. The most likely explanation might be that
during deposition some metal atoms diffuse into the isolator
and build a region around the conductor surface possessing a
much higher εr. Since this region is rather thin the enlarged
εr contributes significantly only for minimal spacing. Further
work is necessary to get a deeper understanding of this
behavior.

V. The parameterized 3D-Modeling

As has been shown in the previous section, the inclusion of
detailed information about the shapes of the interconnects
from SEM microphotographs will improve the extraction of
the interconnect parasitics. It still remains to explain how
such models can be generated efficiently and accurately
enough.

The solution proposed in this work is to use the
parameterized 3D-modeling [14]. With this is meant to
replace a physical modeling step (e.g. by performing
accurate TCAD simulations or direct measurements of
fabricated silicon) with a purely geometrical modeling based
on the phenomenology of the interconnects to be
characterized. The physics of the fabrication process will be
reflected in the 3D-structure by the proper application of
some simple parameterized features, e.g. a trapezoidal
conductor cross section, to the basic 2D-layout data. To
allow accurate replication of the real physical structures on
silicon, which is needed to achieve high accuracy, the
parameterized features have to be chosen carefully. Fig. 4
shows the application to test structure S7 of the previous
section as an example.

The whole modeling step thus becomes a purely
geometric operation which can be implemented very
Fig. 4. 3D-Modeling of a part of structure S7. The model includes the fill structures from the post processing step.

efficiently on the input layout data. This facilitates operation on complete blocks, signal busses or clocks which is required during the final extraction to ensure the required accuracy.

The parameterized features found to be most important and chosen for inclusion in the tool currently cover the modeling of non planar, planar and conformal dielectrics (e.g. for low-k technologies and Cu), trapezoidal conductor cross sections (etch effects) and corner rounding of conductors and contacts/vias in the x-y plane (e.g. modeling lithography). Fig. 5 explains the basic features and their parameters.

The implementation takes as input the 2-dimensional layout with the correct netting information attached by the first rough netlist extraction (by directly interfacing to the binary database of a commercially available extractor), and the process description (see Fig. 6).

The first step done in the modeling is the preparation of the input data. The preprocessing will mainly account for the rounding before a corner stitching representation of the layout data to be modeled is generated. The corner stitching data representation ([15], [16]) is especially well suited to this application because it allows immediate access in each corner stitching tile (respectively trapezoid) to the layering above that tile and the height of the individual layout sections present (cf. Fig. 7). The trapezoid representation has been extended to include the description of non Manhattan all angle structures. This information will in turn allow immediate output of the 3-D model either as volume or boundary representation, whichever format is required by the analysis tool to be run on the extracted data. A capacitance extraction for example is done most efficiently with a boundary element solver, only requiring a discretization of the conductor and dielectric boundary.

Fig. 5. The basic parameterized shapes covered in the 3D-modeling tool, a) Modeling of non planar dielectrics (conformal dielectrics included), b) Trapezoidal cross section, c) Rounding of corners.

Another feature implemented is the partitioning of long nets such that effectively independent tasks for the field solver can be generated. Each of the partitions can be solved separately, thus allowing speed-ups almost linear with the number of available computers [17].

The proposed modeling has been integrated in the layout extraction flow by interfacing to a commercially available standard extraction tool (Fig. 8). A rough and rather inaccurate extraction is being used up front to obtain a first rough approximation of the parasitics. By analyzing the extracted data, nets are identified that need higher accuracy in the second refinement step. Usually only a very limited number of nets need further refinement. This allows to spend much more effort on their characterization, in effect allowing to achieve high accuracy for the complete chip.

The presented approach allows the modeling of very large sections of the layout within reasonable time, cf. Fig. 9. The limiting step in the characterization is solving the Maxwell equation to get the numerical results, but here substantial progress has been made as well [18].

VI. Conclusions

In this paper some deficits in the standard extraction methodology for parasitics extraction have been pointed out. They originate from post processing and process specific effects related to DFM optimizations. Neglecting these effects might lead to wrong predictions on the performance of a chip since signal delays are always underestimated within the standard parasitics extraction flow. In fact, a chip...
design that has been signed off after successful verification could fail on silicon. In order to improve the extraction, a methodology has been proposed that applies a parameterized 3D-modeling to selected nets requiring high accuracy and to include all effects of design manipulation and fill structure insertion in the rough pre-estimation step. Considering them will lead to significantly enlarged efforts extracting parasitics but will ensure reliable characterization of the interconnect parasitics when DFM optimizations are performed.

It should be noted as well that if the optimizations were fully accounted for, many of these changes are such that they will not be seen on silicon as they are required to reproduce the nominal layout structures on silicon. Such layout changes should of course never be used for a parasitic extraction. But nevertheless, some will lead to observable changes on the silicon as compared to the layout data base. This is for example true for line widening for isolated lines, which is done for yield enhancement, or the insertion of fill structures for CMP. These need to be taken care of, but only to the amount to be seen on silicon. Other differences between layout and silicon are due to the specific nature of the fabrication process, e.g. the trapezoidal cross section of conductors. For an accurate extraction of the interconnect parasitics such effects need to be handled as well.

Thus the importance of using accurate interconnect characterizations that go beyond the scope of the normal standard parasitics extraction flow to obtain reliable data in comparison with measured silicon results has been shown. In examining the reasons for the discrepancies it has been made clear that the inclusion of more complicated process features significantly improves the accuracy of the layout characterization step. It has also been shown that simply using the existing methods and programs from the TCAD world is not sufficient as they are not capable of processing the complexity of today's designs. TCAD programs should be viewed as an expert's tool to obtain reference results needed to identify the features to be covered in the parameterized modeling.

Instead parameterized 3D-modeling in combination with a two phase extraction can account for the DFM optimization induced effects on the full chip level as required for the final verification of timing and signal integrity.

Acknowledgements

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References

[2] Tools for P&R such as Apollo, Hyperextract, Magma and tools for verification such as Assura, xCalibre, Columbus, Space, StarRC, etc. (enumeration alphabetical).
[8] Tools for TCAD interconnect simulation such as Clever, Taurus-Topography, etc. (enumeration alphabetical).


